E2O0016-39-81

OKI Semiconductor

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MSM82C37B-5RS/GS/VJS

PROGRAMMABLE DMA CONTROLLER

GENERAL DESCRIPTION

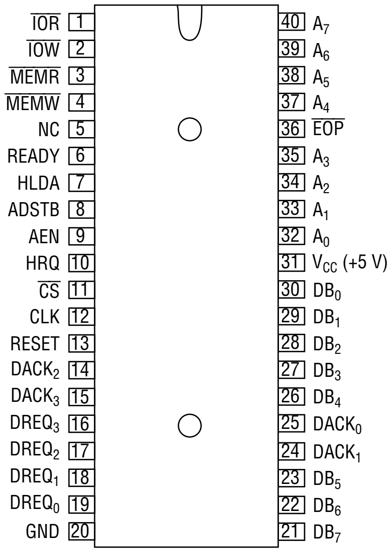
The MSM82C37B-5RS/GS/VJS, DMA (Direct Memory Access) controller is capable of high-speed data transfer without CPU intervention and is used as a peripheral device in microcomputer systems. The device features four independent programmable DMA channels.
Due to the use of silicon gate CMOS technology, standby current is 10 µA (max.), and power consumption is as low as 10 mA (max.) when a 5 MHz clock is generated.
All items of AC characteristics are compatible with intel 8237A-5.

FEATURES

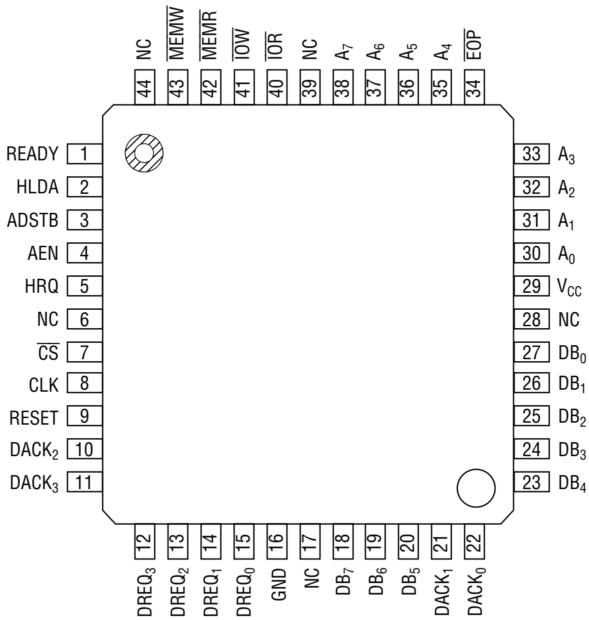
- Maximum operating frequency of 5 MHz (Vcc = 5 V ±10%)
- High-speed operation at very low power consumption due to silicon gate CMOS technology
- Wide operating temperature range from –40°C to +85°C
- 4-channels independent DMA control
- DMA request masking and programming
- DMA request priority function
- DREQ and DACK input/output logic inversion
- DMA address increment/decrement selection
- Memory-to-Memory Transfers
- Channel extension by cascade connection
- DMA transfer termination by EOP input
- Intel 8237A-5 compatibility
- TTL Compatible
- 40-pin Plastic DIP (DIP40-P-600-2.54): (Product name: MSM82C37B-5RS)
- 44-pin Plastic QFJ (QFJ44-P-S650-1.27): (Product name: MSM82C37B-5VJS)
- 44-pin Plastic QFP (QFP44-P-910-0.80-2K): (Product name: MSM82C37B-5GS-2K)

PIN CONFIGURATION (TOP VIEW)

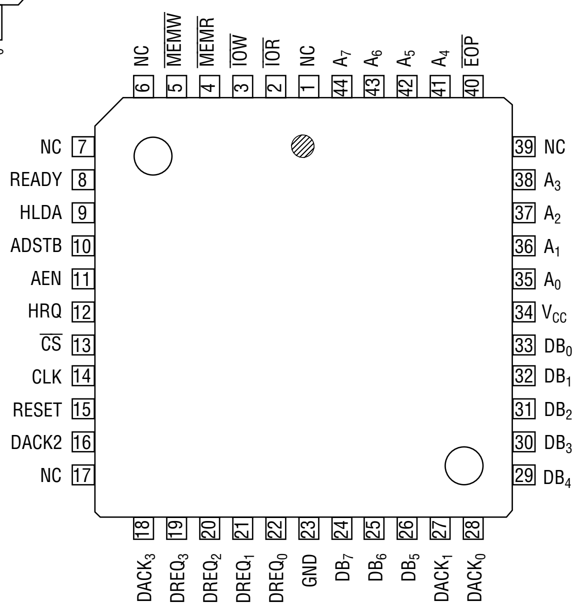
40 pin Plastic DIP



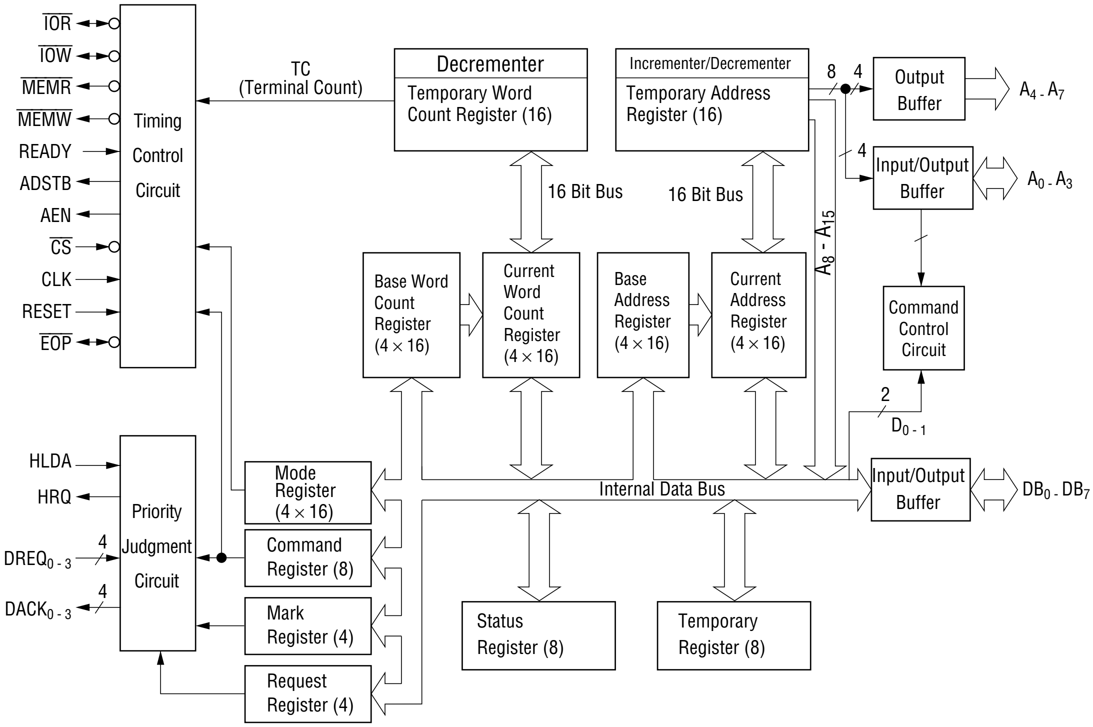
44 pin Plastic QFP



44 pin Plastic QFJ



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating			Unit
			MSM82C37B-5RS	MSM82C37B-5GS	MSM82C37B-5VJS	
Power Supply Voltage	V_{CC}	with respect to GND	–0.5 to +7			V
Input Voltage	V_{IN}	with respect to GND	–0.5 to V_{CC} +0.5			V
Output Voltage	V_{OUT}	with respect to GND	–0.5 to V_{CC} +0.5			V
Storage Temperature	T_{STG}	—	–55 to +150			°C
Power Dissipation	P_D	Ta = 25°C	1.0	0.7	1.0	W

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Operating Temperature	T_{op}	–40	+25	+85	°C
"L" Input Voltage	V_{IL}	–0.5	—	+0.8	V
"H" Input Voltage	T_{IH}	2.2	—	V_{CC} + 0.5	V

DC CHARACTERISTICS

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
"L" Output Voltage	V_{OL}	I_{OL} = 3.2 mA	V_{CC} = 4.5 V to 5.5 V Ta = –40°C to +85°C	—	—	0.4	V
"H" Output Voltage	V_{OH}	I_{OH} = –1.0 mA		3.7	—	—	V
Input Leak Current	I_{LI}	$0V \leq V_{IN} \leq V_{CC}$		–10	—	10	μA
Output Leak Current	I_{LO}	$0V \leq V_{OUT} \leq V_{CC}$		–10	—	10	μA
Average Power Supply Current during Operations	I_{CC}	Input frequency 5 MHz, when RESET V_{IN} = 0 V/V_{CC}, C_L = 0 pF		—	—	10	mA
Power Supply Current in Standby Mode	I_{CCS}	HLDA = 0 V, V_{IL} = 0 V, V_{IH} = V_{CC}		—	—	10	μA

AC CHARACTERISTICS

DMA (Master) Mode

(Ta = –40 to +85°C, V_{CC} = 4.5 to 5.5 V)

Symbol	Item	Min.	Max.	Unit	Comments
t_{AEL}	Delay Time from CLK Falling Edge up to AEN Leading Edge	—	200	ns	—
t_{AET}	Delay Time from CLK Rising Edge up to AEN Trailing Edge	—	130	ns	—
t_{AFAB}	Delay Time from CLK Rising Edge up to Address Floating Status	—	90	ns	—
t_{AFC}	Delay Time from CLK Rising Edge up to Read/Write Signal Floating Status	—	120	ns	—
t_{AFDB}	Delay Time from CLK Rising Edge up to Data Bus Floating Status	—	170	ns	—
t_{AHR}	Address Valid Hold Time to Read Signal Trailing Edge	t_{CY} – 100	—	ns	—
t_{AHS}	Data Valid Hold Time to ADSTB Trailing Edge	30	—	ns	—
t_{AHW}	Address Valid Hold Time to Write Signal Trailing Edge	t_{CY} – 50	—	ns	—
t_{AK}	Delay Time from CLK Falling Edge up to Active DACK	—	170	ns	(Note 3)
	Delay Time from CLK Rising Edge up to $\overline{EOP}$ Leading Edge	—	170	ns	(Note 5)
	Delay Time from CLK Rising Edge up to $\overline{EOP}$ Trailing Edge	—	170	ns	—
t_{ASM}	Time from CLK Rising Edge up to Address Valid	—	170	ns	—
t_{ASS}	Data Set-up Time to ADSTB Trailing Edge	100	—	ns	—
t_{CH}	Clock High-level Time	68	—	ns	(Note 6)
t_{CL}	Clock Low-level Time	68	—	ns	(Note 6)
t_{CY}	CLK Cycle Time	200	—	ns	—

DMA (Master) Mode (continued)

Symbol	Item	Min.	Max.	Unit	Comments
t_{DCL}	Delay Time from CLK Rising Edge to Read/Write Signal Leading Edge	—	190	ns	(Note 2)
t_{DCTR}	Delay Time from CLK Rising Edge to Read Signal Trailing Edge	—	190	ns	(Note 2)
t_{DCTW}	Delay Time from CLK Rising Edge to Write Signal Trailing Edge	—	130	ns	(Note 2)
t_{DQ}	Delay Time from CLK Rising Edge to HRQ Valid	—	120	ns	—
t_{EPS}	$\overline{EOP}$ Leading Edge Set-up Time to CLK Falling Edge	40	—	ns	—
t_{EPW}	$\overline{EOP}$ Pulse Width	220	—	ns	—
t_{FAAB}	Delay Time from CLK Rising Edge to Address Valid	—	170	ns	—
t_{FAC}	Time from CLK Rising Edge up to Active Read/Write Signal	—	150	ns	—
t_{FADB}	Delay Time from CLK Rising Edge to Data Valid	—	200	ns	—
t_{HS}	HLDA Valid Set-up Time to CLK Rising Edge	75	—	ns	—
t_{IDH}	Input Data Hold Time to $\overline{MEMR}$ Trailing Edge	0	—	ns	—
t_{IDS}	Input Data Set-up to $\overline{MEMR}$ Trailing Edge	170	—	ns	—
t_{ODH}	Output Data Hold Time to $\overline{MEMW}$ Trailing Edge	10	—	ns	—
t_{ODV}	Time from Output Data Valid to $\overline{MEMW}$ Trailing Edge	125	—	ns	—
t_{QS}	DREQ Set-up Time to CLK Falling Edge	0	—	ns	(Note 3)
t_{RH}	READY Hold Time to CLK Falling Edge	20	—	ns	—
t_{RS}	READY Set-up Time to CLK Falling Edge	60	—	ns	—
t_{STL}	Delay Time from CLK Rising Edge to ADSTB Leading Edge	—	130	ns	—
t_{STT}	Delay Time from CLK Rising Edge to ADSTB Trailing Edge	—	90	ns	—

Slave Mode

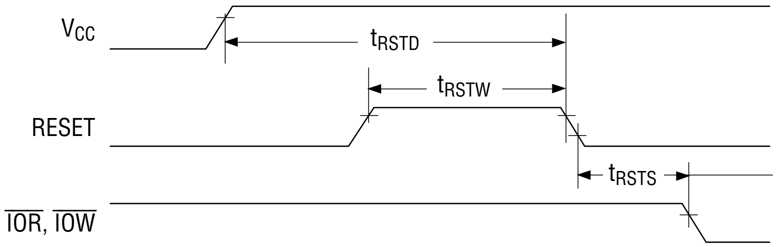
(Ta = –40 to +85°C, V_{CC} = 4.5 to 5.5 V)

Symbol	Item	Min.	Max.	Unit	Comments
t_{AR}	Time from Address Valid or $\overline{CS}$ Leading Edge to $\overline{IOR}$ Leading Edge	50	—	ns	—
t_{AW}	Address Valid Set-up Time to $\overline{IOW}$ Trailing Edge	130	—	ns	—
t_{CW}	$\overline{CS}$ Leading Edge Set-up Time to $\overline{IOW}$ trailing edge	130	—	ns	—
t_{DW}	Data Valid Set-up Time to $\overline{IOW}$ Trailing Edge	130	—	ns	—
t_{RA}	Address or $\overline{CS}$ Hold Time to $\overline{IOR}$ Trailing Edge	0	—	ns	—
t_{RDE}	Data Access Time to $\overline{IOR}$ Leading Edge	—	140	ns	—
t_{RDF}	Delay Time to Data Floating Status from $\overline{IOR}$ Trailing Edge	0	70	ns	—
t_{RSTD}	Supply Power Leading Edge Set-up time to RESET Trailing Edge	500	—	ns	—
t_{RSTS}	Time to First Active $\overline{IOR}$ or $\overline{IOW}$ from RESET Trailing Edge	$2t_{CY}$	—	ns	—
t_{RSTW}	RESET Pulse Width	300	—	ns	—
t_{RW}	$\overline{IOR}$ Pulse Width	200	—	ns	—
t_{WA}	Address Hold Time to $\overline{IOW}$ Trailing Edge	20	—	ns	—
t_{WC}	$\overline{CS}$ Trailing Edge Hold Time to $\overline{IOW}$ Trailing Edge	20	—	ns	—
t_{WD}	Data Hold Time to $\overline{IOW}$ Trailing Edge	30	—	ns	—
t_{WWS}	$\overline{IOW}$ Pulse Width	160	—	ns	—

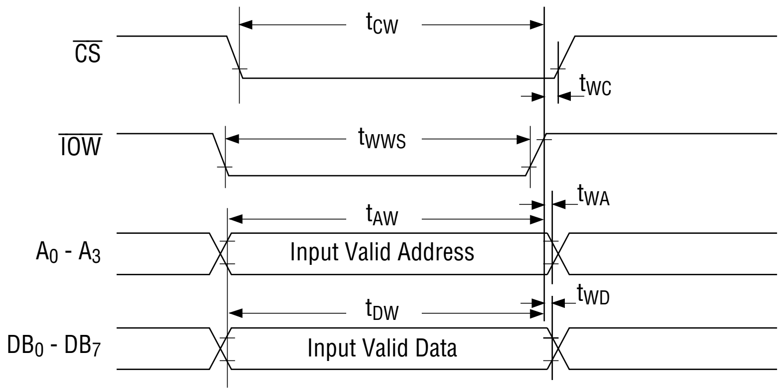
Notes:
1. Output load capacitance of 150 (pF).
2. $\overline{IOW}$ and $\overline{MEMW}$ pulse widths of t_{CY} – 100 (ns) for normal writing, and $2t_{CY}$ – 100 (ns) for extended writing. $\overline{IOR}$ and $\overline{MEMR}$ pulse widths of $2t_{CY}$ – 50 (ns) for normal timing, and t_{CY} – 50 (ns) for compressed timing.
3. DREQ and DACK signal active level can be set to either low or high. In the timing chart, the DREQ signal has been set to active-high, and the DACK signal to active-low.
4. When the CPU executes continuous read or write in programming mode, the interval during which the read or write pulse becomes active must be set to at least 400 ns.
5. $\overline{EOP}$ is an open drain output. The value given is obtained when a 2.2 kΩ pull-up resistance is connected to V_{CC}.
6. Rise time and fall time are less than 10 ns.
7. Waveform measurement points for both input and output signals are 2.2 V for HIGH and 0.8 V for LOW, unless otherwise noted.

TIMING CHART

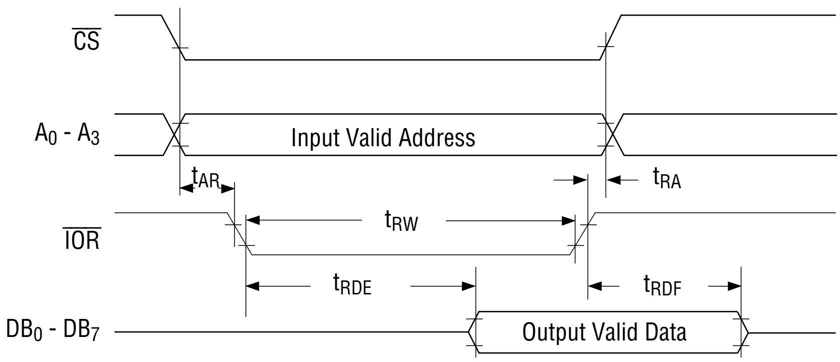
Reset Timing



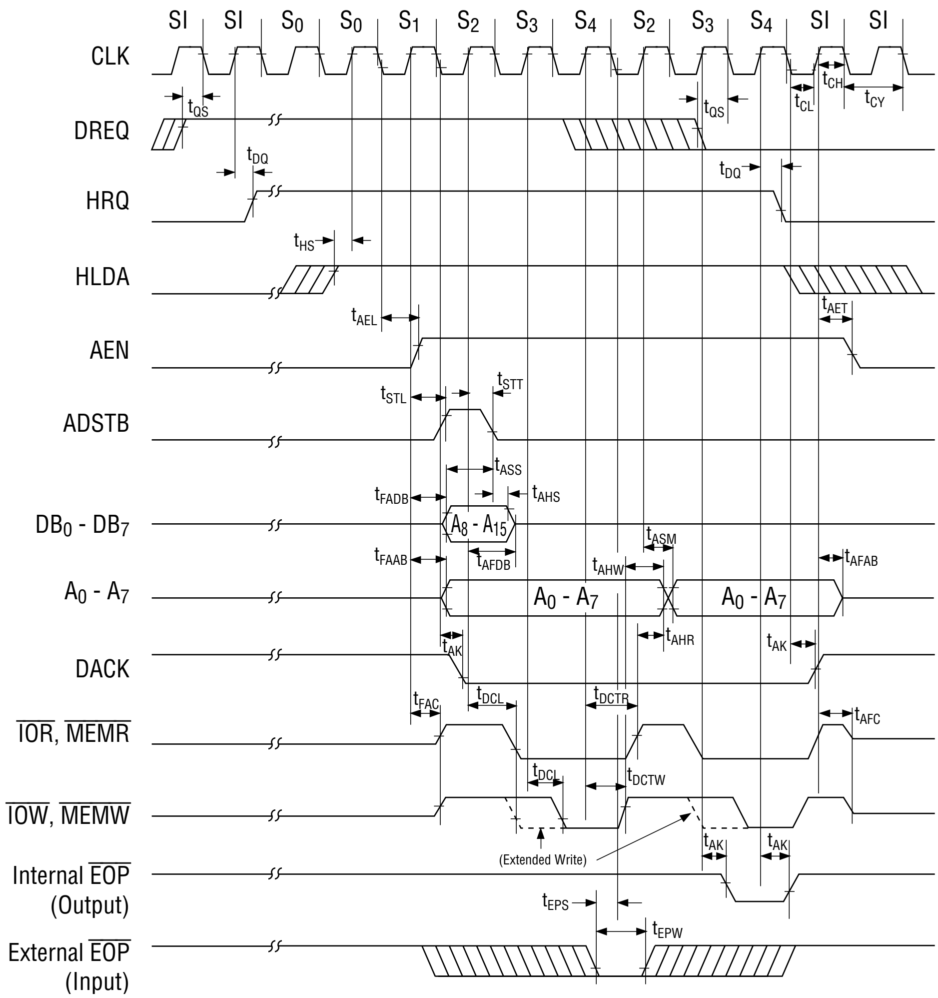
Slave Mode Write Timing



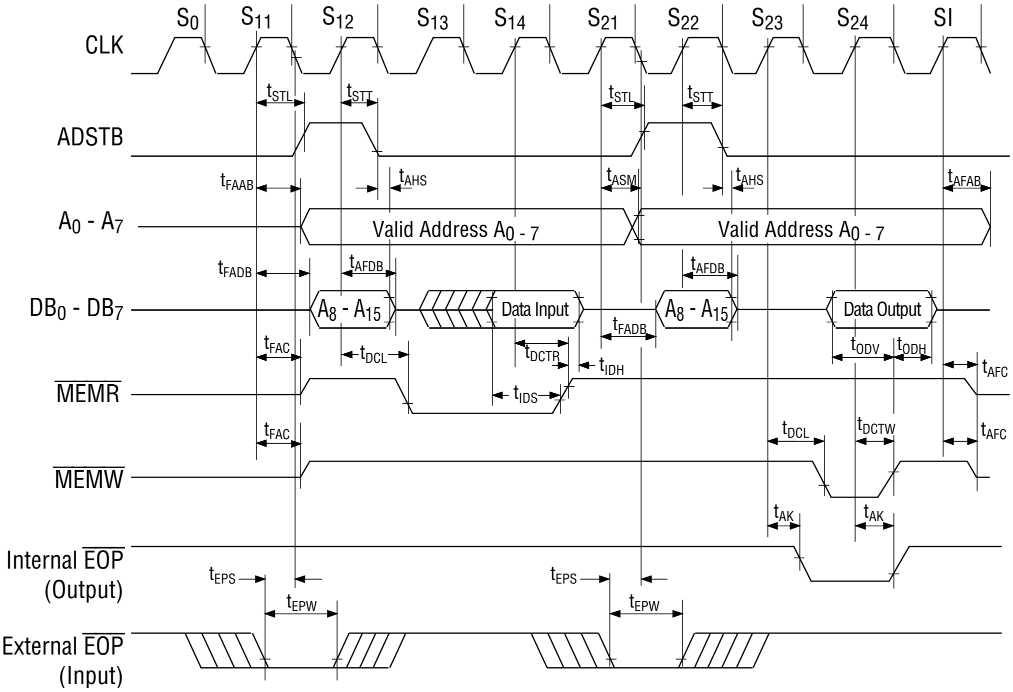
Slave Mode Read Timing



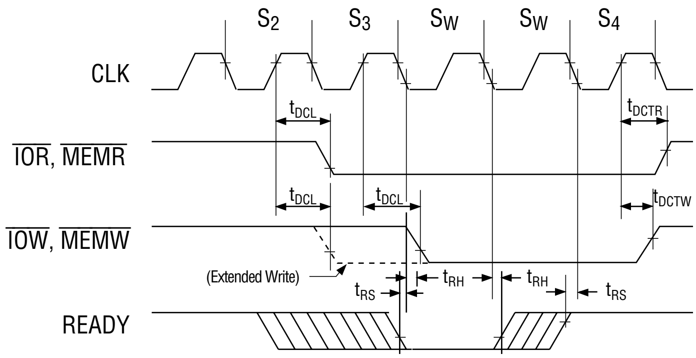
DMA Transfer Timing



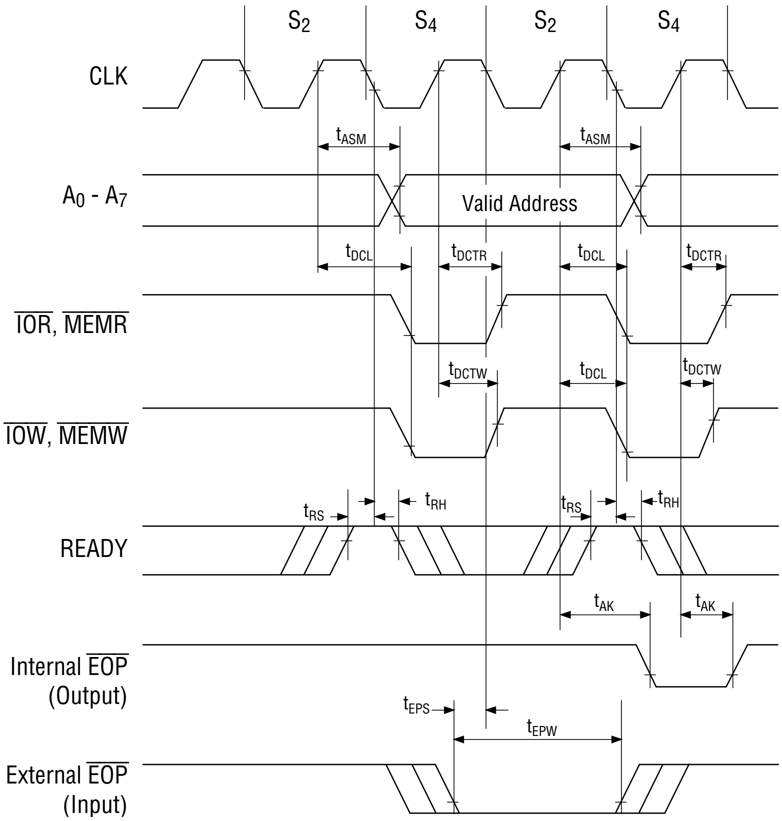
Memory to Memory Transfer Timing



Ready Timing



Compressed Transfer Timing



PIN FUNCTIONS

Symbol	Pin Name	Input/Output	Function
V_{CC}	Power	—	+5 V power supply
GND	Ground	—	Ground (0 V) connection.
CLK	Clock	Input	Control of MSM82C37B-5 internal operations and data transfer speed.
$\overline{CS}$	Chip Select	Input	$\overline{CS}$ is active-low input signal used for the CPU to select the MSM82C37B-5 as an I/O device in an idle cycle.
RESET	Reset	Input	RESET is active-high asynchrounous input signal used to clear command, status, request, temporary registers, and first/last F/F, and to set mask register. The MSM82C37B-5 enters an idle cycle following a RESET.
READY	Ready	Input	The read or write pulse width can be extended to accomodate slow access memories and I/O devices when this input is switched to low level. Note this input must not change within the prescribed set-up/hold time.
HLDA	Hold Acknowledge	Input	HLDA is active-high input signal used to indicate that system bus control has been released when a hold request is recieved by the CPU.
$DREQ_0$ - $DREQ_3$	DMA Request 0 - 3 Channels	Input	DREQ is asynchronous DMA transfer request input signals. Although these pins are switched to active-high by reset, they can be programmed to become active-low. DMA requests are received in accordance with a prescribed order of priority. DREQ must be held until DACK becomes active.
DB_0 - DB_7	Data Bus 0 - 7	Input/Output	DB is bidirectional three-state signals connected to the system data bus, and which is used as an input/output of MSM82C37B-5 internal registers during idle cycles, and as an output of the eight higher order bits of transfer addresses during active cycles. Also used as input and output of transfer data during memory-memory transfers.
$\overline{IOR}$	I/O Read	Input/Output	$\overline{IOR}$ is active-low bidirectional three-state signal used as an input control signal for CPU reading of MSM82C37B-5 internal registers during idle cycles, and as an output control signal for reading I/O device transfer data in writing transfers during active cycles.
$\overline{IOW}$	I/O Write	Input/Output	$\overline{IOW}$ is active-low bidirectional three-state signal used as an input control signal for CPU writing of MSM82C37B-5 internal registers during idle cycles, and as an output control signal for writing I/O device transfer data in writing transfers during active cycles.

PIN FUNCTIONS (continued)

Symbol	Pin Name	Input/Output	Function
$\overline{EOP}$	End of Process	Input/Output	$\overline{EOP}$ is active-low bidirectional three-state signal. Unlike other pins, this pin is an N-channel open drain. During DMA operations, a low-level output pulse is obtained from this pin if the channel word count changes from 0000H to FFFFH. And DMA transfers can be terminated by pulling the $\overline{EOP}$ input to low level. Both of these actions are called terminal count (TC). When internal or external $\overline{EOP}$ is generated, the MSM82C37B-5 terminates the transfer and resets the DMA request. When the EOP pin is not used, it is necessary to hold the pin at high level by pull-up resistor to prevent the input of an EOP by error. Also note that the $\overline{EOP}$ function cannot be satisfied in cascade mode.
A_0 - A_3	Address 0 - 3	Input/Output	A_0 - A_3 is bidirectional three-state signals used as input signals for specifying the MSM82C37B-5 internal register to be accessed by the CPU during idle cycles, and as an output the four lower order bits of the transfer address during active cycles.
A_4 - A_7	Address 4 - 7	Output	A_4 - A_7 is three-state signals used as an output the four higher order bits of the transfer address during active cycles.
HRQ	Hold Request	Output	HRQ is active-high signal used as an output of hold request to the CPU for system data bus control purposes. After HRQ has become active, at least one clock cycle is required before HLDA becomes active.
$DACK_0$ - $DACK_3$	DMA Acknowledge 0 - 3 Channels	Output	DACK is output signals used to indicate that DMA transfer to peripheral devices has been permitted. (Available in each channel.) Although these pins are switched to active-low when reset, they can be programmed to become active-high. Note that there is no DACK output signal during memory-memory transfers.
AEN	Address Enable	Output	AEN is active-high ouput signal used to indicate that output signals sent from the MSM82C37B-5 to the system are valid. And in addition to enabling external latch to hold the eight higher order bits of the transfer address, this signal is also used to disable other system bus buffers.
ADSTB	Address Strobe	Output	ADSTB is active-high signal used to strobe the eight higher order bits of the transfer address by external latch.
$\overline{MEMR}$	Memory Read	Output	$\overline{MEMR}$ is active-low three-state output signal used as a control signal in reading data from memory during read transfers and memory-memory transfers.
$\overline{MEMW}$	Memory Write	Output	$\overline{MEMW}$ is active-low three-state output signal used as a control signal in writing data into memory during write transfers and memory-memory transfers.

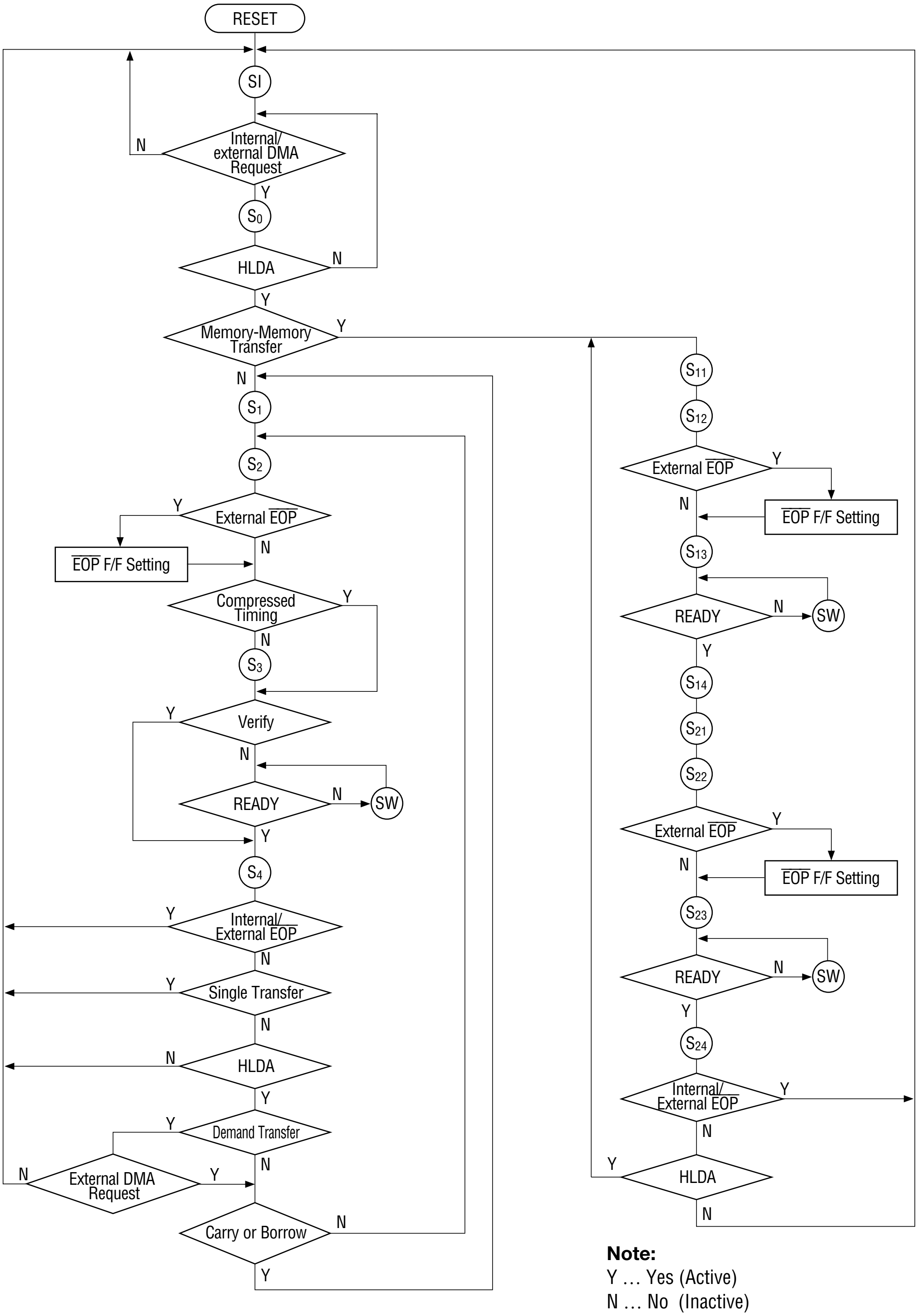


Figure 1 DMA Operation State Transition Diagram

OUTLINE OF FUNCTIONS

The MSM82C37B-5 consists of five blocks = three logic sections, an internal register section, and a counter section.
The logic sections include a timing control block where the internal timing and external control signals are generated, a command control block where each instruction from the CPU is decoded, and a priority decision block where the order of DMA channel priority is determined. The purpose of the internal register section is to hold internal states and instructions from the CPU, while the counter section computes addresses and word counts.

DESCRIPTION OF OPERATIONS

The MSM82C37B-5 operates in two cycles (called the idle and active cycles) which are divided into independent states. Each state is commenced by a clock falling edge and continues for a single clock cycle. The transition from one state to the next in DMA operations is outlined in Figure 1.

Idle Cycle

The idle cycle is entered from the SI state when there is no valid DMA request on any MSM82C37B-5 channel. During this cycle, DREQ and $\overline{CS}$ inputs are monitored during each cycle. When a valid DMA request is then received, an active cycle is commenced. And if the HLDA and $\overline{CS}$ inputs are at low level, a programming state is started with MSM82C37B-5 reading or writing executed by $\overline{IOR}$ or $\overline{IOW}$. Programming details are described later.

Active Cycle

If a DMA request is received in an unmasked channel while the MSM82C37B-5 is in idle cycle, or if a software DREQ is generated, the HRQ is changed to high level to commence an active cycle. The initial state of an active cycle is the S_0 state which is repeated until the HLDA input from the CPU is changed to high level. (But because of internal operational reasons, a minimum of one clock cycle is required for the HLDA is be changed to high level by the CPU after the HRQ has become high level. That is, the S_0 state must be repeated at least twice.)
After the HLDA has been changed to high level, the S_0 state proceeds to operational states S1 thru S_4 during I/O-memory transfers, or to operational states S_{11} thru S_{14} and S_{21} thru S_{24} during memory-memory transfers.
If the memory or I/O device cannot be accessed within the normal timing, an SW state (wait state) can be inserted by a READY input to extend the timing.

DESCRIPTION OF TRANSFER TYPES

MSM82C37B-5 transfers between an I/O and memory devices, or transfers between memory devices. The three types of transfers between I/O and memory devices are read, write, and verify.

I/O-Memory Transfers

The operational states during an I/O-memory transfer are S_1, S_2, S_3, and S_4.
In the S_1 state, an AEN output is changed to high level to indicate that the control signal from the MSM82C37B-5 is valid. The eight lower order bits of the transfer address are obtained from A_0 thru A_7, and the eight higher order bits are obtained from DB_0 thru DB_7. The ADSTB output is changed to high level at this time to set the eight higher order bits in an external address latch, and the DACK output is made active for the channel where the DMA request is acknowledged. Where there is no change in the eight higher bit transfer address during demand and block mode transfers, however, the S_1 state is omitted.
In the S_2 state, the $\overline{IOR}$ or $\overline{MEMR}$ output is changed to low level.
In the S_3 state, $\overline{IOW}$ or $\overline{MEMW}$ is changed to low level. Where compressed timing is used, however, the S_3 state is omitted.
The S_2 and S_3 states are I/O or memory input/output timing control states. In the S_4 state, $\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$, and $\overline{MEMW}$ are changed to high level, and the word count register is decremented by 1 while the address register is incremented (or decremented) by 1. This completes the DMA transfer of one word.
Note that in I/O-memory transfers, data is transferred directly without being taken in by the MSM82C37B-5. The differences in the three types of I/O-memory transfers are indicated below.

Read Transfer

Data is transferd from memory to the I/O device by changing $\overline{MEMR}$ and $\overline{IOW}$ to low level. $\overline{MEMW}$ and $\overline{IOR}$ are kept at high level during this time.

Write Transfer

Data is transferred from the I/O device to memory by changing $\overline{MEMW}$ and $\overline{IOR}$ to low level. $\overline{MEMR}$ and $\overline{IOW}$ are kept at high level during this time.
Note that writing and reading in these write and read transfers are with respect to the memory.

Verify Transfer

Although verify transfers involve the same operations as write and read transfers (such as transfer address generation and $\overline{EOP}$ input responses),they are in fact pseudo transfers where all I/O and memory reading/writing control signals are kept inactive. READY inputs are disregarded in verify transfers.

Memory-memory Transfer

Memory-memory transfers are used to transfer data blocks from one memory area to another. Memory-memory transfers require a total of eight states to complete a single transfer four states (S_{11} thru S_{14}) for reading from memory, and four states (S_{21} thru S_{24}) for writing into memory. These states are similar to I/O-memory transfer states, and are distinguished by using two-digit numbers. In memory-memory transfers, channel 0 is used for reading data from the source area, and channel 1 is used for writing data into the destination area. During the initial four states, data specified by the channel 0 address is read from the memory when MEMR is made active, and is taken in the MSM82C37B-5 temporary register. Then during the latter four states, the data in the temporary register is written in the address specified by channel 1. This completes the transfer of one byte of data. With channel 0 and channel 1 addresses subsequently incremented (or decremented) by 1, and channel 0, 1 word count decremented by 1, this operation is repeated. The transfer is terminated when the word count reaches FFFF(H) from 0000(H), or when an $\overline{\text{EOP}}$ input is applied from an external source. Note that there is no DACK output signal during this transfer.
The following preparations in programming are requiring to enable memory-memory transfers to be started.

Command Register Setting

Memory-memory transfers are enabled by setting bit 0. Channel 0 address can be held for all transfers by setting bit 1. This setting can be used to enable 1-word contents of the source area to be written into the entire destination area.

Mode Register Setting

The transfer type destination is disregarded in channels 0 and 1. Memory-memory transfers are always executed in block transfer mode.

Request Register Setting

Memory-memory transfers are started by setting the channel 0 request bit.

Mask Register Setting

Mask bits for all channels are set to prevent selection of any other channel apart from channel 0.

Word Count Register Setting

The channel 1 word count is validated, while the channel 0 word count is disregarded.
In order to autoinitialize both channels, it is necessary to write the same values into both word count registers.

DESCRIPTION OF OPERATION MODES

Single Transfer Mode

In single transfer mode, only one word is transferred, and the addresses are incremented (or decremented) by 1 while the word count is decremented by 1. The HRQ is then changed to low level to return the bus control to the CPU. If DREQ remains active after completion of a transfer, the HRQ is changed to low level. After the HLDA is changed to low level by the CPU, and then changes the HRQ back to high level to commence a fresh DMA cycle. For this reason, a machine cycle can be inserted between DMA cycles by the CPU.

Block Transfer Mode

Once a DMA transfer is started in block mode, the transfer is continued until terminal count (TC) status is reached.
If DREQ remains active until DACK becomes active, the DMA transfer is continued even if DREQ becomes inactive.

Demand Transfer Mode

The DMA transfer is continued in demand transfer mode until DREQ is no longer active, or until TC status is reached.
During a DMA transfer, intermediate address and word count values are held in the current address and current word count registers. Consequently, if the DMA transfer is suspended as a result of DREQ becoming inactive before TC status is reached, and the DREQ for that channel is then made active again, the suspended DMA transfer is resumed.

Cascade Transfer Mode

When DMA transfers involving more than four channels are required, connecting a multiple number of MSM82C37A-5 devices in a cascade connection (see Figure 2) enables a simple system extension. This mode is set by setting the first stage MSM82C37B-5 channel to cascade mode. The DREQ and DACK lines for the first stage MSM82C37B-5 channel set to cascade mode are connected to the HRQ and HLDA lines of the respective MSM82C37B-5 devices in the second stage. The first stage MSM82C37B-5 DACK signal must be set to active-high, and the DREQ signal to active-low.
Since the first stage MSM82C37B-5 is only used functionally in determining the order of priority of each channel when cascade mode is set, only DREQ and DACK are used–all other inputs are disregarded. And since the system may be hung up if the DMA transfer is activated by software DREQ, do not set a software DREQ for channels where cascade mode has been set.
In addition to the dual stage cascade connection shown in Figure 2, triple stage cascade connections are possible with the second stage also set to cascade mode.

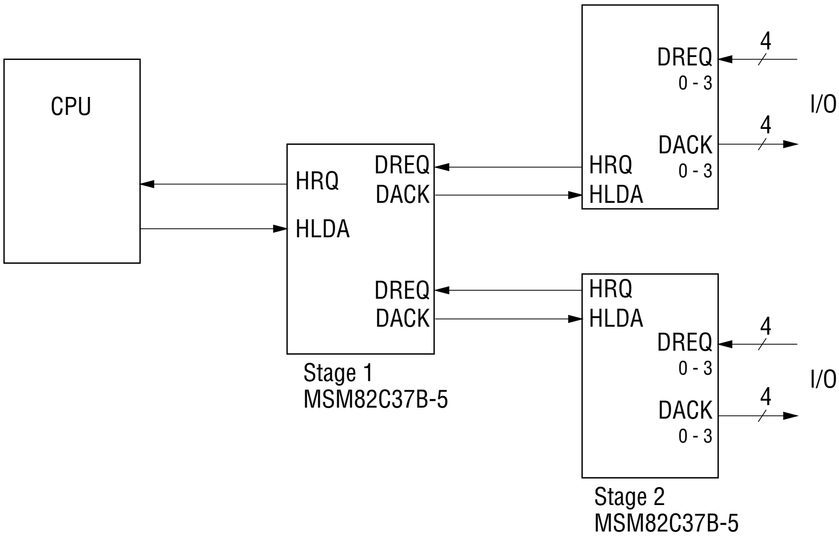


Figure 2 MSM82C37B-5 Cascade Connection System

Autoinitialize Mode

Setting bit 4 of the mode register enables autoinitialization of that channel. Following TC generation, autoinitialize involves writing of the base address and the base word count register values in the respective current address and current word count registers. The same values as in the current registers are written in the base registers by the CPU, and are not changed during DMA transfers. When a channel has been set to autoinitialize, that channel may be used in a second transfer without involving the CPU and without the mask bit being reset after the TC generation.

Priority Modes

The MSM82C37B-5 makes use of two priority decision modes, and acknowledges the DMA channel of highest priority among the DMA requesting channels.

Fixed Priority Mode

In fixed priority mode, channel 0 has the highest priority, followed by channels 1, 2, and 3 in that order.

Rotating Priority Mode

In rotating priority mode, the order of priority is changed so that the channel where the current DMA transfer has been completed is given lowest priority. This is to prevent any one channel from monopolizing the system.
The fixed priority is regained immediately after resetting.

Table 1 MSM82C37B-5 Priority Decision Modes

Priority Mode		Fixed	Rotating			
Service Terminated Channel		—	CH_0	CH_1	CH_2	CH_3
Order of Priority for Next DMA	Highest	CH_0	CH_1	CH_2	CH_3	CH_0
	↕	CH_1	CH_2	CH_3	CH_0	CH_1
		CH_2	CH_3	CH_0	CH_1	CH_2
	Lowest	CH_3	CH_0	CH_1	CH_2	CH_3

Compressed Timing

Setting the MSM82C37B-5 to compressed timing mode enables the S_3 state used in extension of the read pulse access time to be omitted (if permitted by system structure) for two or three clock cycle DMA transfers. If the S_3 state is omitted, the read pulse width becomes the same as the write pulse width with the address updated in S_2 and the read or write operation executed in S_4. This mode is disregarded if the transfer is a memory-memory transfer, transfer.

Extended Writing

When this mode is set, the $\overline{IOW}$ or $\overline{MEMW}$ signal which normally appears during the S_3 state is obtained during the S_2 state, thereby extending the write pulse width. The purpose of this extended write pulse is to enable the system to accomodate memories and I/O devices where the access time is slower. Although the pulse width can also be extended by using READY, that involves the insertion of a SW state to increase the number of states.

DESCRIPTION OF INTERNAL REGISTERS

Current Address Register

Each channel is equipped with a 16-bit long current address register where the transfer address is held during DMA transfers. The register value is incremented (or decremented) in each DMA cycle. Although this register is 16 bits long, the CPU is accessed by the MSM82C37B-5 eight bits at a time, therefore necessitating two successive 8-bit (lower and higher order bits) reading or writing operations using internal first/last flip-flops.
When autoinitialize has been set, the register is automatically initialized to the original value after TC.

Current Word Count Register

Each channel is also equipped with a 16 bit-long current word count register where the transfer count is held during DMA transfers. The register value is decremented in each DMA cycle. When the word count value reaches FFFF(H) from 0000(H), a TC is generated. Therefore, a word count value which is one less than the actual number of transfers must be set.
Since this register is also 16 bits long, it is accessed by first/last flip-flops control in the same way as the address register. And if autoinitialize has been set, the register is automatically initialized to the original value after TC.

Base Address Register and Base Word Count Register

Each channel is equipped with a 16-bit long base address register and base word count register where the initial value of each current register is held. The same values are written in each base register and the current register by the CPU. The contents of the current register can be made ready by the CPU, but the content of the base register cannot be read.

Command Register

This 8-bit write-only register prescribes DMA operations for all MSM82C37B-5 channels. An outline of all bits is given in Figure 3. When the controller is disabled by setting D B_2, there is no HRQ output even if DMA request is active.
DREQ and DACK signals may be active high or active low by setting D B_6 and DB_7.

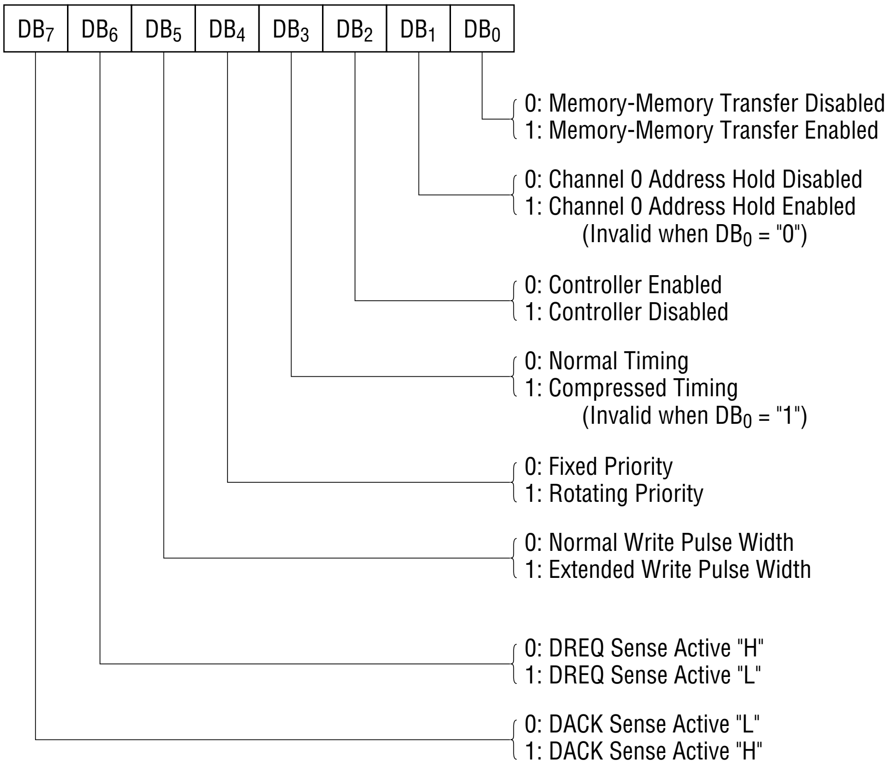


Figure 3 Command Register

Mode Register

Each channel is equipped with a 6-bit write-only mode register, which is decided by setting DB_0, DB_1 which channel is to be written when writing from CPU is programming status. The bit description is outlined in Figure 4.
This register is not cleared by Reset or Master Clear instruction.

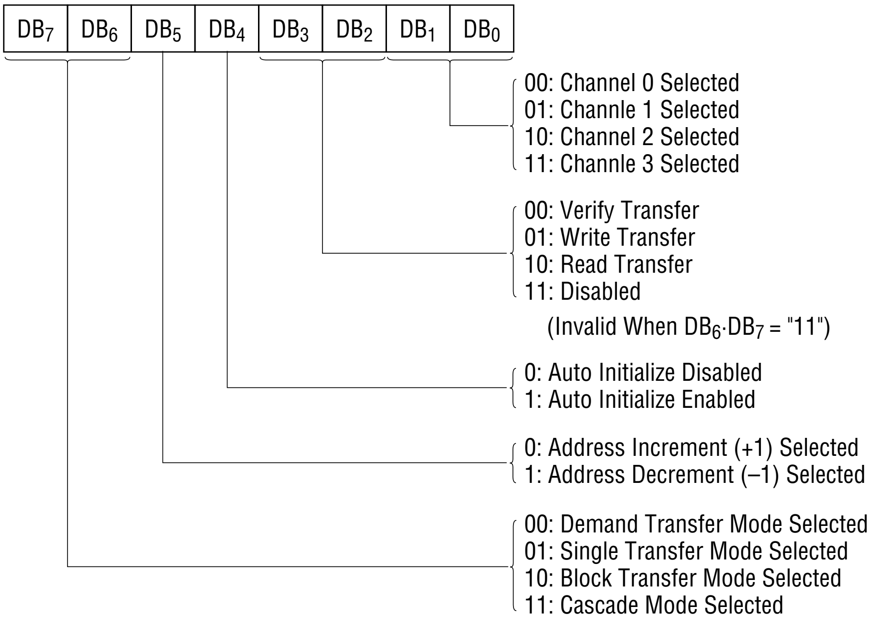


Figure 4 Mode Register

Request Register

In addition to using the DREQ signal, the MSM82C37B-5 can request DMA transfers by software means. This involves setting the request bit of request register. Each channel has a corresponding request bit in the request register, and the order of priority of these bits is determined by the priority decision circuit irrespective of the mask register. DMA transfers are acknowledged in accordance with the decided order of priority.
All request bits are reset when the TC is reached, and when the request bit of a certain channel has been received, all other request bits are cleared. When a memory-memory transfer is commenced, the channel 0 request bit is set. The bit description is outlined in Figure 5.

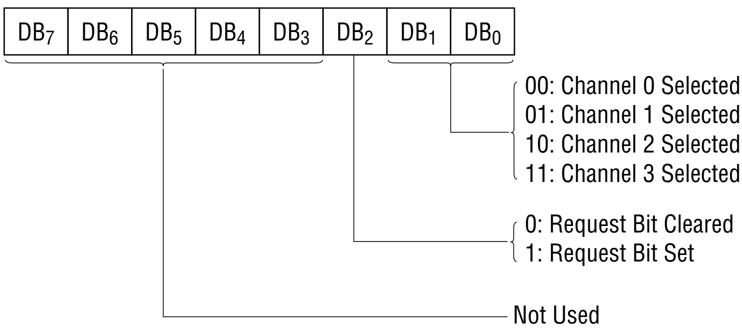
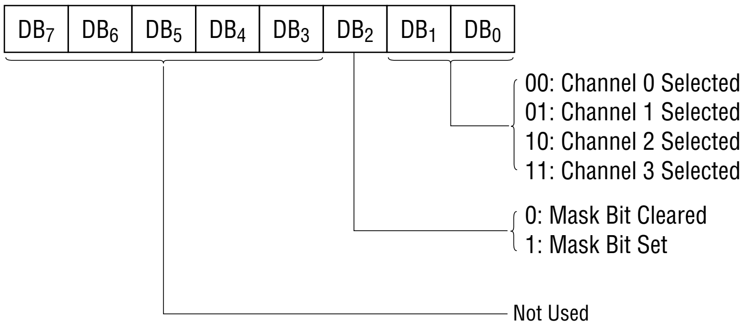


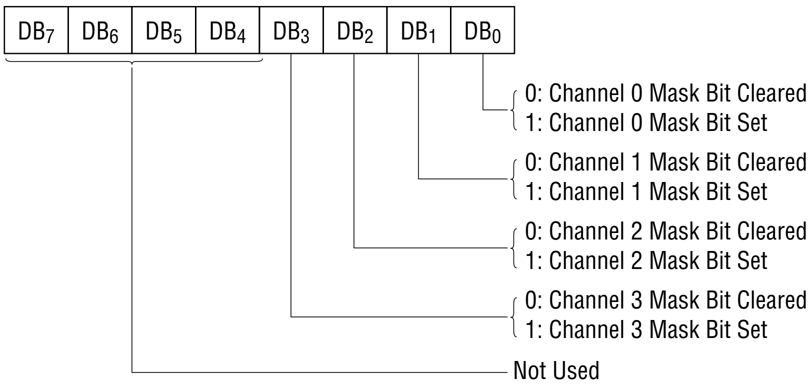
Figure 5 Request Register

Mask Register

This register is used in disabling and enabling of DMA transfers in each channel. Each channel includes a corresponding mask bit in the mask register, and each bit is set when the TC is reached if not in autoinitialize mode. This mask register can be set in two different ways.
The method for setting/resetting the register for each channel is outlined in Figure 6(a), while the method for setting/resetting the register for all channels at once is outlined in Figure 6(b).



(a) Single Mask Register (Setting/Resetting for Each Channel)



(b) All Mask Register (Setting/Resetting of All Channels at Once)

Figure 6 Mask Register

Status Register

This register is a read-only register used in CPU reading of the MSM82C37B-5 status. The four higher order bits indicate the DMA transfer request status for each channel, '1' being set when the DREQ input signal is active.
The four lower order bits indicate whether the corresponding channel has reached the TC or not, '1' being set when the TC status is reached. These four lower order bits are reset by status register reading, or RESET input and master clearing. A description of each bit is outlined in Figure 7

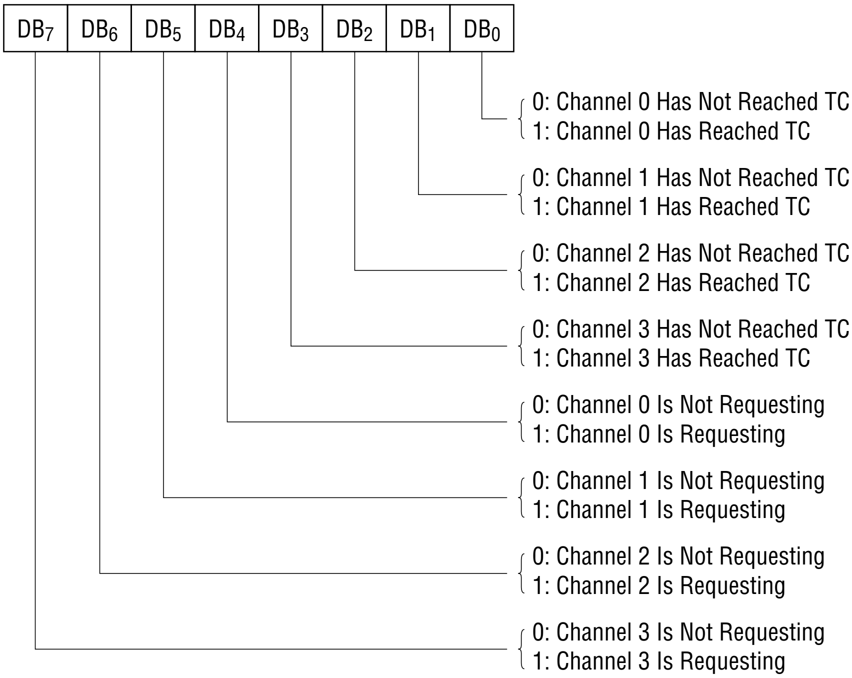


Figure 7 Status Register

Temporary Register

The temporary register is a register where transfer data is held temporarily during memory-memory transfers. Since the last item of data to be transferred is held after completion of the transfer, this item can be read by the CPU.

Software Command

The MSM82C37B-5 is equipped with software commands for executing special operations to ensure proper programming. Software command is irrespective of data bus contents.

Clear First/Last Flip-Flop

16-bit address and word count registers are read or written in two consecutive operations involving eight bits each (higher and lower order bits) under data bus port control. The fact that the lower order bits are accessed first by the MSM82C37B-5, followed by accessing of the higher order bits, is discerned by the internal first/last flip-flop. This command resets the first/last flip-flop with the eight lower order bits being accessed immediately after execution.

Master Clear

The same operation as when the hardware RESET input is applied. Thus command clears the contents of the command, status (four lower order bits), request, and temporary registers, also clears the first/last flip-flop, and sets the mask register. This command is followed by an idle cycle.

Clear Mask Register

When this command is executed, the mask bits for all channels are cleared to enable reception of DMA transfers.

PROGRAMMING

The MSM82C37B-5 is switched to programming status when the HLDA input and $\overline{CS}$ are both at low level. In this state, $\overline{IOR}$ is changed to low level with $\overline{IOW}$ held at high level to enable reading by the CPU, or else $\overline{IOW}$ is changed to low level while $\overline{IOR}$ is held at high level to enable writing by the CPU. A list of command codes for reading from the MSM82C37B-5 is given in Table 2, and a list of command codes for writing in the MSM82C37B-5 is given Table 3.

Note: If a DMA transfer request is received from an I/O device during MSM82C37B-5 programming, that DMA transfer may be commenced to prevent proper programming. To prevent this interference, the DMA channel must be masked, or the controller disabled by the command register, or the system set to as to prevent DREQ becoming active during the programming.

Table 2 List of MSM82C37B-5 Read Commands

$\overline{CS}$	$\overline{IOR}$	A_3	A_2	A_1	A_0	Internal First/Last Flip/Flop	Read Out Data		
0	0	0	0	0	0	0	Channel 0	Current Address Register	8 Lower Order Bits
0	0	0	0	0	0	1			8 Higher Order Bits
0	0	0	0	0	1	0		Current Word Count Register	8 Lower Order Bits
0	0	0	0	0	1	1			8 Higher Order Bits
0	0	0	0	1	0	0	Channel 1	Current Address Register	8 Lower Order Bits
0	0	0	0	1	0	1			8 Higher Order Bits
0	0	0	0	1	1	0		Current Word Count Register	8 Lower Order Bits
0	0	0	0	1	1	1			8 Higher Order Bits
0	0	0	1	0	0	0	Channel 2	Current Address Register	8 Lower Order Bits
0	0	0	1	0	0	1			8 Higher Order Bits
0	0	0	1	0	1	0		Current Word Count Register	8 Lower Order Bits
0	0	0	1	0	1	1			8 Higher Order Bits
0	0	0	1	1	0	0	Channel 3	Current Address Register	8 Lower Order Bits
0	0	0	1	1	0	1			8 Higher Order Bits
0	0	0	1	1	1	0		Current Word Count Register	8 Lower Order Bits
0	0	0	1	1	1	1			8 Higher Order Bits
0	0	1	0	0	0	×	Status Register		
0	0	1	1	0	1	×	Temporary Register		
0	0	Other Combinations				×	Output Data Invalid		

Table 3 List of MSM82C37B-5 Write Commands

$\overline{CS}$	$\overline{IOW}$	A_3	A_2	A_1	A_0	Internal First/Last Flip-Flop	Written Data		
0	0	0	0	0	0	0	Channel 0	Current and Base Address Registers	8 Lower Order Bits
0	0	0	0	0	0	1			8 Higher Order Bits
0	0	0	0	0	1	0		Current and Base Word Count Registers	8 Lower Order Bits
0	0	0	0	0	1	1			8 Higher Order Bits
0	0	0	0	1	0	0	Channel 1	Current and Base Address Registers	8 Lower Order Bits
0	0	0	0	1	0	1			8 Higher Order Bits
0	0	0	0	1	1	0		Current and Base Word Count Registers	8 Lower Order Bits
0	0	0	0	1	1	1			8 Higher Order Bits
0	0	0	1	0	0	0	Channel 2	Current and Base Address Registers	8 Lower Order Bits
0	0	0	1	0	0	1			8 Higher Order Bits
0	0	0	1	0	1	0		Current and Base Word Count Registers	8 Lower Order Bits
0	0	0	1	0	1	1			8 Higher Order Bits
0	0	0	1	1	0	0	Channel 3	Current and Base Address Registers	8 Lower Order Bits
0	0	0	1	1	0	1			8 Higher Order Bits
0	0	0	1	1	1	0		Current and Base Word Count Registers	8 Lower Order Bits
0	0	0	1	1	1	1			8 Higher Order Bits
0	0	1	0	0	0	×	Command Register		
0	0	1	0	0	1	×	Request Register		
0	0	1	0	1	0	×	Single Mask Register		
0	0	1	0	1	1	×	Mode Register		
0	0	1	1	0	0	×	Clear First/Last Flip-Flop (Software Command)		
0	0	1	1	0	1	×	Master Clear (Software Command)		
0	0	1	1	1	0	×	Clear Mask Register (Software Command)		
0	0	1	1	1	1	×	All Mask Register		

NOTICE ON REPLACING LOW-SPEED DEVICES WITH HIGH-SPEED DEVICES

The conventional low speed devices are replaced by high-speed devices as shown below.
When you want to replace your low speed devices with high-speed devices, read the replacement notice given on the next pages.

High-speed device (New)	Low-speed device (Old)	Remarks
M80C85AH	M80C85A/M80C85A-2	8-bit MPU
M80C86A-10	M80C86A/M80C86A-2	16-bit MPU
M80C88A-10	M80C88A/M80C88A-2	8-bit MPU
M82C84A-2	M82C84A/M82C84A-5	Clock generator
M81C55-5	M81C55	RAM, I/O, timer
M82C37B-5	M82C37A/M82C37A-5	DMA controller
M82C51A-2	M82C51A	USART
M82C53-2	M82C53-5	Timer
M82C55A-2	M82C55A-5	PPI

Differences between MSM82C37A-5 and MSM82C37B-5

1) Manufacturing Process

These devices use a 3 μ Si-CMOS process technology and have the same chip size.

2) Function

These devices have the same logics except for changes in AC characteristics listed in (3-2).

3) Electrical Characteristics

3-1) DC Characteristics

These devices have the same DC characteristics.

3-2) AC Characteristics

Parameter	Symbol	MSM82C37A-5	MSM82C37B-5
Clock Low Time (at automatic initialization)	t_{CL}	100 ns minimum	68 ns minimum
Clock Low Time (Other than the above)	t_{CL}	68 ns minimum	68 ns minimum

As shown above, the MSM82C37A-5 cannot satisfy the clock low time of 68 ns (at automatic initialization). On the other hand, the MSM82C37B-5 can satisfy the clock low time of 68 ns in any operation status. As for the other characteristics, both the MSM82C37A-5 and the MSM82C37B-5 are identical.

4) Package

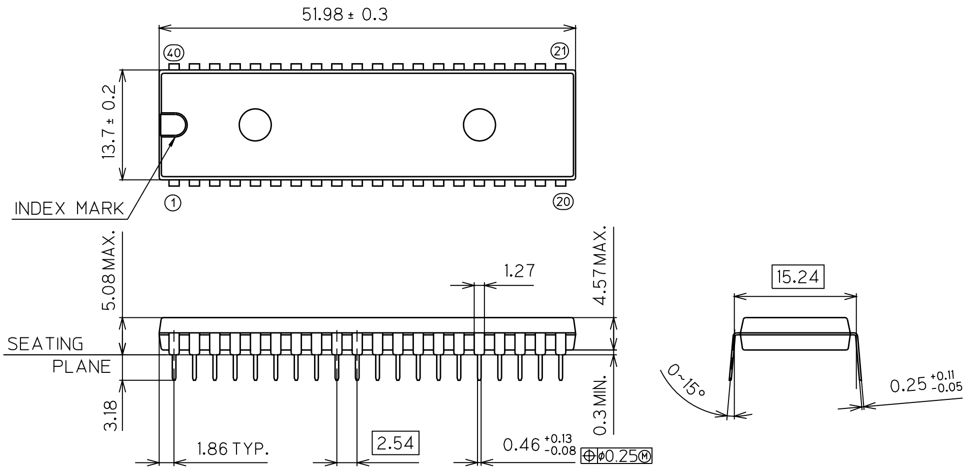
The MSM82C37A-5 employed a PLCC package having OKI's original pin layout, which is not compatible to AMD's PLCC products which has been commercialized before OKI's products.

To meet overseas customers needs, OKI has developed AMD-compatible PLCC productsMSM82C37B-VJS. The OKI's DIP and FLAT package are identical to those of AMD.

PACKAGE DIMENSIONS

(Unit : mm)

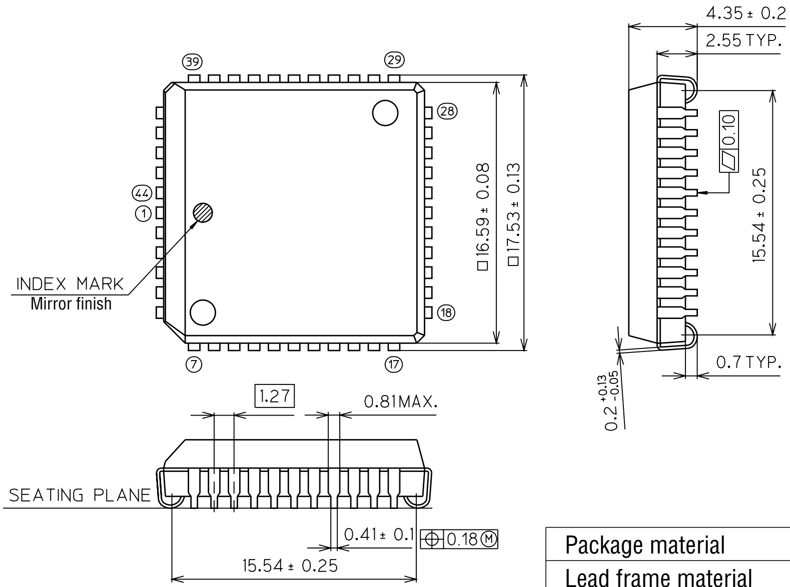
DIP40-P-600-2.54



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 µm or more
Package weight (g)	6.10 TYP.

(Unit : mm)

QFJ44-P-S650-1.27



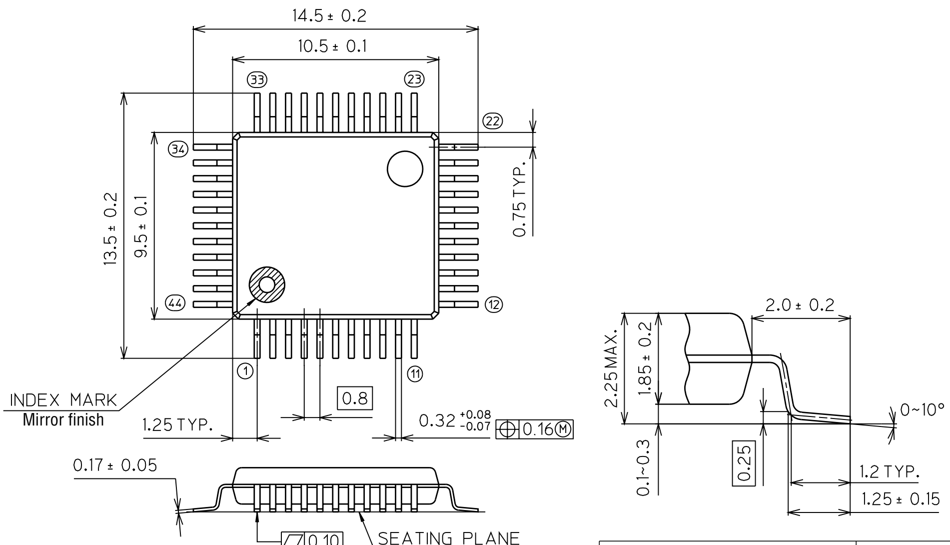
Package material	Epoxy resin
Lead frame material	Cu alloy
Pin treatment	Solder plating
Solder plate thickness	5 µm or more
Package weight (g)	2.00 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ, QFJ (PLCC), SHP, and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

QFP44-P-910-0.80-2K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.41 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ, QFJ (PLCC), SHP, and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

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