OKI Semiconductor

MSM54V16258B/BSL

262,144-Word x 16-Bit DYNAMIC RAM : FAST PAGE MODE TYPE WITH EDO

DESCRIPTION

The MSM54V16258B/BSL is a 262,144-word x 16-bit dynamic RAM fabricated in OKI's CMOS silicon gate technology. The MSM54V16258B/BSL achieves high integration,high-speed operation,and low-power consumption due to quadruple polysilicon double metal CMOS. The MSM54V16258B/BSL is available in a 40-pin plastic SOJ or 44/40-pin plastic TSOP.

FEATURES

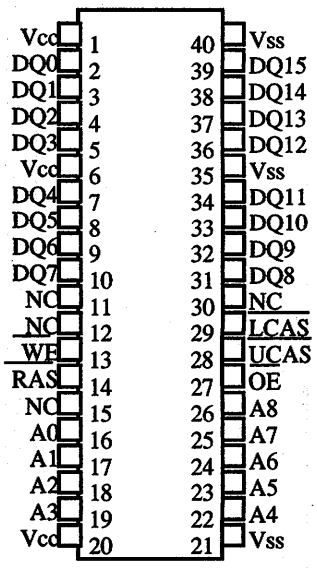
- Single3.3V power supply, ±0.3V tolerance
- Input :TTL compatible
- Output :TTL compatible, 3-state
- Refresh : 512 cycles/64ms
- Fast page mode with EDO,read modify write capability
- Byte wide control: 2 CAS control
- CAS before RAS refresh, Hidden refresh, RAS only refresh capability
- CAS before RAS self-refresh capability (SL Version.)
- Pachage : 40-Pin 400 mil plastic SOJ (SOJ40-P-400) (Product : MSM54V16258B/BSL-xxJS)
  44/40-Pin 400 mil plastic TSOP (TSOP44/40-P-400/0.8-K) (Product : MSM54V16258B-xxTS-K)
  (Product : MSM54V16258BSL-xxTSK)

xx : indicates speed rank.

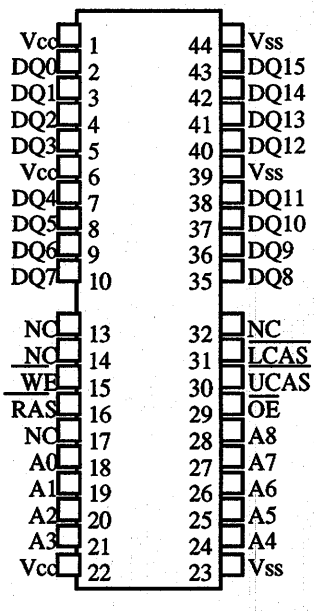
PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)		Power Dissipation
	t_{RAC}	t_{AA}	t_{CAC}	t_{OEA}	t_{RC}	t_{HPC}	
MSM54V16258B/BSL-40	40ns	22ns	10ns	10ns	80ns	15ns	432mW
MSM54V16258B/BSL-45	45ns	24ns	12ns	12ns	90ns	17ns	396mW
MSM54V16258B/BSL-50	50ns	26ns	12ns	14ns	100ns	20ns	360mW

PIN CONFIGURATION (TOP VIEW)



40Pin 400mil SOJ



44/40Pin 400mil TSOP

Pin Names	Function
A0-A8	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{LCAS}$,$\overline{UCAS}$	Column Address Strobe
DQ0-15	Data-Input/ Data-Output
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
Vcc	Power Supply (3.3V)
Vss	Ground (0V)
NC	No Connection

Note1 :
The same power supply voltage must be provided to every Vcc pin, and the same GND voltage level must be provided to every Vss pin.

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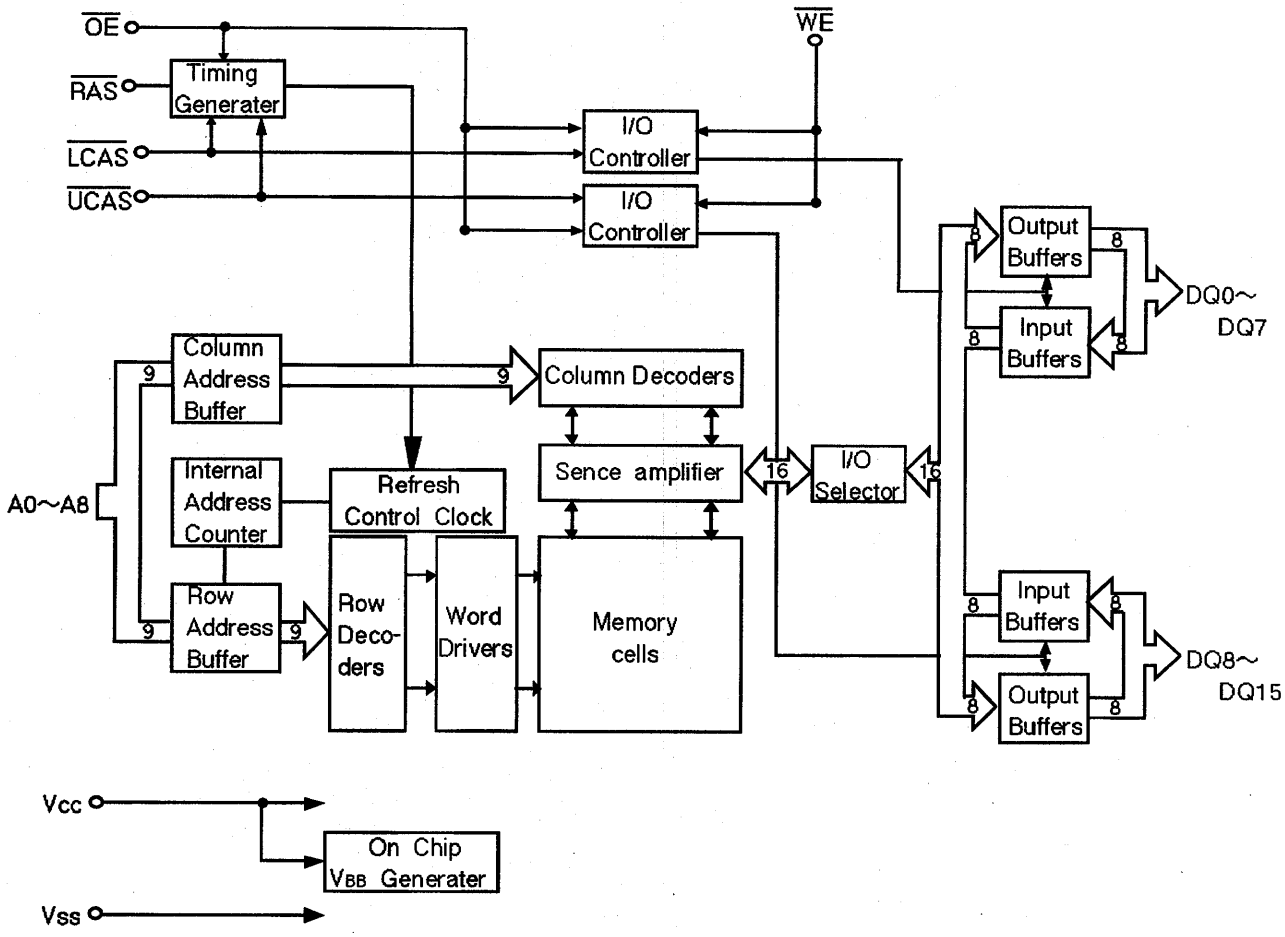
BLOCK DIAGRAM



FUNCTION TABLE

Input Pin					DQPin		Functinal Mode
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	DQ0~DQ7	DQ8~DQ15	
H	*	*	*	*	High-Z	High-Z	Standby
L	H	H	*	*	High-Z	High-Z	Refresh
L	L	H	H	L	DOUT	High-Z	Lower Byte Read
L	H	L	H	L	High-Z	DOUT	Upper Byte Read
L	L	L	H	L	DOUT	DOUT	Word Read
L	L	H	L	H	DIN	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	DIN	Upper Byte Write
L	L	L	L	H	DIN	DIN	Word Write
L	L	L	H	H	High-Z	High-Z	—

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Rating	Symbol	Conditions	Value	Unit
Voltage on any pin relative to Vss	Vt	Ta=25℃	-0.5～+4.6	V
Short circuit output current	Ios	Ta=25℃	50	mA
Power dissipation	P_D	Ta=25℃	1	W
Operrating temperrature	Topr	—	0～+70	℃
Storage temperature	Tstg	—	-55～+150	℃

Recommended Operating Conditions

(Ta=0℃ to 70℃)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	—	3.0	3.3	3.6	V
	Vss	—	0	0	0	V
Input high voltage	V_{IH}	—	2.4	—	Vcc+0.3	V
Input low voltage	V_{IL}	—	-0.3	—	0.8	V

Capacitance

(Vcc=3.3V±0.3V,Ta=25℃,f=1MHz)

Parameter	Symbol	Conditions	Typ.	Max.	Unit
Input capacitance (A0～A8)	C_{IN1}	—	—	8	pf
Input capacitance ($\overline{RAS}$,$\overline{LCAS}$,$\overline{UCAS}$,$\overline{WE}$,$\overline{OE}$)	C_{IN2}	—	—	8	pf
Input / output capacitance (DQ0～DQ15)	$C_{I/O}$	—	—	9	pf

DC CHARACTERISTICS

(V_{CC}=3.3V±0.3V , Ta=0 to 70°C)

Parameter	Symbol	Condition	MSM54V16258 B/BSL-40		MSM54V16258 B/BSL-45		MSM54V16258 B/BSL-50		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	I_{OH}= - 1.0mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	I_{OL}= 2.0mA	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	I_{LI}	0V≦V_{IN}≦Vcc	-10	10	-10	10	-10	10	μA	
Output Leakage Current	I_{LO}	DQi Disable 0V≦V_O≦5.5V	-10	10	-10	10	-10	10	μA	
Average Power Supply Current (Operating)	I_{CC1}	$\overline{RAS}$,$\overline{CAS}$ Cycling t_{RC}=Min.	—	120	—	110	—	100	mA	1,2
Power Supply Current (Standby)	I_{CC2}	$\overline{RAS}$,$\overline{CAS}$ = V_{IH}	—	2	—	2	—	2	mA	1
Average Power Supply Current ($\overline{RAS}$ only Refresh)	I_{CC3}	$\overline{RAS}$=Cycling $\overline{CAS}$=V_{IH} t_{RC}=Min.	—	110	—	100	—	90	mA	1,2
Average Power Supply Current (Fast Page Mode)	I_{CC4}	$\overline{RAS}$=V_{IL} $\overline{CAS}$ Cycling t_{HPC}=Min.	—	70	—	65	—	60	mA	1,3
Average Power Supply Current ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	I_{CC5}	$\overline{RAS}$=Cycling $\overline{CAS}$ Befor $\overline{RAS}$	—	100	—	90	—	80	mA	1,2
Average Power Supply Current (Battery Backup)	I_{CC6}	tRC=125 μs $\overline{CAS}$ Befor $\overline{RAS}$ tRAS≦1 μs	—	300	—	300	—	300	μA	1,2,4,5
Average Power Supply Current ($\overline{CAS}$ Before $\overline{RAS}$ Self-Refresh)	I_{CC7}	$\overline{RAS}$=V_{IL} $\overline{CAS}$=V_{IL}	—	300	—	300	—	300	μA	1,2,4,5

Notes : 1. Icc Max. is specified as Icc for the output open cindition
2. Address can be changed once or less while RAS=VIL.
3. Address can be changed once or less while CAS=VIH.
4. Vcc-0.2V≦VIH≦6.5V , -1.0V≦VIL≦0.2V.
5. SL version.

AC CHARACTERISTICS (1/2)

(Vcc = 3.3V ± 0.3V, Ta = 0~70°C)

Parameter	Symbol	MSM54V16258 B/BSL-40		MSM54V16258 B/BSL-45		MSM54V16258 B/BSL-45		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Random read or write cycle time	tRC	80	—	90	—	100	—	ns	
Read/Write cycle time	tRMW	115	—	130	—	145	—	ns	
Fast page mode cycle time	tHPC	15	—	17	—	20	—	ns	
Fast page mode read/write cycle time	tPRMW	55	—	60	—	65	—	ns	
Access time from $\overline{RAS}$	tRAC	—	40	—	45	—	50	ns	7,12,13
Access time from $\overline{CAS}$	tCAC	—	10	—	12	—	14	ns	7,12
Access time from column address	tAA	—	22	—	24	—	26	ns	7,13
Access time from $\overline{OE}$	tOEA	—	10	—	12	—	14	ns	
Access time from $\overline{CAS}$ precharge	tCPA	—	24	—	26	—	28	ns	7,12
Output low impedance time from $\overline{CAS}$	tCLZ	0	—	0	—	0	—	ns	
Data hold after $\overline{CAS}$ low	tCOH	3	—	3	—	3	—	ns	17
Output buffer turn-off delay time	tOFF	3	8	3	8	3	8	ns	8
Output buffer turn-off delay time from $\overline{OE}$	tOEZ	3	8	3	8	3	8	ns	8
Output buffer turn-off delay time from $\overline{RAS}$	tREZ	3	8	3	8	3	8	ns	8
Output buffer turn-off delay time from $\overline{WE}$	tWEZ	3	8	3	8	3	8	ns	8
Transition time	tT	2	35	2	35	2	35	ns	
Refresh preiod	tREF	—	64	—	64	—	64	ms	
$\overline{RAS}$ precharge time	tRP	30	—	35	—	40	—	ns	
$\overline{RAS}$ pulse width	tRAS	40	10,000	45	10,000	50	10,000	ns	
$\overline{RAS}$ pulse width (Fast page mode)	tRASP	40	100,000	45	100,000	50	100,000	ns	
$\overline{RAS}$ hold time	tRSH	8	—	10	—	10	—	ns	
$\overline{RAS}$ hold time reference to $\overline{OE}$	tROH	8	—	8	—	10	—	ns	
$\overline{CAS}$ precharge time	tCP	5	—	6	—	7	—	ns	
$\overline{CAS}$ pulse width	tCAS	6	10,000	7	10,000	8	10,000	ns	
$\overline{CAS}$ hold time	tCSH	40	—	45	—	50	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5	—	5	—	5	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	18	30	18	33	20	38	ns	12
$\overline{RAS}$ to column address delay time	tRAD	13	18	13	21	15	24	ns	
Row address set-up time	tASR	0	—	0	—	0	—	ns	13
Row address hold time	tRAH	8	—	8	—	10	—	ns	
Column address set-up time	tASC	0	—	0	—	0	—	ns	
Column address hold time	tCAH	5	—	6	—	8	—	ns	
Column address hold time from $\overline{RAS}$	tAR	30	—	30	—	35	—	ns	
Column address to $\overline{RAS}$ lead time	tRAL	22	—	24	—	26	—	ns	
Read command set-up time	tRCS	0	—	0	—	0	—	ns	
Read command hold time	tRCH	0	—	0	—	0	—	ns	9
Read command hold time reference to $\overline{RAS}$	tRRH	0	—	0	—	0	—	ns	9
$\overline{WE}$ pulse width	tWEP	10	—	10	—	10	—	ns	

AC CHARACTERISTICS (2/2)

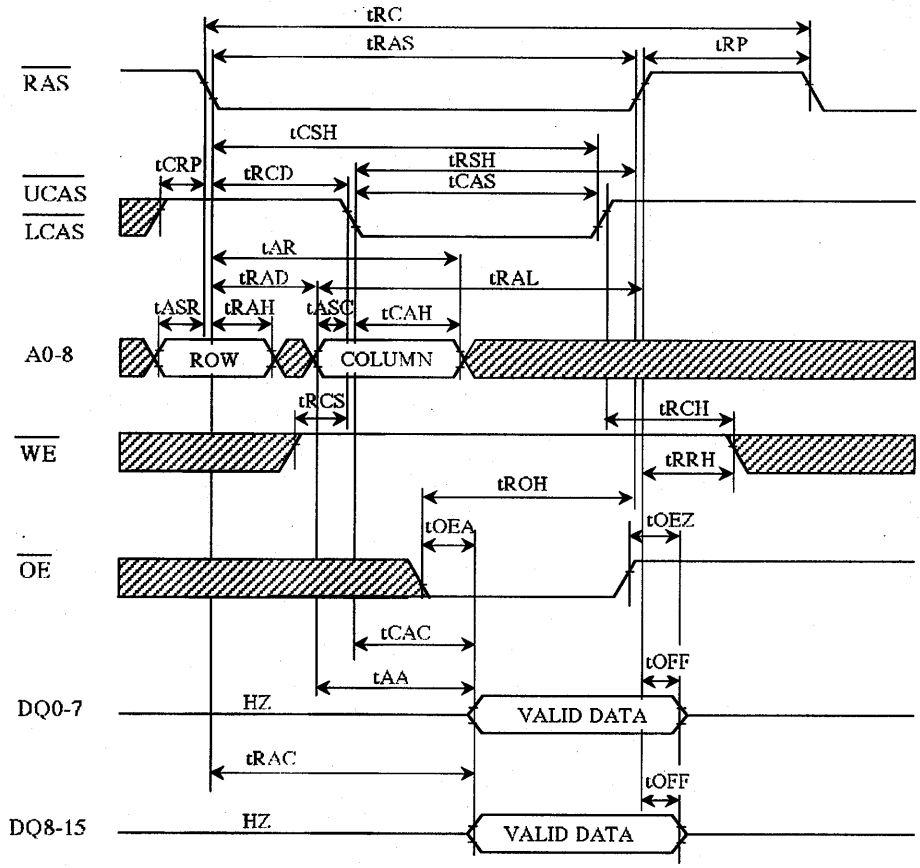
(Vcc = 3.3V ± 0.3V, Ta = 0~70°C)

Parameter	Symbol	MSM54V16258 B/BSL-40		MSM54V16258 B/BSL-45		MSM54V16258 B/BSL-50		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Write command set-up time	t_{WCS}	0	—	0	—	0	—	ns	
Write command hold time	t_{WCH}	7	—	8	—	9	—	ns	
Write command pulse width	t_{WP}	7	—	8	—	9	—	ns	
Write command hold time from $\overline{RAS}$	t_{WCR}	30	—	30	—	35	—	ns	
$\overline{OE}$ command hold time	t_{OEH}	7	—	8	—	9	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	7	—	8	—	9	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	8	—	12	—	14	—	ns	
Data to $\overline{CAS}$ delay time	t_{DZC}	0	—	0	—	0	—	ns	
Data to BE/$\overline{OE}$ delay time	t_{DZO}	0	—	0	—	0	—	ns	
Data-in set-up time	t_{DS}	0	—	0	—	0	—	ns	10
Data-in hold time	t_{DH}	6	—	7	—	8	—	ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	30	—	30	—	35	—	ns	
$\overline{OE}$ to Data delay time	t_{OED}	8	—	8	—	8	—	ns	
$\overline{OE}$ "L" to $\overline{CAS}$ "H" lead time	t_{OCH}	10	—	10	—	10	—	ns	
$\overline{CAS}$ "H" to $\overline{OE}$ "L" lead time	t_{CHO}	10	—	10	—	10	—	ns	
Hi-Z command pulse width	t_{OEP}	10	—	10	—	10	—	ns	
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	28	—	30	—	32	—	ns	11
Column address to $\overline{WE}$ delay time	t_{AWD}	38	—	40	—	44	—	ns	11
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	55	—	60	—	65	—	ns	11
$\overline{CAS}$ active delay time from $\overline{RAS}$ precharge	t_{RPC}	0	—	0	—	0	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	10	—	10	—	10	—	ns	
$\overline{RAS}$ pulse width ($\overline{CAS}$ before $\overline{RAS}$ self-refresh)	t_{RASS}	100	—	100	—	100	—	us	19
$\overline{RAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$ self-refresh)	t_{RPS}	100	—	100	—	100	—	ns	19
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ self-refresh)	t_{CHS}	-40	—	-40	—	-40	—	ns	19

Notes:

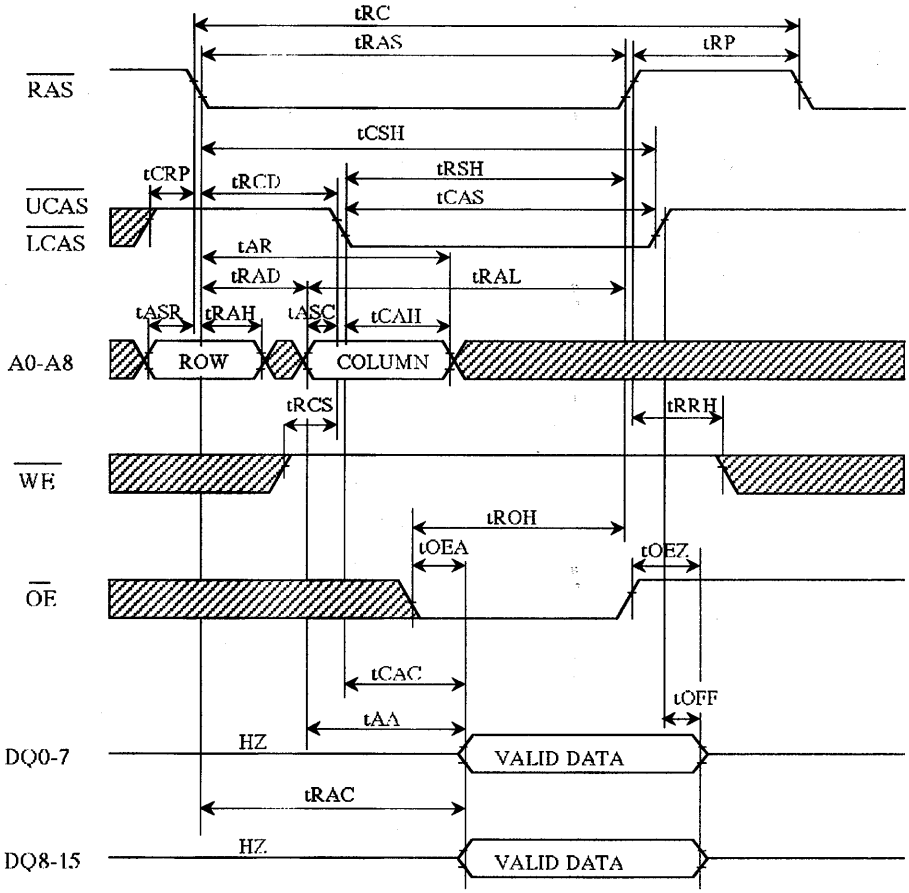
1. All voltages are referenced to Vss.
2. This parameter is dependent upon the cycle rate.
3. This parameter is dependent upon the output loading. Specified values are obtained with the output open.
4. An initial pause of 200 μs is required after power-up, followed by any 8$\overline{RAS}$ cycles. (Example: $\overline{RAS}$-only-refresh) before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8$\overline{CAS}$ before $\overline{RAS}$ cycles instead of 8$\overline{RAS}$ cycles are required.
5. The AC characteristics assume t_T=5ns.
6. V_{IH} (Min.)and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Data outputs are measured with a load of 30 pF. DOUT reference levels: V_{OH}/V_{OL}=1.8V/1.4V.
8. t_{REZ} (Max.), t_{OFF} (Max.), t_{WEZ} (Max.) and t_{OEZ} (Max.) define the time at which the outputs achieve the open circuit condition and are not referebced to output voltage levels. This parameter is sampled and not 100 % tested.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to $\overline{CAS}$ leadind edge of early write cycles and to $\overline{WE}$ leading edge in $\overline{OE}$-controlled write cycles and read-modify-write cycles.
11. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (Min.), the cycle is an early write cycle and the data out pins will remain open circuit throughout the entire cycle. If $t_{RWD} \geqq t_{RWD}$ (Min.), $t_{CWD} \geqq t_{CWD}$ (Min.) and $t_{AWD} \geqq t_{AWD}$ (Min.), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither or the above sets of conditions is satisfied, the condition of the data out is indetermunate.
12. Operation within the t_{RCD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled by t_{CDC}.
13. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, then access time is controlled by t_{AA}.
14. Input levels at the AC testing are 3.0V/0V.
15. Addresses (A0 - A8) may be changed two times or less while $\overline{RAS}$ =V_{IL}.
16. Addresses (A0 - A8) may be changed once or less while $\overline{CAS}$ =V_{IH} and $\overline{RAS}$ =V_{IL}.
17. This is guaranteed by design. (t_{COH}=t_{CAC} - output transition time). This parameter is not 100 % tested.
18. This parameter is dependent upon the number of address transitions. Specified values are measured with a maximum of two transitions per address cycle in Fast Page Mode.
19. SL version.

READ CYCLE ($\overline{RAS}$ output control)



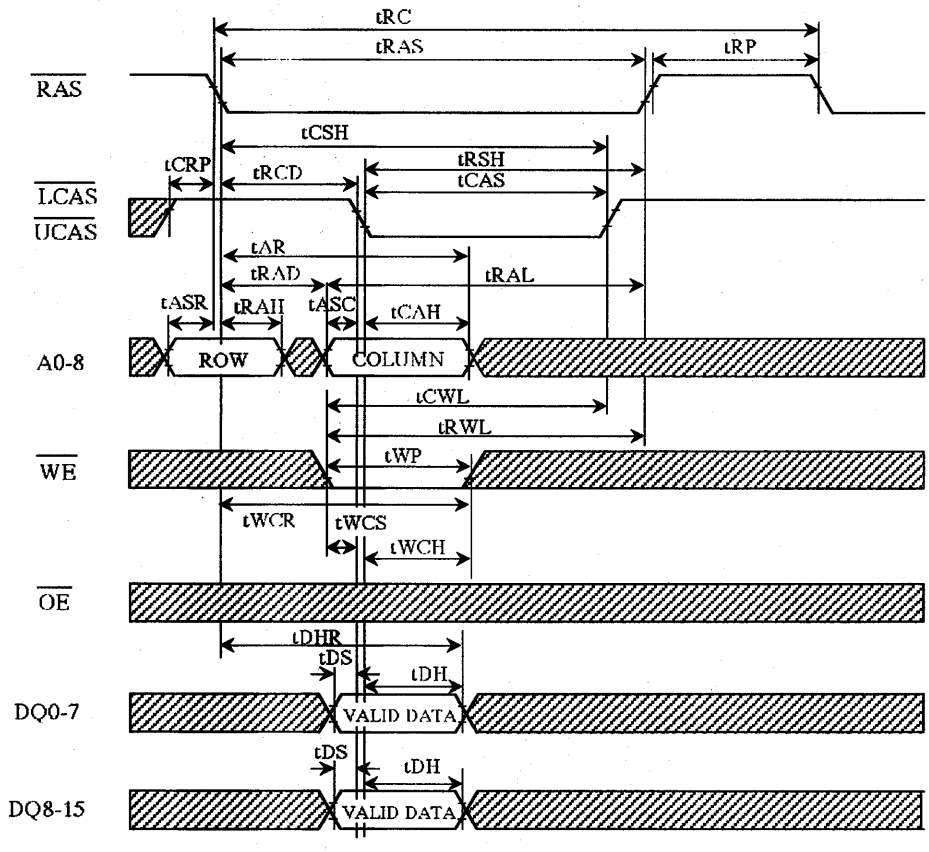
: "H" or "L"

READ CYCLE ($\overline{CAS}$ output control)



: "H" or "L"

EARLY WRITE CYCLE ($\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ active)



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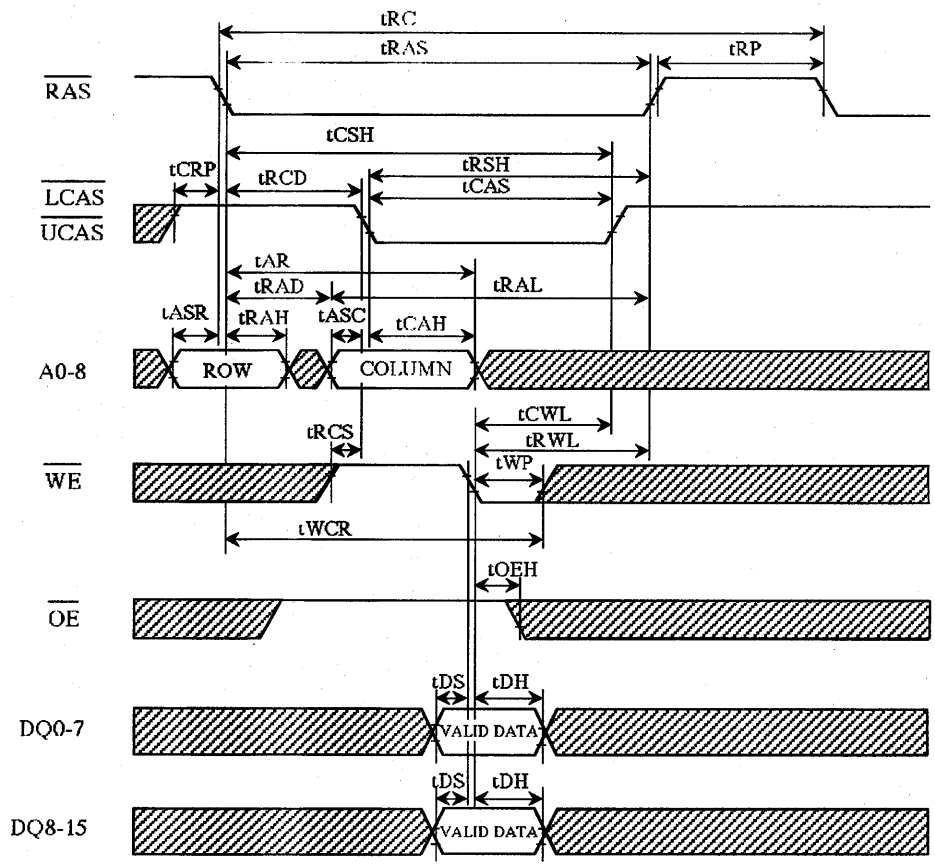
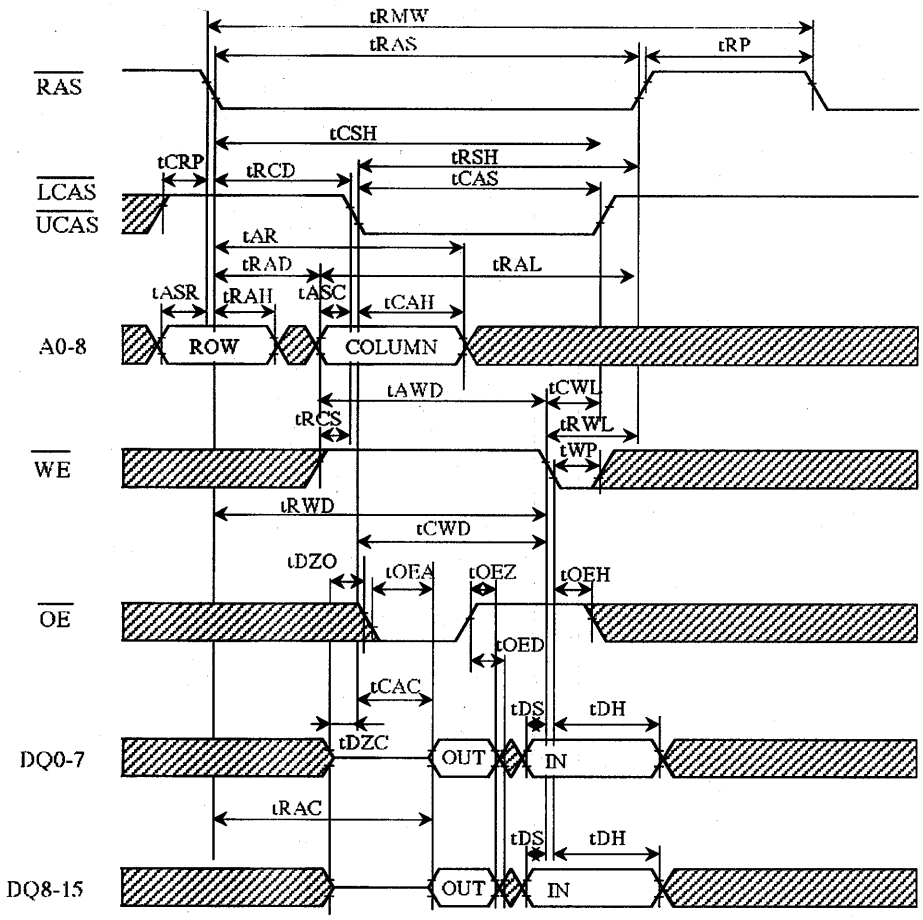
LATE WRITE CYCLE ($\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ active)



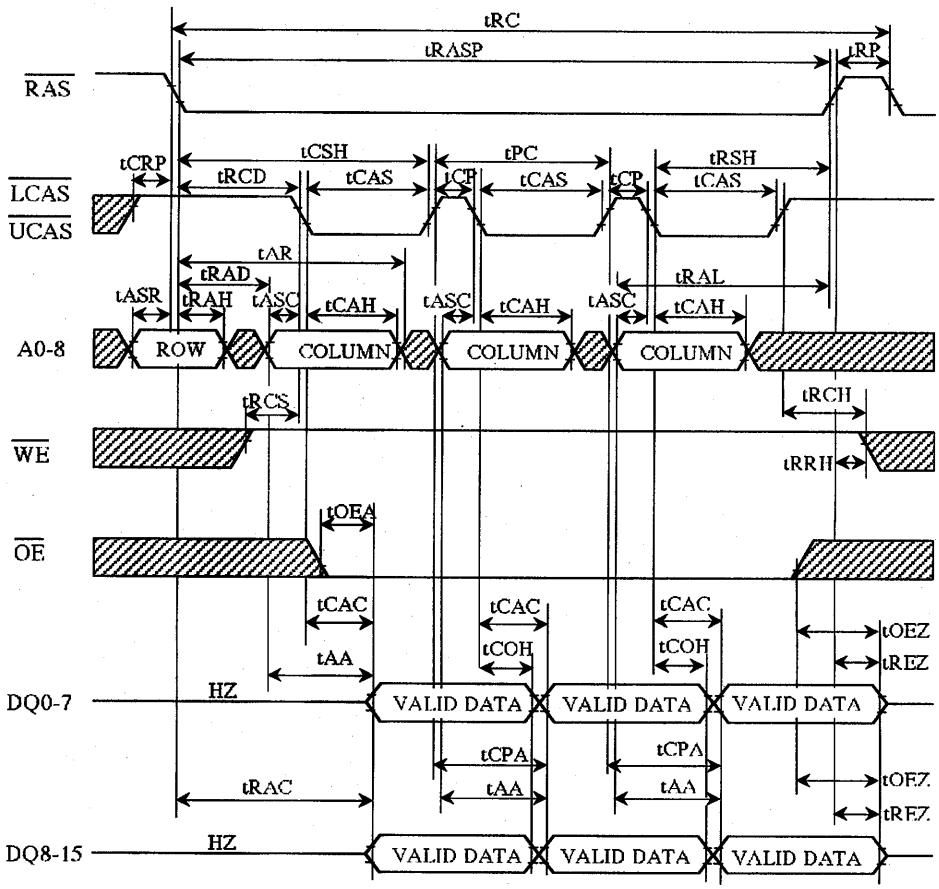
: "H" or "L"

READ MODIFY WRITE CYCLE ($\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ active)



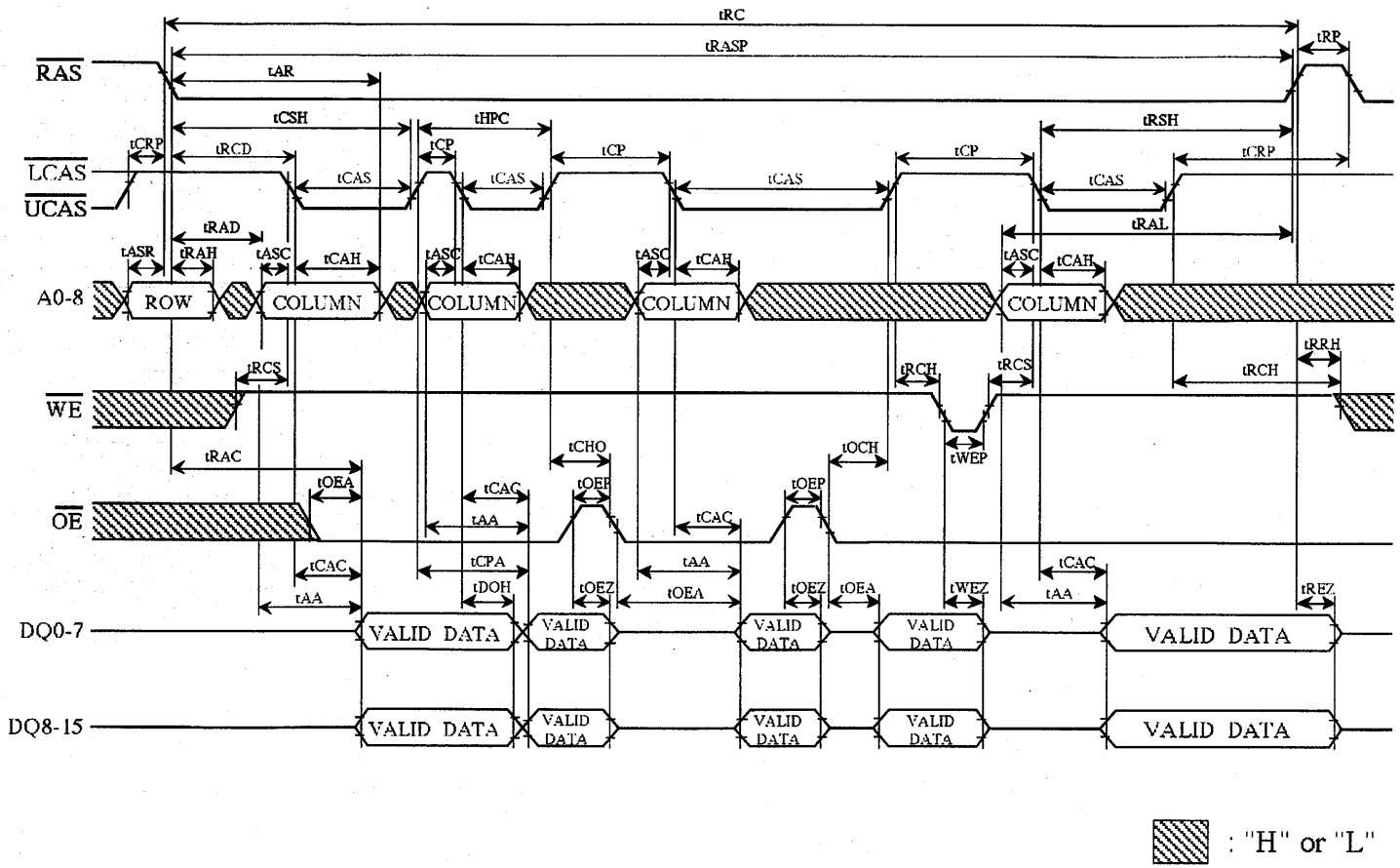
▨ : "H" or "L"

FAST PAGE MODE READ CYCLE with Extended Data Out

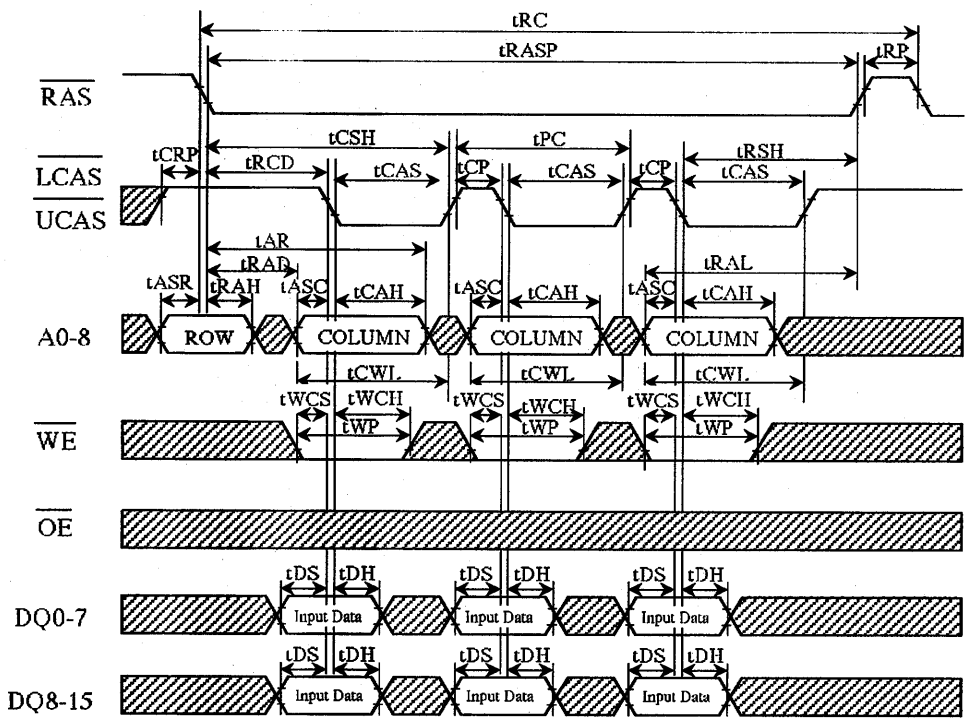


: "H" or "L"

FAST PAGE MODE READ Hi-Z OPERATION

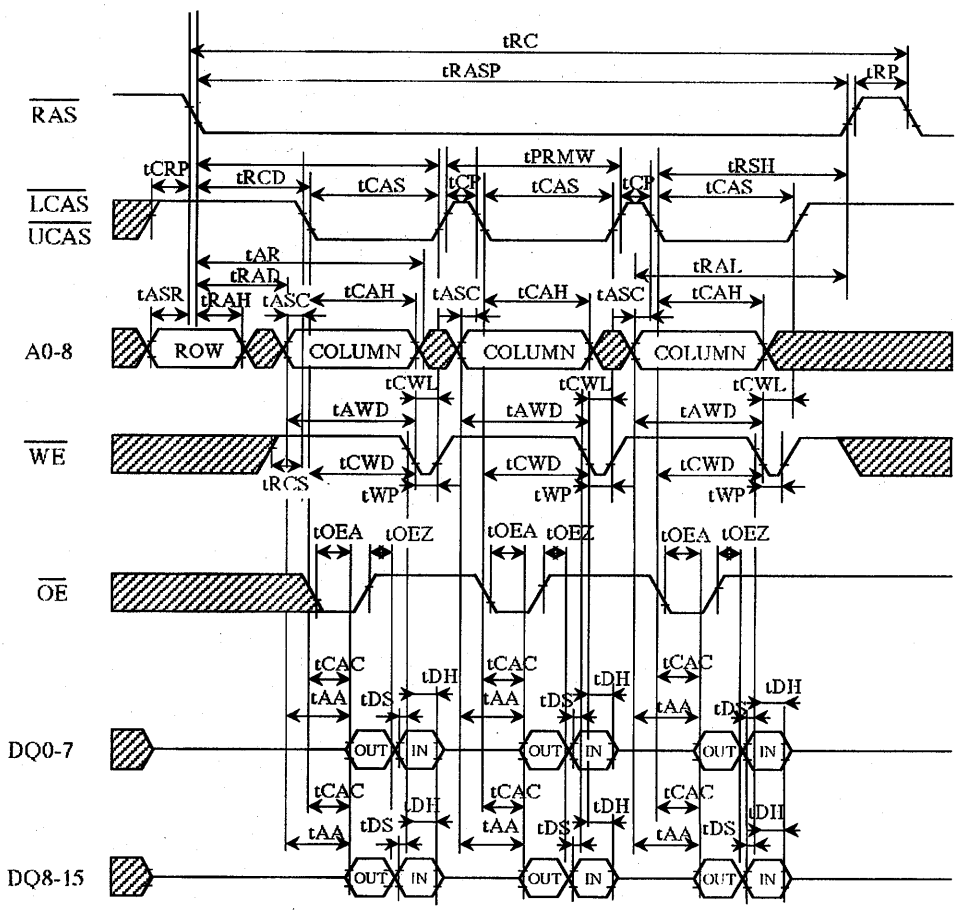


FAST PAGE MODE EARLY WRITE CYCLE



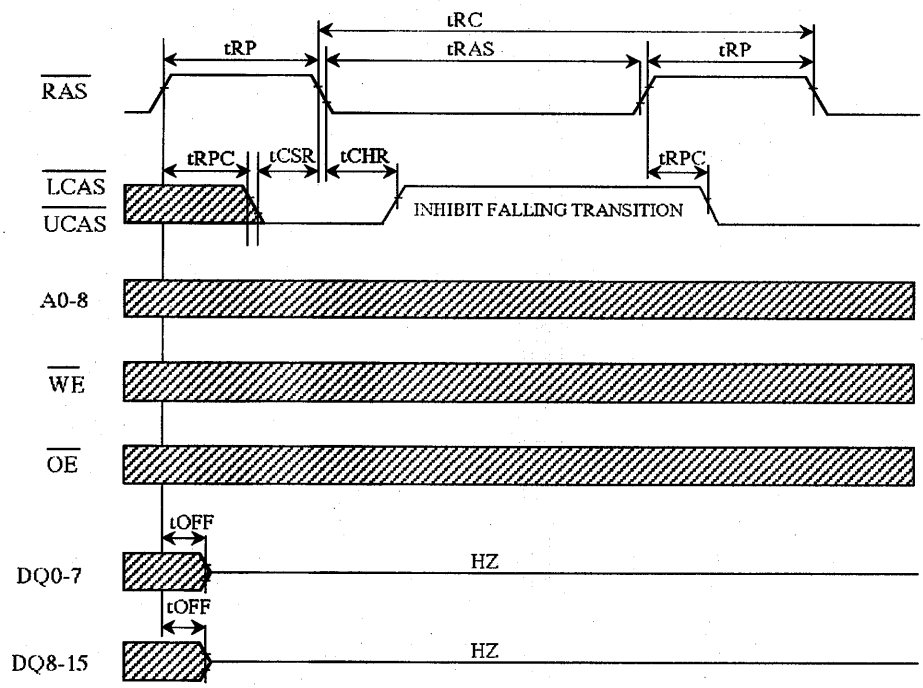
: "H" or "L"

FAST PAGE MODE READ MODIFY WRITE CYCLE



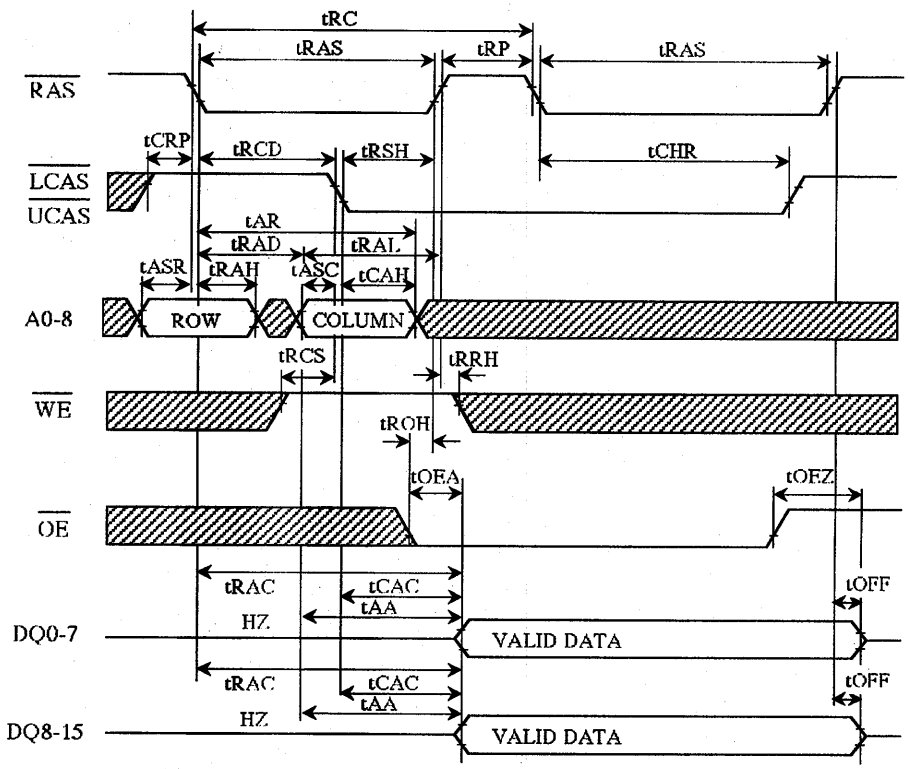
: "H" or "L"

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE



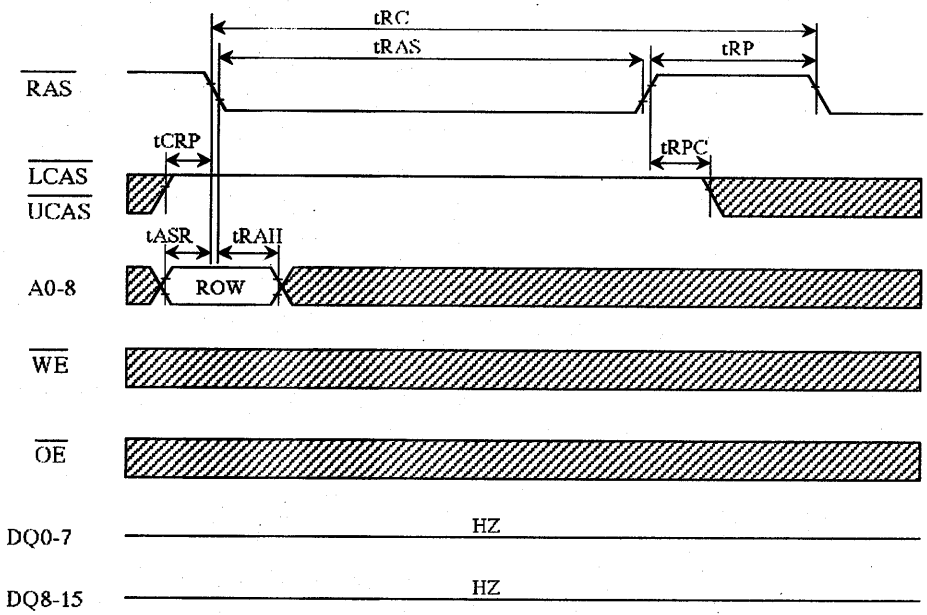
: "H" or "L"

HIDDEN REFRESH CYCLE



: "H" or "L"

$\overline{\text{RAS}}$ ONLY REFRESH CYCLE



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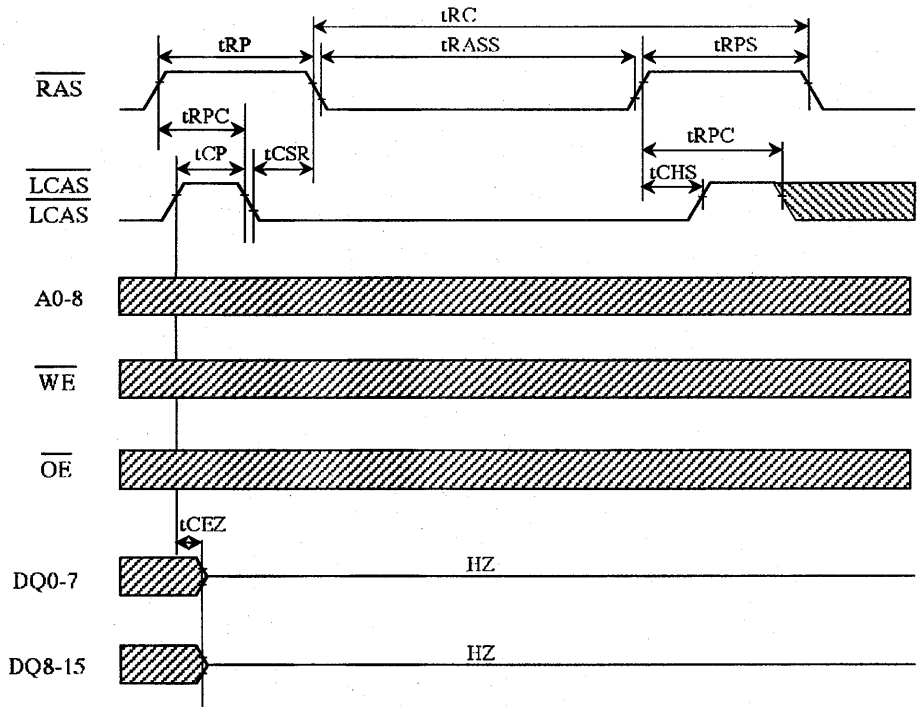
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ SELFREFRESH CYCLE



▨ : "H" or "L"

NOTE : SL version.