FEBL7029-01

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ML7029 Evaluation Board Manual

ADPCM CODEC

GENERAL DESCRIPTION

This Evaluation Board is intended to evaluate the LSI device (ML7029) which performs mutual transcoding between the analog voice band signal and ADPCM data. The Evaluation Board incorporates peripheral circuits necessary for operating the ML7029 and can easily evaluate performance and characteristics of the ML7029. Refer to the data sheet for detailed specifications and performance of the ML7029.

CONFIGURATION OF EVALUATION BOARD

- Evaluation Board PC board 1 pc.
- Power cord 1 pc.

EVALUATION BOARD CIRCUIT AND LAYOUT DIAGRAM

- Evaluation Board circuit diagram Figures 1 and 2
- Evaluation Board PC board mounting diagram Figure 3
- Evaluation data Figures 4 to 6

EVALUATION BOARD USING METHOD AND TERMINALS DESCRIPTION

- Power Supply
  Supply power to Evaluation Board using the supplied power cord.
  Red: 3 V, black: GND, brown: 5 V

- PDN Switch
  Power down control switch for the ML7029.
  0: Normal operation
  1: Power down

- AIN and AOUT
  These terminals (BCN connector and check pin) are connected to resistors and capacitors for easily providing analog interfaces with the ML7029.
  R1, R2, R3, R4: 600Ω termination resistors
  C1, C2, C3: Capacitors for DC separation (1 μF)
  R5, R6, R9, R10: Resistors (20 kΩ) for the operational amplifier (ANP1)
  R11, R12: Divider resistors (20 kΩ) for producing 2.5 V
  R7, R8: Resistors (default 0 dB: 20 kΩ) for adjusting the gain of the internal GSX amplifier of the ML7029
  Using these terminals allows this Evaluation Board to easily interface with evaluation instruments.

- BCLKI, SYNCI, DENI, EXCKI, DINI, and DOUTI
  The signals input to the terminals can be generated in the circuit in FPGA, and can also be provided by the user and these terminals can form interface. For this, insert a shunt pin into the left two pins of each of jumper pins J1, J2, J7, J8, J9, and J10. The Evaluation Board can also provide TTL interface since HC4050 is connected to each signal line.

- PCMSO and PCMSI, IS and IR, and PCMRO and PCMRI
  Each of jumper pins (J3, J4, J15) are used for connecting two terminals of each of the three pairs of the above terminals. By inserting jumper pins into the right two terminals, PCMSO and PCMSI, IS and IR, and PCMRO and PCMRI are connected, analog signals input to the ML7029 are encoded/decoded by APDCM and is output from the AOUT terminal. Moreover, PCM and ADPCM signals can be input/output individually to/from the above terminals.

- CLKSL1 and CLKSL0
  These switches are for selecting sampling frequencies for the ML7029.

CLKSL1	CLKSL0	SYNC (Sampling Frequency)	BCLK *1 (Shift Clock)	MCK (Master Clock)
0	0	8 kHz	64 kHz	10.368 MHz
0	1	16 kHz	128 kHz	20.736 MHz
1	0	11.025 kHz	88.2 kHz	14.2884 MHz

*1 When dip switches BMODE2, BMODE1 and BMODE0 are turned to OFF, ON, and ON respectively.

Note) 22.05 kHz is mentioned at CLKSL (1, 1) on the PC board, but be careful when using the sampling frequency because it has been found that in this Evaluation Board the SN ratio of the signal can deteriorate at this sampling frequency.

This Evaluation Board allows you to select 3 types of sampling frequencies, but by changing the crystal oscillator or directly inputting the clock from the MCK1 terminal, it is also possible to operate at an arbitrary sampling frequency other than the three types of frequencies. For example, in the case of 12 kHz sampling, this can be achieved by changing a 10.368 MHz oscillator to a 15.552 MHz oscillator. (MCK = 1269 * Fsample).

- Switches (R/W, A2 to A0, D7 to D0, and DATA-IN) for MCU Interface
  These switches can generate MCU interface signals for the ML7029. By setting the read/write switch to “0” (R/W = 0), addressing with the A2, A1, and A0 switches, placing data with the D7 to D0 switches and depressing the DATA-IN switch, you can set the control register of the ML7029. By setting the read/write switch to “1” (R/W = 1), addressing and depressing the DATA-IN switch, you can read (LED: B7 to B0) the contents of the control register.

- SW1 Dip Switches (BMODE2 to 0, RESET, and CLKON)
  Frequencies of BCLK can be changed with BMODE2 to 0. See the following table for details.

BMODE2 to 0	BCLK (When Sample = 8 kHz)	BCLK (When Sample = 16 kHz)	BCLK (When Sample = 11.025 kHz)
ON ON ON	3456 kHz	6912 kHz	4762.8 kHz
ON ON OFF	1152 kHz	2304 kHz	1587.6 kHz
ON OFF ON	384 kHz	768 kHz	529.2 kHz
ON OFF OFF	128 kHz	256 kHz	176.4 kHz
OFF ON ON	64 kHz	128 kHz	88.2 kHz
OFF ON OFF	32 kHz	64 kHz	44.1 kHz
OFF OFF ON	16 kHz	32 kHz	22.05 kHz
OFF OFF OFF	8 kHz	16 kHz	11.025 kHz

Normally use RESET in an ON state.
Normally use CLKON in an OFF state.

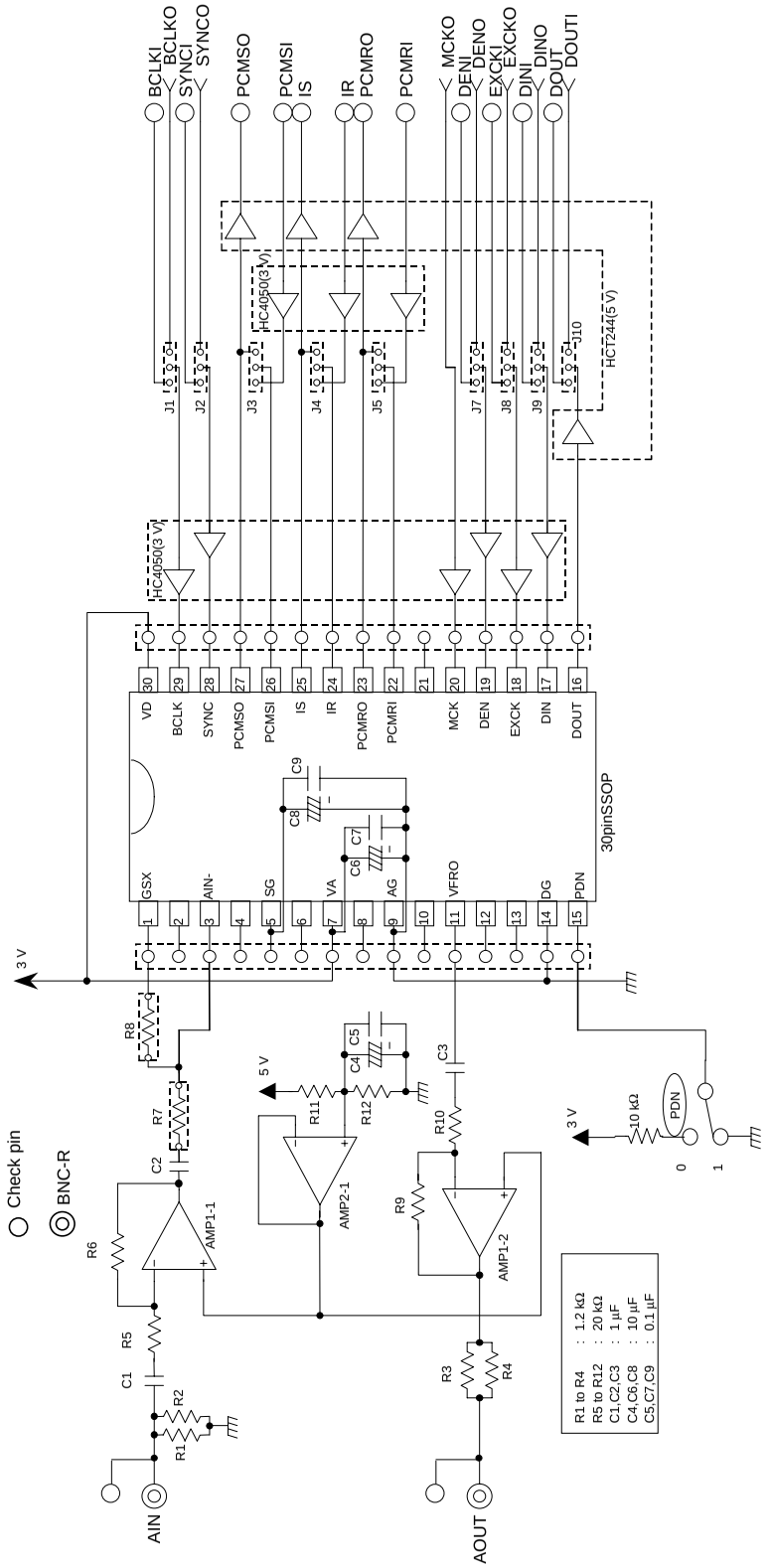

Figure 1 Evaluation Board circuit diagram No. 1

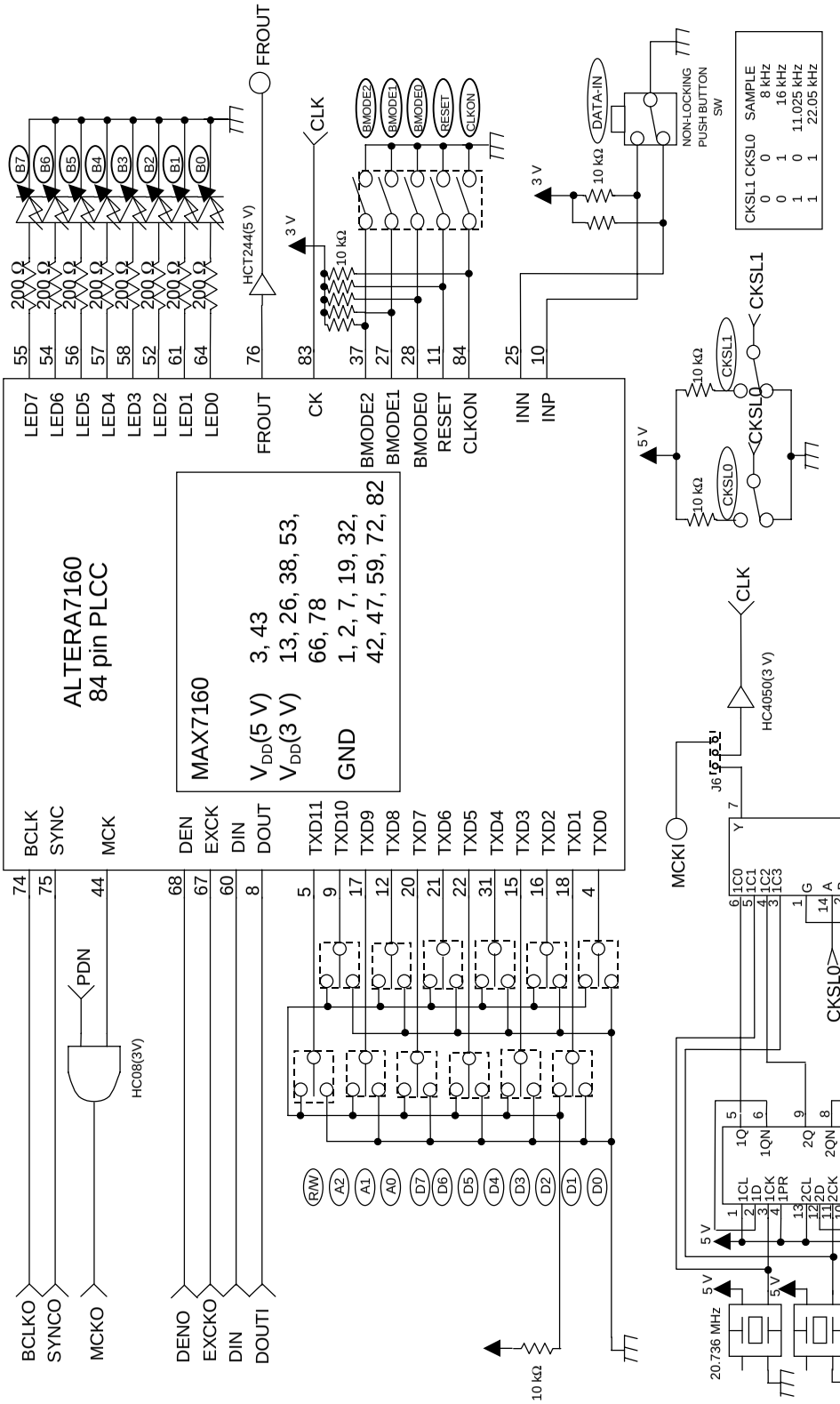

Figure 2 Evaluation Board circuit diagram No. 2

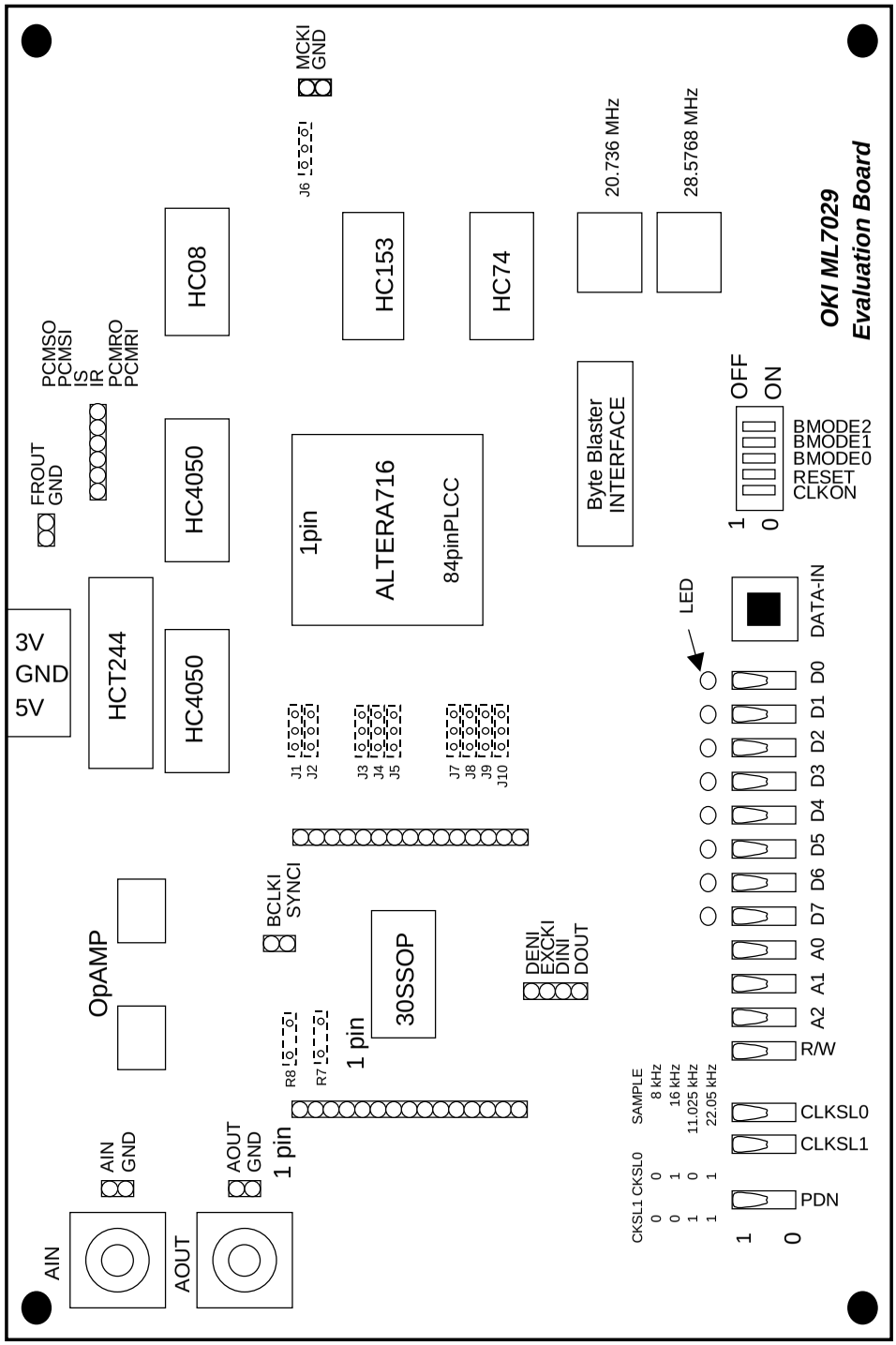

Figure 3 Evaluation Board PC board layout diagram

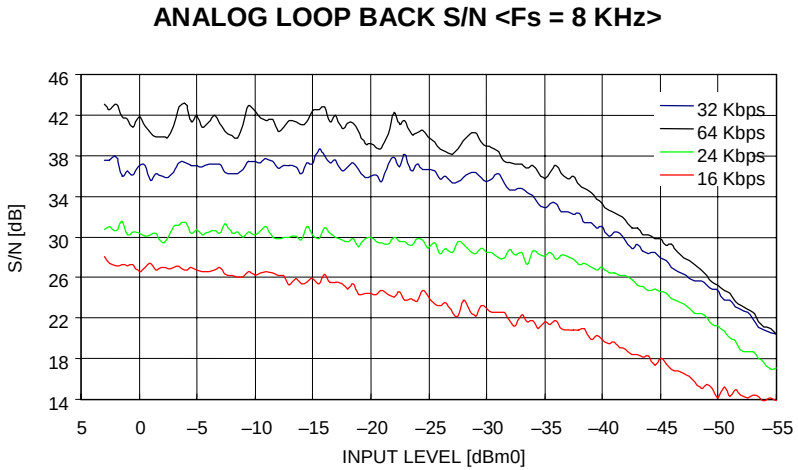

Figure 4 ANALOG LOOPBACK S/N characteristic (at 8 kHz sampling)

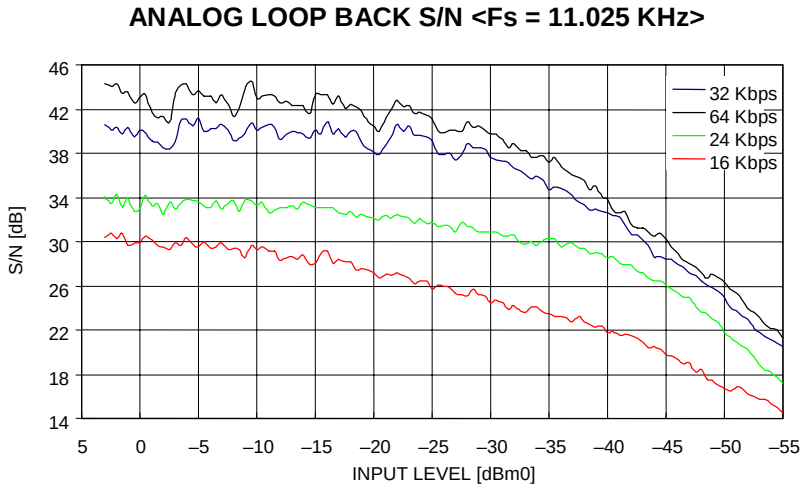

Figure 5 ANALOG LOOPBACK S/N characteristic (at 11.02 kHz sampling)

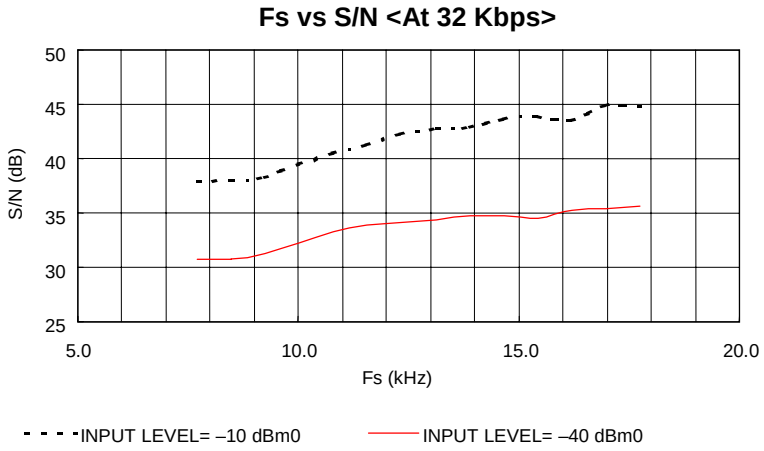

Figure 6 ANALOG LOOPBACK F8 vs. S/N characteristic (at 32 Kbps)

Measuring conditions:

Input frequency	1020 Hz
Voltage	3.0 V
Temperature	Room temperature

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