FEDL66517-02

OKI Semiconductor

This version: Oct. 2001
Previous version: Apr. 2001

ML66517 Family

16-Bit Microcontroller

GENERAL DESCRIPTION

The ML66517 family of highly functional CMOS 16-bit single chip microcontrollers utilizes the nX-8/500S, Oki's proprietary CPU core.

Each device includes capture input with an internal digital filter, 10-bit A/D converter, a number of timers, and dedicated 3-phase PWM (6 outputs) function capable of generating and controlling of AC/DC motor driving waveforms.

By means of the internal dedicated function for motor control, this general-purpose microcontroller is optimally suited for DC and AC motor control applications for energy saving. And the internal hardware multiplier allows high-speed arithmetic operations to be executed. And also the internal clock multiplication circuit can reduce the source frequency noise so that high-speed operations can be performed.

The flash ROM versions (ML66Q517) programmable with a single 5V power supply (4.5 to 5.5V) are also included in the family.

APPLICATIONS

Air conditioner or inverter control
Motor control for FA equipment

ORDERING INFORMATION

Order Code or Product Name	Package	Remark
ML66517-xxGA *1	80-pin plastic QFP (QFP 80-P-1420-0.80-BK)	5 V mask ROM version (4.5 to 5.5 V)
ML66Q517-NGA *2		ML66517 flash ROM version (4.5 to 5.5 V)

*1 : The “xx” of “-xx” stands for the code number.
*2 : The “N” of “-N” stands for the flash ROM, blank version.
When OKI programs and ship the flash ROM, the part number is changed from ”–N” to ”–XX” (code number) , for example, ML66Q517-999GA.

FEATURES

Name	ML66517
Operating temperature	–40°C to 85°C
Power supply voltage/ Maximum operating frequency	V_{DD} = 4.5 to 5.5 V/f = 25 MHz
Minimum instruction execution time	80 nsec @25 MHz
Internal ROM size (max. external)	64 KB (128 KB)
Internal RAM size (max. external)	2 KB (64 KB)
I/O ports	56 I/O pins (with pull-up resistors, programmable at the bit level)
	8 input pins
Timers	16-bit free running counter × 1ch
	Compare output/capture input × 2ch
	16-bit auto-reload timer (also functions as a event input/timer out) × 1ch
	8-bit auto reload timer × 4ch (can also be used as 16-bit auto reload timer × 1ch and 8-bit auto reload timer × 2ch)
	Capture input × 2ch
	8-bit auto reload timer × 2ch (also functions as serial communication baud rate generators)
	8-bit auto reload timer × 1ch (also functions as a watchdog timer)
	8-bit PWM × 4ch (can also be used as 16-bit PWM × 2ch)
Serial port	Synchronous/UART × 2ch
A/D converter	10-bit × 8ch
3-phase PWM (AC/DC motor control)	Available
External interrupt	Non-Maskable × 1ch
	Maskable × 4ch
Interrupt priority	3 levels
Others	External bus interface (Multiplexed address and data buses)
	Multiplication calculator
	Clock multiplication circuit (x2, x4)
Flash ROM version	ML66Q517

SPECIAL FEATURES

1. High-performance CPU
The family includes the high-performance CPU, powerful bit manipulation instruction set, full symmetrical addressing mode, and ROM WINDOW function, and also provides the best optimized C compiler support.

2. 3-phase PWM circuit for generating motor drive waveforms
The device includes a 16-bit three-phase PWM (six outputs) circuit designed specifically for generating AC three-phase motor or DC three-phase brushless motor drive waveforms. PWM and level outputs can be switched by compare and match circuitry and software, and the compare and match circuitry can switch the outputs in real time.
The device has circuitry to fix the three-phase outputs at an inactive level by inputting malfunction signals from a motor at the specific pin.

3. Capture inputs with digital filters
The device has two channels of capture inputs with 3/4 digital filters. The device is best suited to event interval measurement, pulse width measurement, etc. in a high noise environment such as motor control. An optimum filter can be selected according to noise width since a sampling interval of an input signal can be selected. A digital filter OFF mode can also be selected.

4. High-speed multiplier
The device includes a dedicated high-speed multiplier.
The calculation time, 16 bits × 16 bits = 32 bits, is 200 ns (f = 25 MHz).

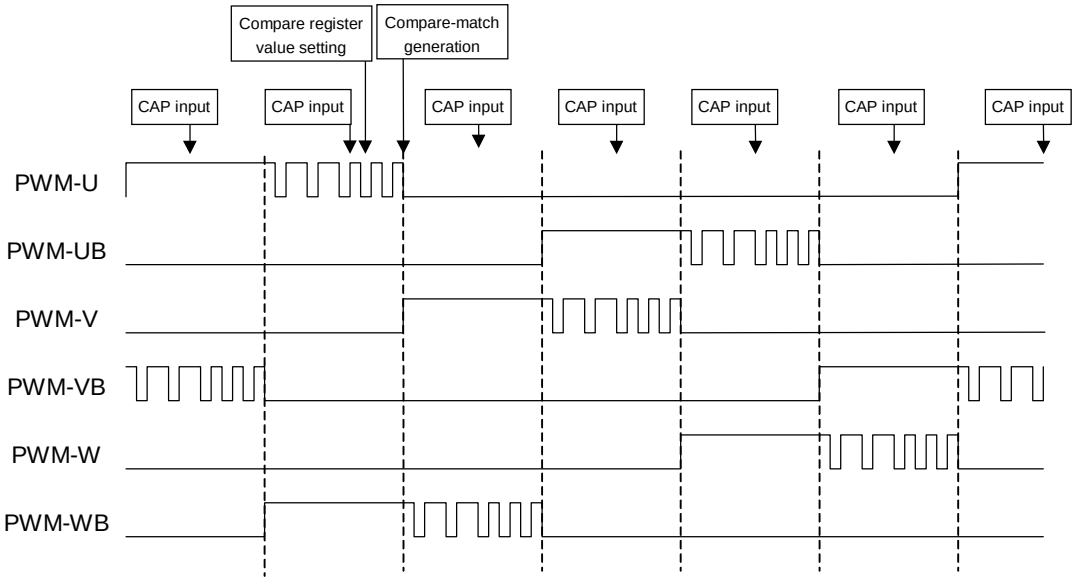
5. Clock multiplication circuit
The device includes a clock multiplication circuit in which the clock can be selected as a source clock (PLL OFF), 2 × clock, or 4 × clock.
Therefore, the use of a low frequency oscillator (external clock) allows the device to internally operate at a high speed, which achieves noise reduction and lower power consumption.

6. Flash memory version programmable with a single power supply
In addition to the mask ROM versions, the family includes the versions (ML66Q517) with 64 KB flash memory that can be programmed with a single 5 V supply (4.5 to 5.5 V).

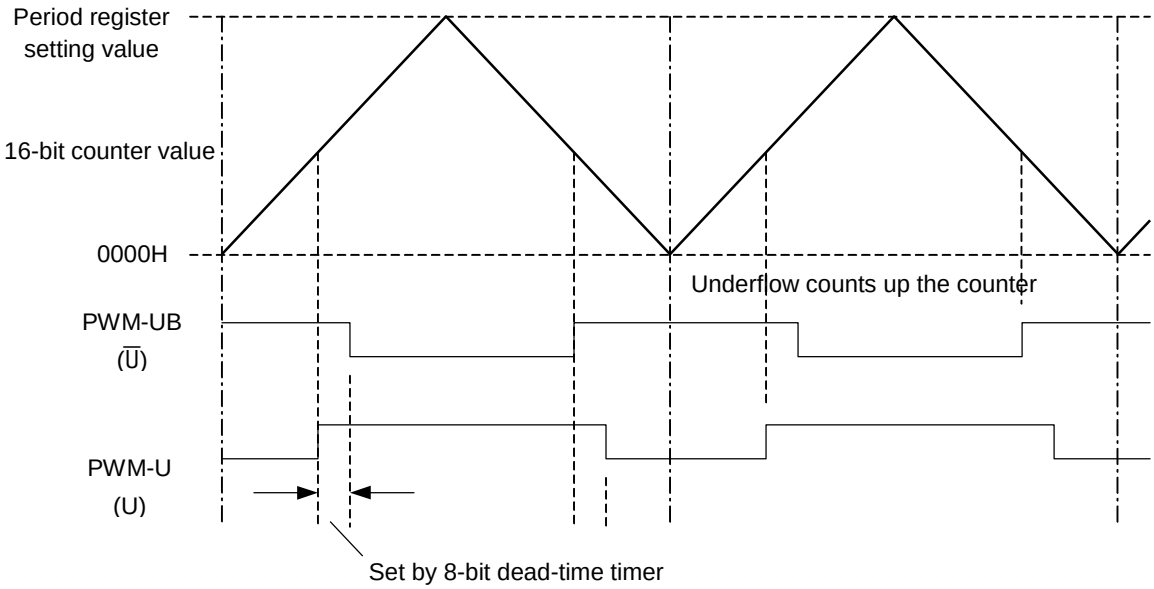
7. A high-precision A/D converter
The device has a high precision 10-bit A/D converter with eight channels.
An independent result register for each channel provides easy accessibility by software.
The A/D converter is activated in a channel select mode, and automatic conversion is also implemented in a scan mode which scans from any designated channel to the last channel (ch 7).

8. Programmable pull-up resistors
Building the pull-up resistors into the chip contributes to overall design compactness. Making them programmable on a per-bit basis allows complete flexibility in circuit board layout and system design. These programmable pull-up resistors are available for all I/O pins not already assigned specific functions (such as the oscillator connection pins).

PWM output switching every 60° of motor turn using the compare-out timer



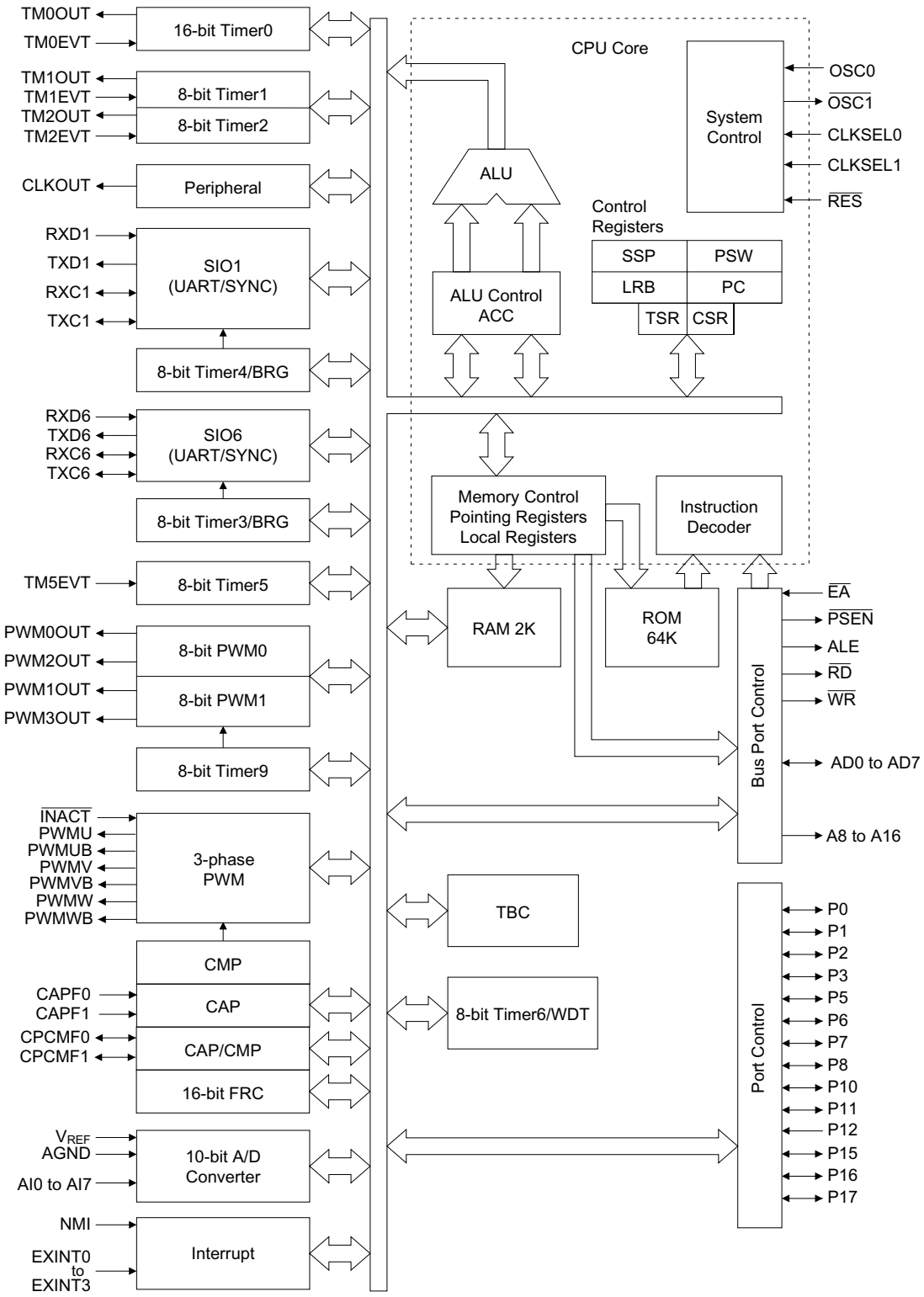
PWM Output Timing (DC Motor Control)



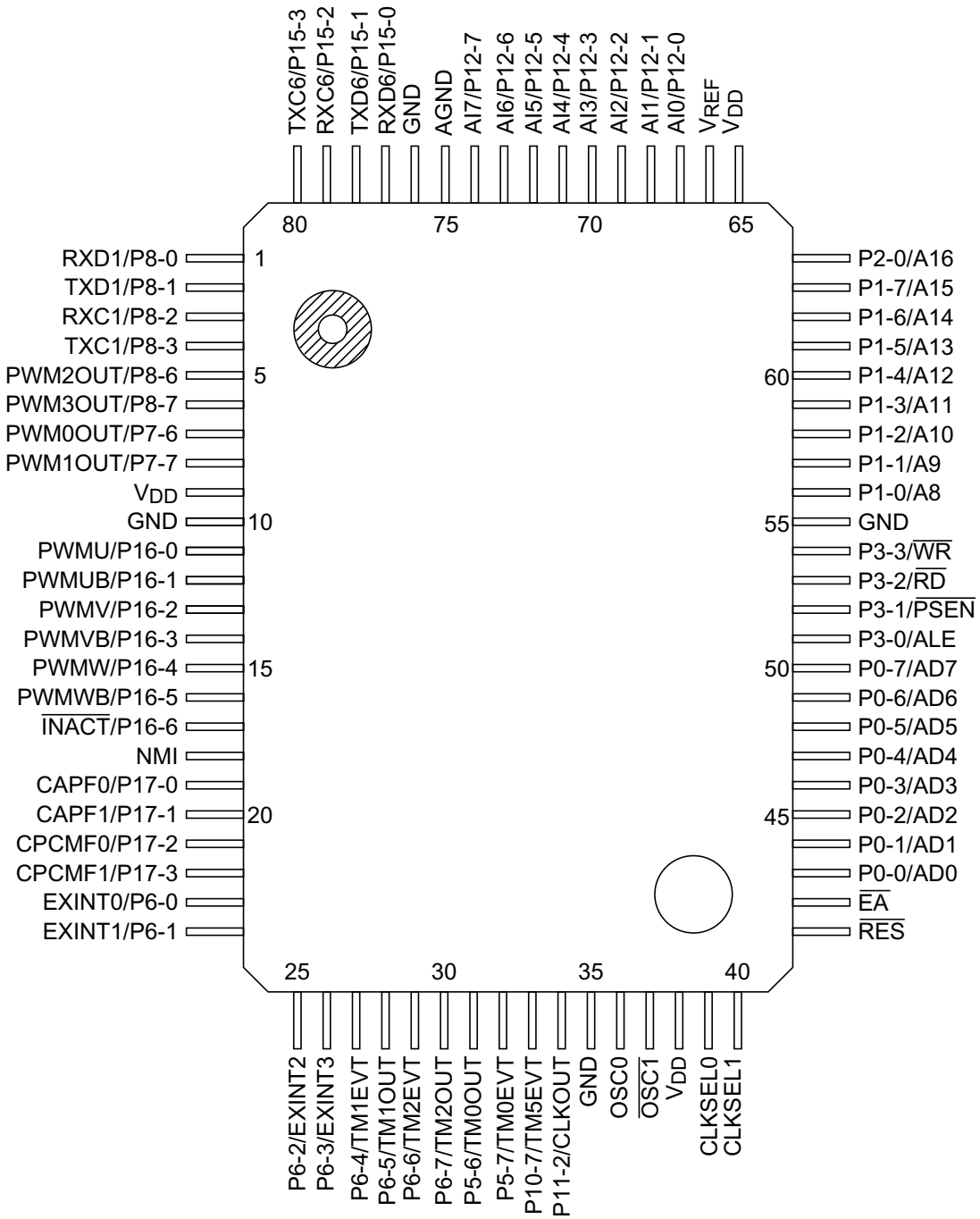
(Only U and U̅ output signals are indicated above)

PWM Output Timing (AC Motor Control)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



80-Pin Plastic QFP

PIN DESCRIPTIONS

In the Type column, "I" indicates an input pin, "O" indicates an output pin, and "I/O" indicates an I/O pin.

Function	Symbol	Description			
		Primary function		Secondary function	
		Type		Type	
Port	P0_0/AD0 to P0_7/AD7	I/O	8-bit I/O port Pull-up resistors can be specified for each bit.	I/O	External memory access Address output/data I/O port
	P1_0/A8 to P1_7/A15	I/O	8-bit I/O port Pull-up resistors can be specified for each bit.	O	External memory access Address output port
	P2_0/A16	I/O	1-bit I/O port Pull-up resistors can be specified.	O	External memory access Address output port
	P3_0/ALE	I/O	4-bit I/O port 10 mA sink capability Pull-up resistors can be specified for each bit.	O	External memory access Address latch enable signal output pin
	P3_1/$\overline{\text{PSEN}}$			O	External program memory access Read strobe output pin
	P3_2/$\overline{\text{RD}}$			O	External data memory access Read strobe output pin
	P3_3/$\overline{\text{WR}}$			O	External data memory access Write strobe output pin
	P5_6/TM0OUT	I/O	2-bit I/O port Pull-up resistors can be specified for each bit.	O	Timer 0 timer output pin
	P5_7/TM0EVT			I	Timer 0 external event input pin
	P6_0/EXINT0	I/O	8-bit I/O port Pull-up resistors can be specified for each bit.	I	External interrupt 0 input pin
	P6_1/EXINT1			I	External interrupt 1 input pin
	P6_2/EXINT2			I	External interrupt 2 input pin
	P6_3/EXINT3			I	External interrupt 3 input pin
	P6_4/TM1EVT			I	Timer 1 external event input pin
	P6_5/TM1OUT			O	Timer 1 timer output pin
	P6_6/TM2EVT			I	Timer 2 external event input pin
	P6_7/TM2OUT			O	Timer 2 timer output pin
	P7_6/PWM0OUT	I/O	2-bit I/O port Pull-up resistors can be specified for each bit.	O	PWM0 output pin
	P7_7/PWM1OUT			O	PWM1 output pin

Function	Symbol	Description			
		Primary function		Secondary function	
		Type		Type	
Port	P8_0/RXD1	I/O	6-bit I/O port Pull-up resistors can be specified for each bit.	I	SIO1 receive data input pin
	P8_1/TXD1			O	SIO1 transmit data output pin
	P8_2/RXC1			I/O	SIO1 receive clock I/O pin
	P8_3/TXC1			I/O	SIO1 transmit clock I/O pin
	P8_6/PWM2OUT			O	PWM2 output pin
	P8_7PWM3OUT			O	PWM3 output pin
	P10_7/TM5EVT	I/O	1-bit I/O port Pull-up resistors can be specified.	I	Timer 5 external event input pin
	P11_2/CLKOUT	I/O	1-bit I/O port Pull-up resistors can be specified.	O	Main clock pulse output pin
	P12_0/AI0 to P12_7/AI7	I	8-bit input port	I	A/D converter analog input port
	P15_0/RXD6	I/O	4-bit I/O port Pull-up resistors can be specified for each bit.	I	SIO6 receive data input pin
	P15_1/TXD6			O	SIO6 transmit data output pin
	P15_2/RXC6			I/O	SIO6 receive clock I/O pin
	P15_3/TXC6			I/O	SIO6 transmit clock I/O pin
	P16_0/PWMU	I/O	7-bit I/O port Pull-up resistors can be specified for each bit.	O	3-phase PWMU output pin
	P16_1/PWMUB			O	3-phase PWMUB output pin
	P16_2/PWMV			O	3-phase PWMV output pin
	P16_3/PWMVB			O	3-phase PWMVB output pin
	P16_4/PWMW			O	3-phase PWMW output pin
	P16_5/PWMWB			O	3-phase PWMWB output pin
	P16_6/$\overline{\text{INACT}}$			I	Abnormality detect input pin
	P17_0/CAPF0	I/O	4-bit I/O port Pull-up resistors can be specified for each bit.	I	Capture 0 input pin
	P17_1/CAPF1			I	Capture 1 input pin
	P17_2/CPCMF0			I/O	Capture 0 input/compare 0 output pin
	P17_3/CPCMF1			I/O	Capture 1 input/compare 1 output pin

Function	Symbol	Type	Description
Power supply	V_{DD}	I	Power supply pin Connect all V_{DD} pins to the power supply.*
	GND	I	GND pin Connect all GND pins to GND.*
	V_{REF}	I	Analog reference voltage pin (Connect to the V_{DD} pin when A/D converter is not used.)
	AGND	I	Analog GND pin (Connect to the GND pin when A/D converter is not used.)
Oscillation	OSC0	I	Main clock oscillation input pin Connect to a crystal or ceramic oscillator. Or, input an external clock.
	$\overline{OSC1}$	O	Main clock oscillation output pin Connect to a crystal or ceramic oscillator. The clock output is opposite in phase to OSC0. Leave this pin unconnected when an external clock is used.
	CLKSEL0	I	Clock multiplication factor select pin Clock multiplication factor is selected from source oscillation (PLL OFF), source oscillation × 2, or source oscillation × 4
	CLKSEL1	I	
Reset	$\overline{RES}$	I	Reset input pin
Others	NMI	I	Non-maskable interrupt input pin
	$\overline{EA}$	I	External program memory access input pin If the $\overline{EA}$ pin is enabled (low level), the internal program memory is masked and the CPU executes the program code in external program memory all address space.

* Each of the family devices has unique pattern routes for the internal power and ground. Connect the power supply voltage to all V_{DD} pins and the ground potential to all GND pins. If a device may have one or more V_{DD} or GND pins to which the power supply voltage or the ground potential is not connected, it can not be guaranteed for normal operation.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition		Rating	Unit
Digital power supply voltage	V_{DD}	GND = AGND = 0 V Ta = 25°C		–0.3 to +7.0	V
Input voltage	V_I			–0.3 to V_{DD} +0.3	V
Output voltage	V_O			–0.3 to V_{DD} +0.3	V
Analog reference voltage	V_{REF}			–0.3 to V_{DD} +0.3	V
Analog input voltage	V_{AI}			–0.3 to V_{REF}	V
Power dissipation	P_D	Ta = 85°C per package	80-pin QFP	600	mW
Storage temperature	T_{STG}	—		–50 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition		Rating	Unit
Digital power supply voltage	V_{DD}	$f_{OSC} \leq 25$ MHz		4.5 to 5.5	V
Analog reference voltage	V_{REF}	—		V_{DD} – 0.3 to V_{DD}	V
Analog input voltage	V_{AI}	—		AGND to V_{REF}	V
Memory hold voltage	V_{DDH}	f_{OSC} = 0 Hz		2.0 to 5.5	V
Internal operating frequency	f_{OSC}	PLL (multiplier) OFF		2 to 25	MHz
		PLL (multiplier) ON		20 to 25	
Ambient temperature	Ta	—		–40 to +85	°C
Fan out	N	MOS load		20	—
		TTL load	P3	6	—
			P0, P16	2	
			P1, P2, P5 to P8, P10, P11, P15, P17	1	

INTERNAL FLASH ROM PROGRAMMING CONDITIONS

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}	—	4.5 to 5.5	V
Ambient temperature	Ta	During Read	–40 to +85	°C
		During Programming	+0 to +50	
Endurance	CEP	—	100	Cycles
Blocks size	—	—	128	bytes

ALLOWABLE OUTPUT CURRENT

(V_{DD} = 4.5 to 5.5 V, Ta = –40 to +85°C)

Parameter	Pin	Symbol	Min.	Typ.	Max.	Unit
"H" output pin (1 pin)	All output pins	I_{OH}	—	—	–2	mA
"H" output pins (sum total)	Sum total of all output pins	Σ_{IOH}	—	—	–50	
"L" output pin (1 pin)	P3	I_{OL}	—	—	10	
	Other ports		—	—	5	
"L" output pins (sum total)	Sum total of P0, P3	Σ_{IOL}	—	—	60	
	Sum total of P1, P2				50	
	Sum total of P7, P8, P15					
	Sum total of P5, P6, P10, P11, P16, P17					
	Sum total of all output pins				100	

Note: Each of the family devices has unique pattern routes for the internal power and ground. Connect the power supply voltage to all V_{DD} pins and the ground potential to all GND pins. If a device may have one or more V_{DD} or GND pins to which the power supply voltage or the ground potential is not connected, it can not be guaranteed for normal operation.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 4.5 to 5.5 V, Ta = –40 to +80°C)

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	*1	V_{IH}	—	0.44 V_{DD}	—	V_{DD} + 0.3	V
"H" input voltage	*2 to *8			0.80 V_{DD}	—	V_{DD} + 0.3	
"L" input voltage	*1	V_{IL}	—	–0.3	—	0.16 V_{DD}	
"L" input voltage	*2 to *8			–0.3	—	0.2 V_{DD}	
"H" output voltage	*1, *4, *5	V_{OH}	I_O = –400 µA	V_{DD} – 0.4		—	
			I_O = –2.0 mA	V_{DD} – 0.6	—	—	
"H" output voltage	*2		I_O = –200 µA	V_{DD} – 0.4	—	—	
			I_O = –2.0 mA	V_{DD} – 0.6	—	—	
"L" output voltage	*1, *5	V_{OL}	I_O = 3.2 mA	—	—	0.4	
			I_O = 5.0 mA	—	—	0.8	
"L" output voltage	*4		I_O = 3.2 mA	—	—	0.4	
			I_O = 10.0 mA	—	—	1.0	
"L" output voltage	*2		I_O = 1.6 mA	—	—	0.4	
			I_O = 5.0 mA	—	—	0.8	
Input leakage current	*3, *7	I_{IH}/I_{IL}	V_I =V_{DD}/0 V	—	—	1/–1	µA
Input current	*6			—	—	1/–250	
Input current	*8			—	—	15/–15	
Output leakage current	*1, *2, *4, *5	I_{LO}	V_O =V_{DD}/0 V	—	—	± 10	µA
Pull-up resistance		R_{pull}	V_I = 0 V	25	50	100	kΩ
Input capacitance		C_I	f = 1 MHz, Ta = 25°C	—	5	—	pF
Output capacitance		C_O		—	7	—	
Analog reference supply current		I_{REF}	During A/D operation	—	—	4	mA
			When A/D is stopped	—	—	10	µA

*1: Applicable to P0
*2: Applicable to P1, P2, P6, P7, P8, P10, P11, P15, P17
*3: Applicable to P12
*4: Applicable to P3
*5: Applicable to P16
*6: Applicable to $\overline{RES}$
*7: Applicable to $\overline{EA}$, NMI, CLKSEL0, CLKSEL1
*8: Applicable to OSC0

Supply current

Mode	Symbol	Condition	Min.	Typ.	Max.	Unit
CPU operation mode *1	I_{DD}	f=25 MHz	—	40	60	mA
HALT mode *2	I_{DDH}	f=25 MHz	—	30	40	mA
STOP mode *3	I_{DDS}	ML66Q517	—	20	900	µA
		ML66517	—	1	50	

[Note] Ports used as inputs are at V_{DD} or 0 V. Other ports are unloaded.
*1. CPU and all the peripheral functions (timer, PWM, A/D, etc.) are activated.
*2. CPU is stopped, and all the peripheral functions (timer, PWM, A/D, etc.) are activated.
*3. CPU and all the peripheral functions are deactivated.

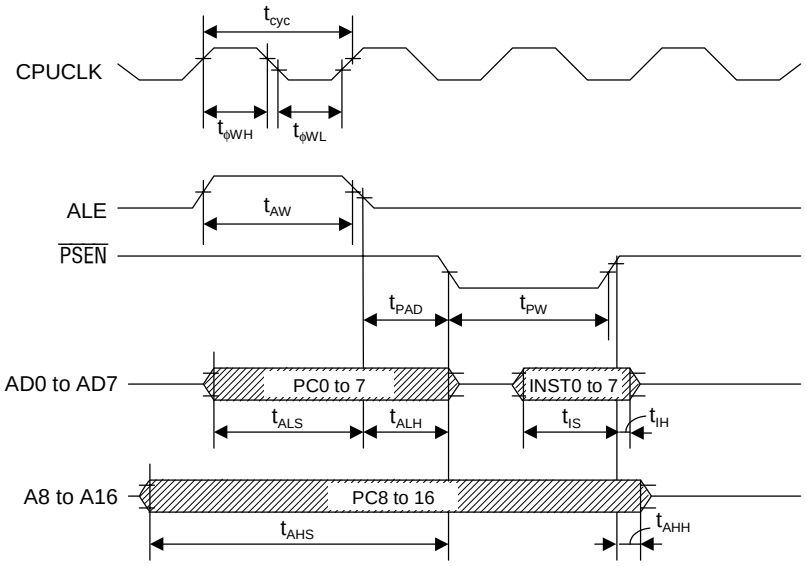
AC Characteristics

(1) External program memory control

(V_{DD} = 4.5 to 5.5 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 25 MHz	40	—	ns
Clock pulse width (HIGH level)	$t_{\phi WH}$	C_L = 50 pF	13	—	
Clock pulse width (LOW level)	$t_{\phi WL}$		13	—	
ALE pulse width	t_{AW}		2tϕ – 10	—	
$\overline{PSEN}$ pulse width	t_{PW}		2tϕ – 18	—	
$\overline{PSEN}$ pulse delay time	t_{PAD}		tϕ – 5	—	
Low address setup time	t_{ALS}		2tϕ – 15	—	
Low address hold time	t_{ALH}		tϕ – 13	—	
High address setup time	t_{AHS}		3tϕ – 30	—	
High address hold time	t_{AHH}		–8	—	
Instruction setup time	t_{IS}		30	—	
Instruction hold time	t_{IH}		–8	tϕ – 3	

Note: tϕ = t_{cyc}/2



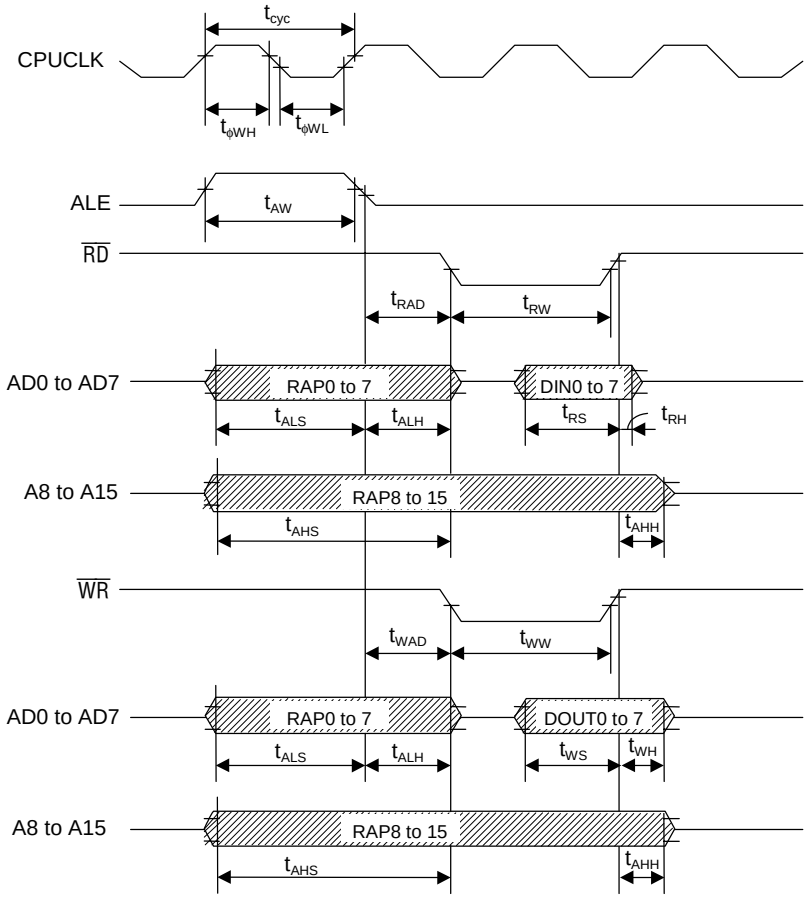
Bus timing during no wait cycle time

(2) External data memory control

(V_{DD} = 4.5 to 5.5 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 25 MHz	40	—	ns
Clock pulse width (HIGH level)	$t_{\phi WH}$	C_L = 50 pF	13	—	
Clock pulse width (LOW level)	$t_{\phi WL}$		13	—	
ALE pulse width	t_{AW}		2tϕ – 10	—	
$\overline{RD}$ pulse width	t_{RW}		2tϕ – 18	—	
$\overline{WR}$ pulse width	t_{WW}		2tϕ – 18	—	
$\overline{RD}$ pulse delay time	t_{RAD}		tϕ – 5	—	
$\overline{WR}$ pulse delay time	t_{WAD}		tϕ – 5	—	
Low address setup time	t_{ALS}		2tϕ – 15	—	
Low address hold time	t_{ALH}		tϕ – 13	—	
High address setup time	t_{AHS}		3tϕ – 30	—	
High address hold time	t_{AHH}		tϕ – 3	—	
Read data setup time	t_{RS}		30	—	
Read data hold time	t_{RH}		0	tϕ – 3	
Write data setup time	t_{WS}		2tϕ – 30	—	
Write data hold time	t_{WH}		tϕ – 3	—	

Note: tϕ = t_{cyc}/2



Bus timing during no wait cycle time

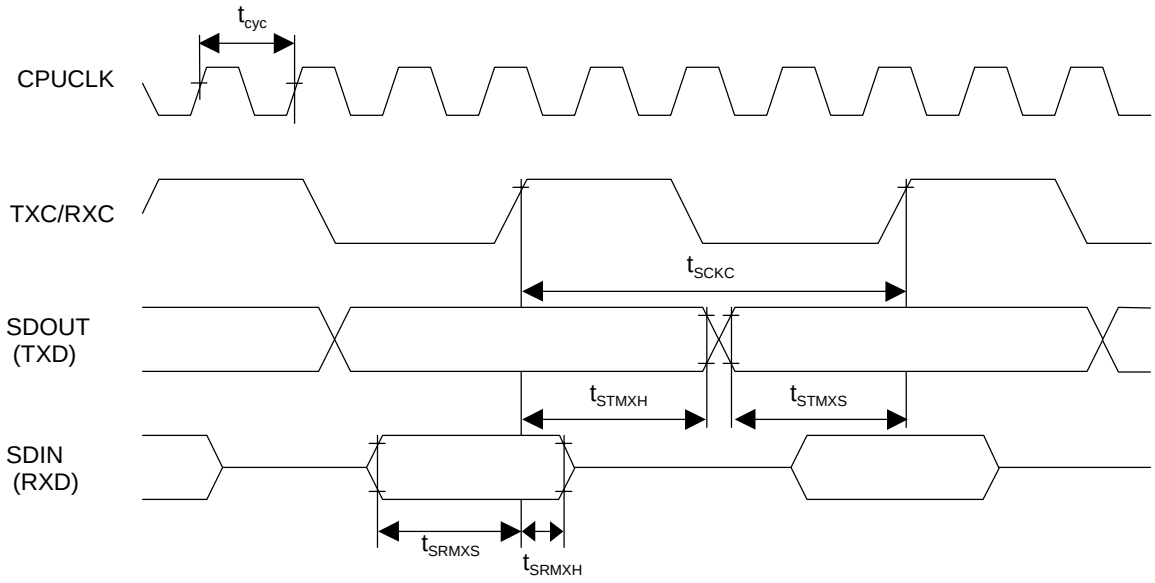
(3) Serial port control

Master mode (Clock synchronous serial port)

(V_{DD} = 4.5 to 5.5 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 25 MHz	40	—	ns
Serial clock cycle time	t_{SCKC}	C_L = 50 pF	4 t_{cyc}	—	
Output data setup time	t_{STMXS}		2tϕ – 5	—	
Output data hold time	t_{STMXH}		5tϕ – 10	—	
Input data setup time	t_{SRMXS}		13	—	
Input data hold time	t_{SRMXH}		0	—	

Note: tϕ = t_{cyc}/2

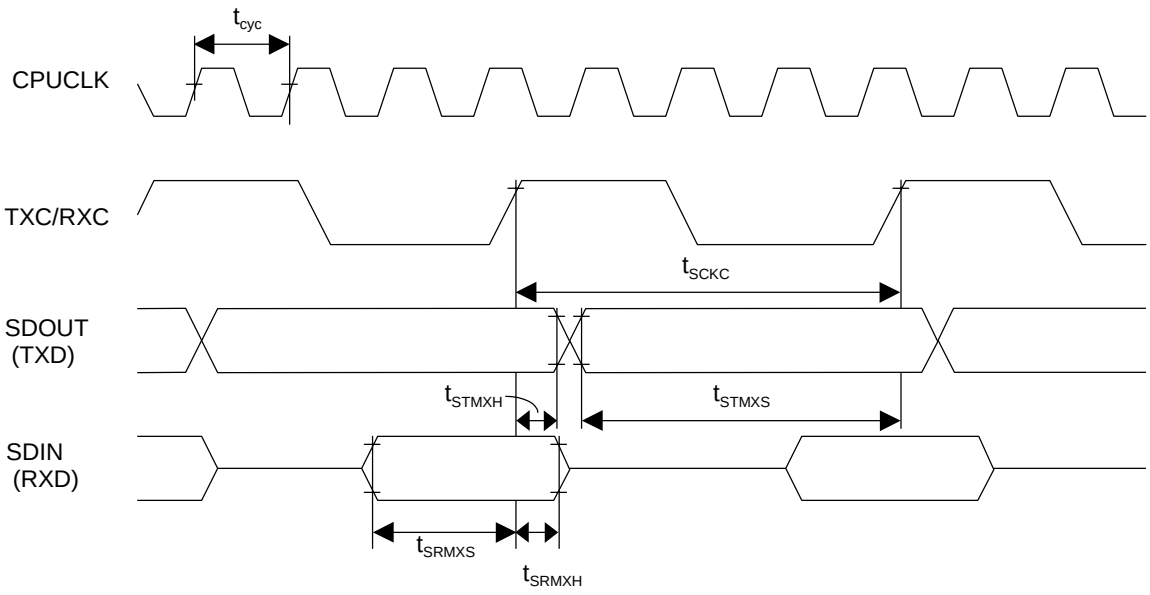


Slave mode (Clock synchronous serial port)

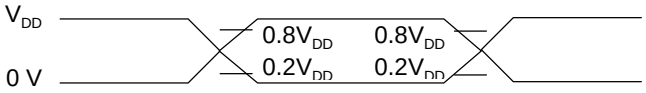
(V_{DD} = 4.5 to 5.5 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 25 MHz	40	—	ns
Serial clock cycle time	t_{SCKC}	C_L = 50 pF	4 t_{cyc}	—	
Output data setup time	t_{STMXS}		2tϕ – 15	—	
Output data hold time	t_{STMXH}		4tϕ – 10	—	
Input data setup time	t_{SRMXS}		13	—	
Input data hold time	t_{SRMXH}		3	—	

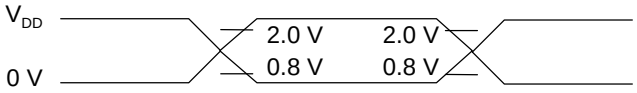
Note: tϕ = t_{cyc}/2



Measurement points for AC timing (the serial port)



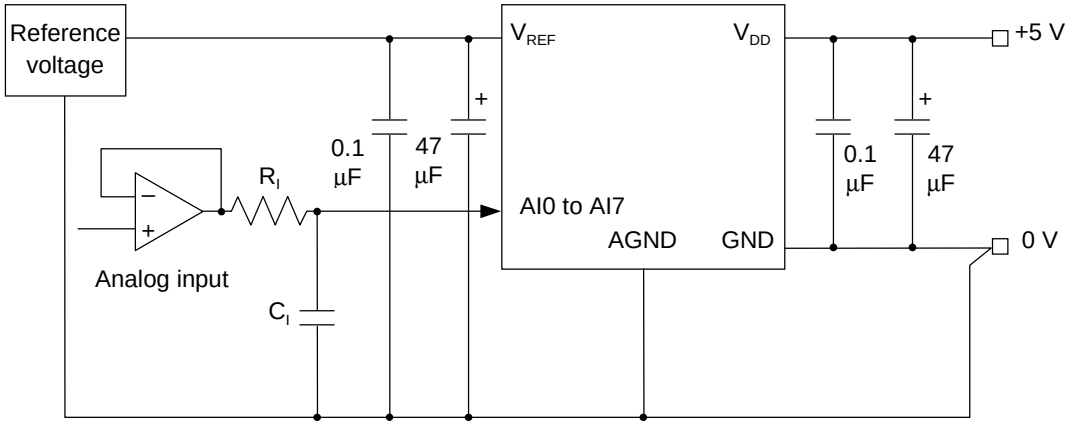
Measurement points for AC timing (except the serial port)



A/D Converter Characteristics

(Ta = –40 to +85°C, V_{DD} = V_{REF} = 4.5 to 5.5 V, AGND = GND = 0 V)

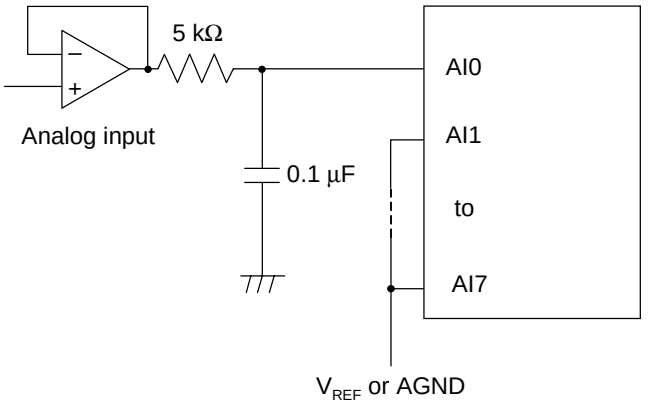
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	Refer to measurement circuit 1 Analog input source impedance $R_I \leq 5$ kΩ t_{CONV} = 10.7 µs	—	10	—	Bit
Linearity error	E_L		—	—	±3	LSB
Differential linearity error	E_D		—	—	±2	
Zero scale error	E_{ZS}		—	—	+3	
Full-scale error	E_{FS}		—	—	–3	
Cross talk	E_{CT}	Refer to measurement circuit 2	—	—	±1	
Conversion time	t_{CONV}	Set according to ADTM set data	10.7	—	—	µs/ch



R_I (impedance of analog input source) ≤5 kΩ

$C_I \cong 0.1$ µF

Measurement Circuit 1



Cross talk is the difference between the A/D conversion results when the same analog input is applied to AI0 through AI7 and the A/D conversion results of the circuit to the left.

Measurement Circuit 2

Definition of Terminology

1. Resolution
   Resolution is the value of minimum discernible analog input.
   With 10 bits, since $2^{10} = 1024$, resolution of $(V_{REF} - AGND) \div 1024$ is possible.

2. Linearity error
   Linearity error is the difference between ideal conversion characteristics and actual conversion characteristics of a 10-bit A/D converter (not including quantization error).
   Ideal conversion characteristics can be obtained by dividing the voltage between V_{REF} and AGND into 1024 equal steps.

3. Differential linearity error
   Differential linearity error indicates the smoothness of conversion characteristics. Ideally, the range of analog input voltage that corresponds to 1 converted bit of digital output is $1LSB = (V_{REF} - AGND) \div 1024$. Differential error is the difference between this ideal bit size and bit size of an arbitrary point in the conversion range.

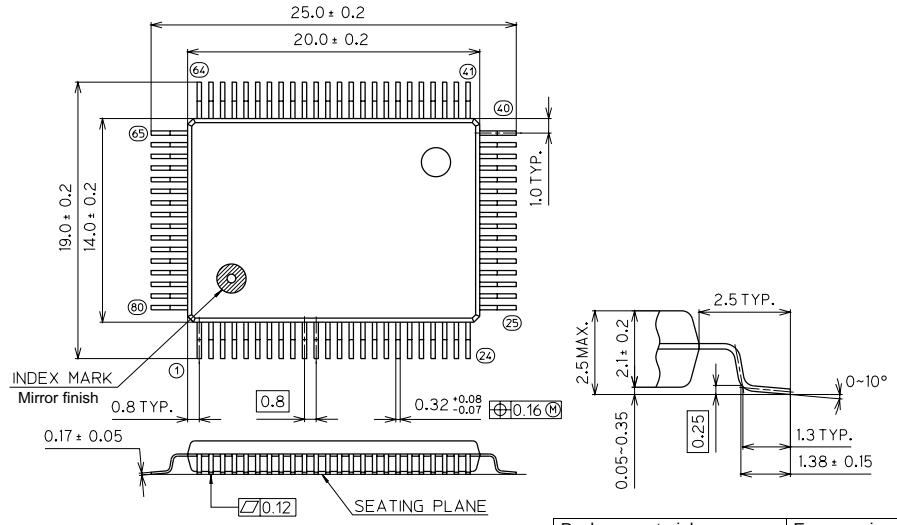
4. Zero scale error
   Zero scale error is the difference between ideal conversion characteristics and actual conversion characteristics at the point where the digital output changes from 000H to 001H.

5. Full-scale error
   Full-scale error is the difference between ideal conversion characteristics and actual conversion characteristics at the point where the digital output changes from 3FEH to 3FFH.

PACKAGE DIMENSIONS

(Unit: mm)

QFP80-P-1420-0.80-BK



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	1.27 TYP.
Rev. No./Last Revised	4/Nov. 28, 1996

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Packages

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Date	Changes compared to previous version
Mar. 2000	-
Apr. 2001	- Modified the contents on P-1. - Added the contents in table on P-2. - Modified the contents in Fig. on P-9. - Added the contents of P3_2 and P3_3 in table on P-10 and P-13. - Modified the contents of P5_6 and P5_7 in table on P-13. - Added the contents of V_{REF} and AGND in table on P-12 and P-15. - Modified the contents of "H" output pin (1pin) in table on P-17. - Added the contents in Fig. and table on P-23.
Oct. 2001	- Deleted the product name of ML66514. - Deleted the product name of ML66Q515.

NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

4. Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.

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