OKI

ML64168/P168

4-Bit Microcontroller User's Manual

THIRD EDITION

Sep. 1999

OKI ELECTRIC INDUSTRY CO., LTD.

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Introduction

The ML64168 is a high-performance single chip microcontroller that uses a 4-bit CPU core (nX-4/30). This Oki-original CPU core architecture is combined with additional on-Chip peripheral functions.

This manual explains hardware of the ML64168 and instruction set.

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Chapter 1

Overview

This chapter describes the features, block diagrams, pin configurations, pin descriptions and basic operation timings.

Chapter 1 Overview

1.1 Overview

The ML64168 is a CMOS 4-bit microcontroller that has built-in 512-nibble RAM, 20 I/O ports, buzzer output, a serial port, a 2-channel RC oscillation type A/D converter and 34 LCD segment drivers.

The ML64168 uses a high-performance 4-bit CPU core (nX-4/30) with byte processing instructions and is best suited for applications such as thermometers, hygrometers and body thermometers because of its compact chip layout and rich peripheral functions.

Note: See Chapter 17 for the overview of the OTP version (ML64P168).

1.2 Features

(1) Rich instruction set including byte operation instructions
- 148 instructions
- Byte addition/subtraction, byte transfer and byte comparison instructions
- Bit manipulation instructions
- Data exchange instructions

(2) Rich addressing modes
- Two kinds of indirect addressing modes using HL register and XY register
- Bit manipulation on entire data memory area
- Byte operation on entire data memory area

(3) Operating frequencies
- Low speed clock 32.768 kHz crystal oscillation (minimum instruction execution time: 91 μs)
- High speed clock 700 kHz RC oscillation

(4) Built-in program memory : 8160 bytes

(5) Built-in data memory : 512 nibbles

(6) I/O ports : 20
- 4-bit input/output port (NMOS open drain output/CMOS output selectable, input with pull-down/pull-up resistance or high-impedance input selectable) × 3
- 4-bit input port (Input with pull-down/pull-up resistance selectable) × 1
- 4-bit output port (NMOS open drain output/CMOS output selectable) × 1

(7) Buzzer output : 1
- 4 output modes selectable

(8) Serial port : 1
- Synchronous 8-bit transfer
- External clock/internal clock selectable
- MSB head/LSB head selectable

(9) LCD driver : 34
- At 1/4 duty and 1/3 bias : 120 segments (30 × 4)
- At 1/3 duty and 1/3 bias : 93 segments (31 × 3)
- At 1/2 duty and 1/2 bias : 64 segments (32 × 2)
- Output port selectable by mask option for 8 drivers
- Externally supplied (from power supply voltage)/internally supplied (from built-in regulator) reference voltage selectable by mask option

(10) RC oscillation method A/D converter : 2 channels
- Time dividing 2-channel method
- A counter: $1/(10^4 \times 8) \times 1$
- B counter :$1/2^{14} \times 1$

(11) Capture circuit : 2 channels
- 256 Hz, 128 Hz, 64 Hz and 32 Hz

(12) Watchdog timer

(13) Interrupt causes: 10 causes
- 2 external causes, 5 time base causes, 1 serial port cause, 1 A/D converter cause and 1 watchdog timer cause

(14) Power supply voltage
- 1.5 V/3 V selectable by mask option
- Low power consumption

(15) Battery check circuit

(16) Exterior
- Chip
- 80-pin flat package

1.3 Block Diagram

Figure 1-1 shows the block diagram of the ML64168.

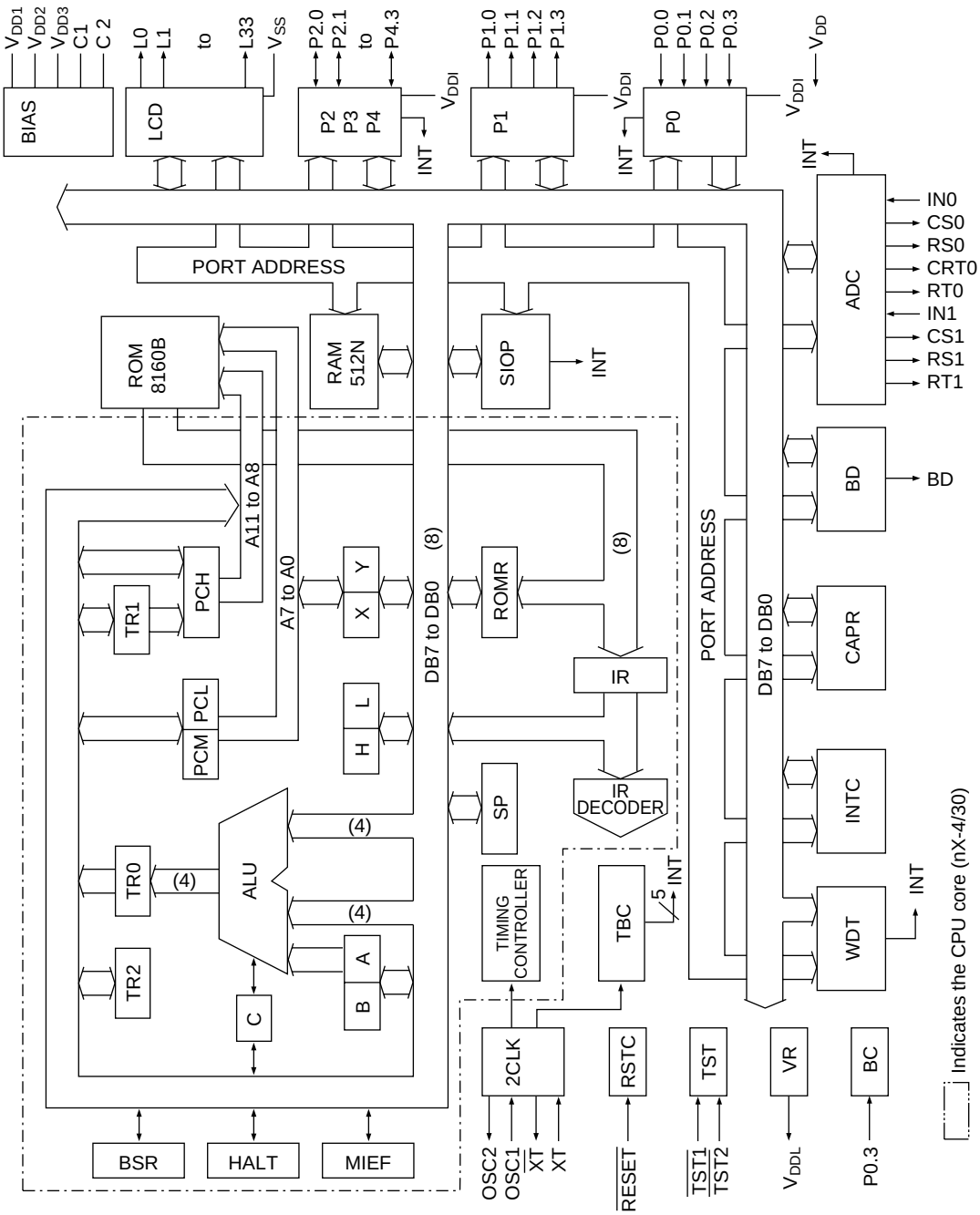


Figure 1-1 ML64168 Block Diagram

1.4 Pin Configuration

The pin configuration of the package of ML64168 and the chip exterior figure are shown in Figures 1-2, 1-3, 1-4 and 1-5.

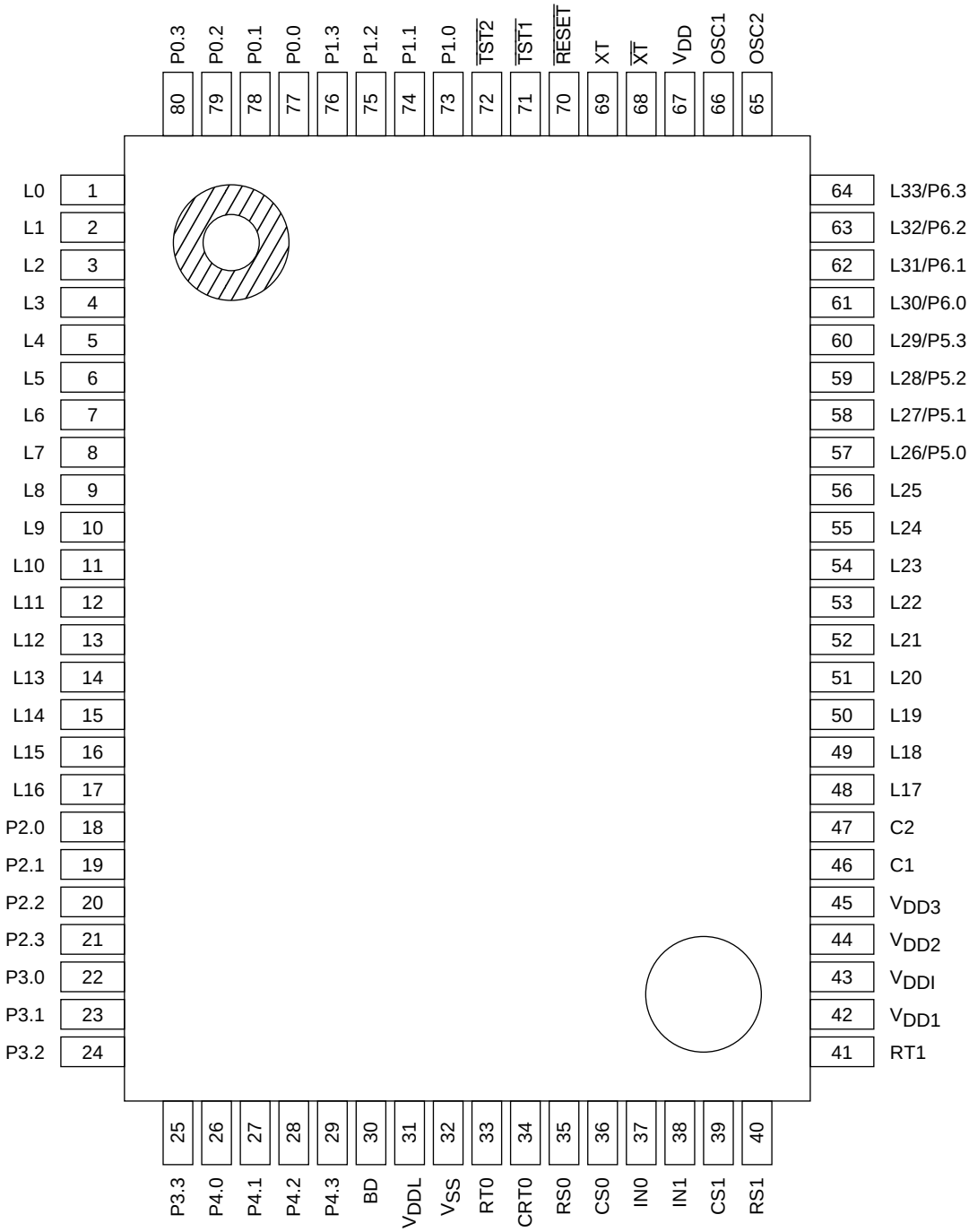


Figure 1-2 ML64168 (GP) Pin Configuration

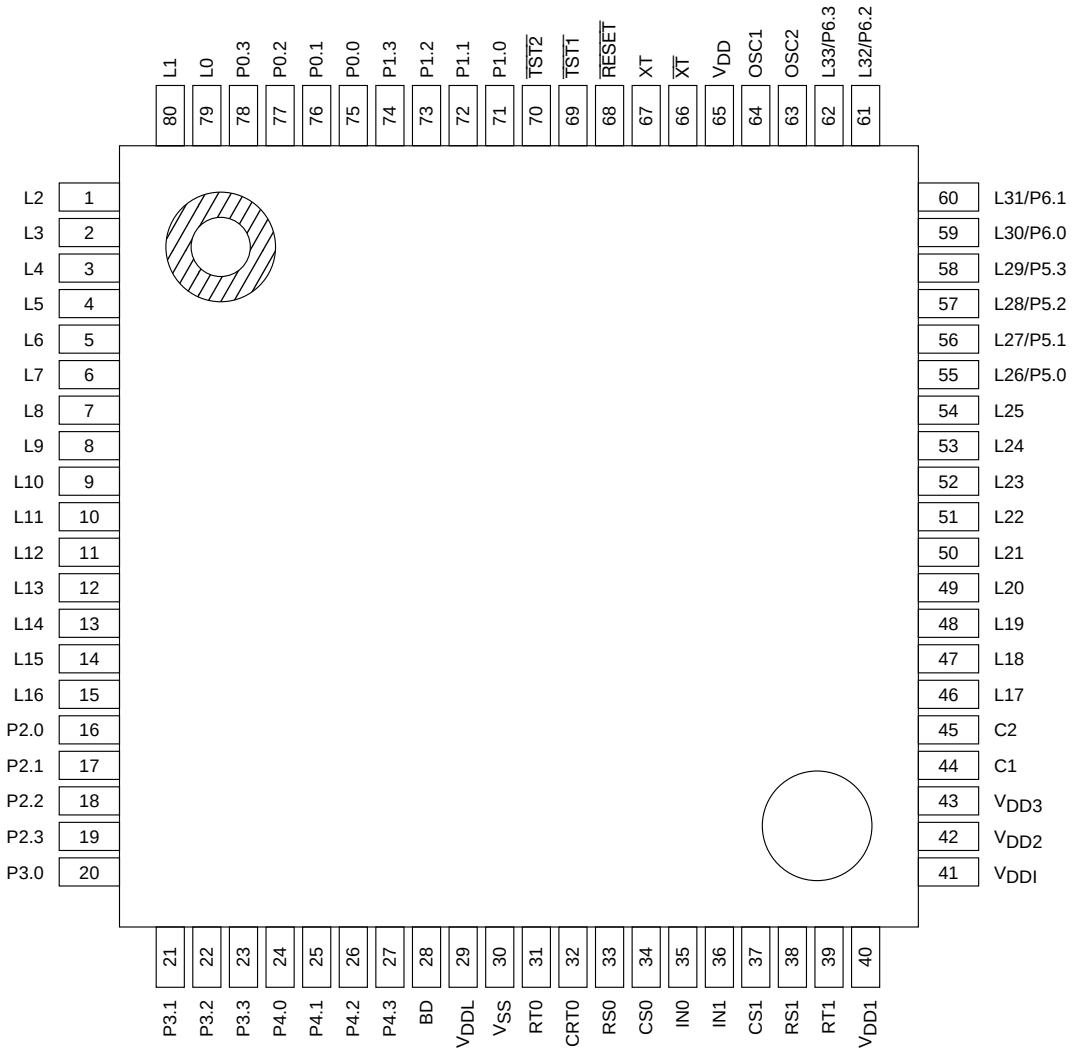


Figure 1-3 ML64168 (GA) Pin Configuration

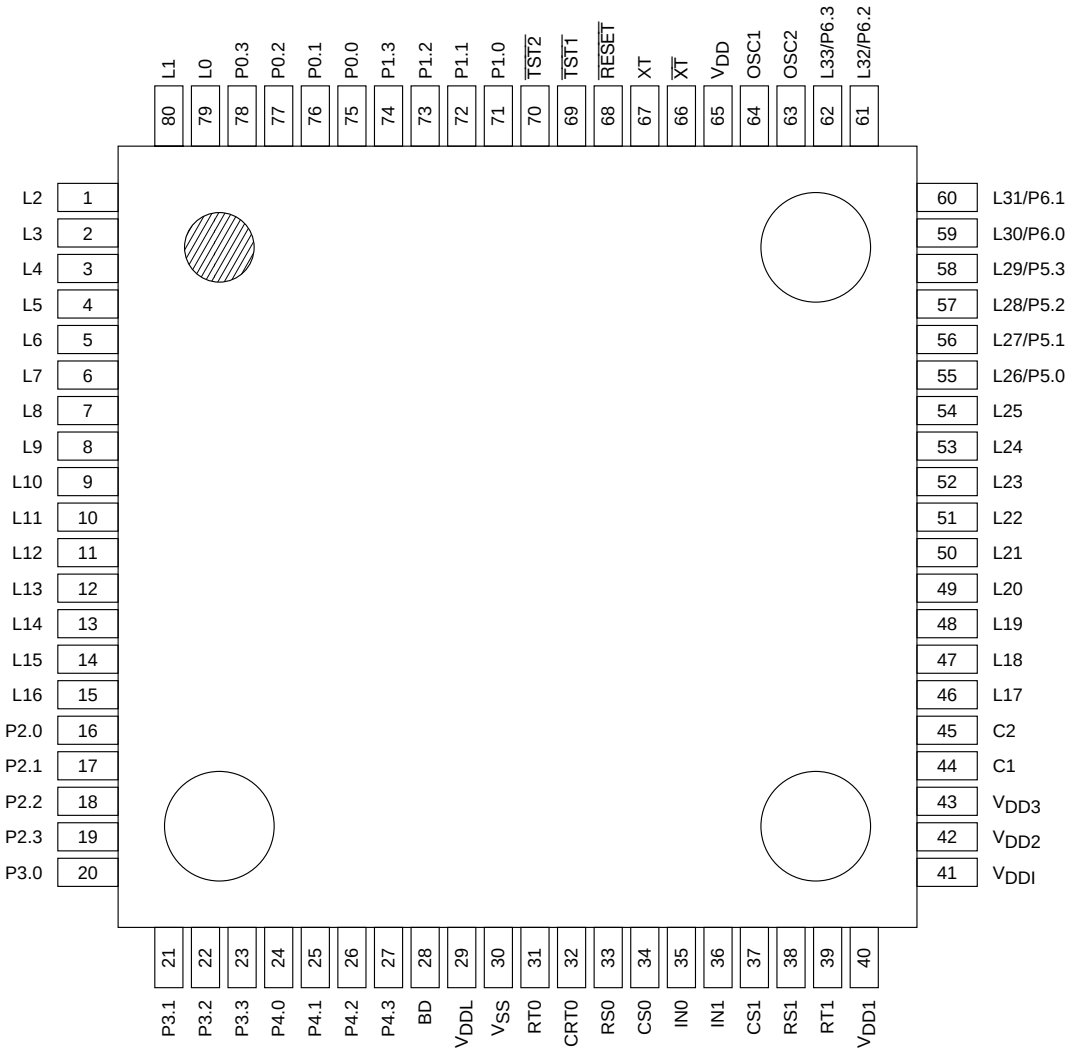


Figure 1-4 ML64168 (TB) Pin Configuration

ML64168-xxx Chip size : 5.07 mm × 5.50 mm / Thickness : 350 μm (Typ.)

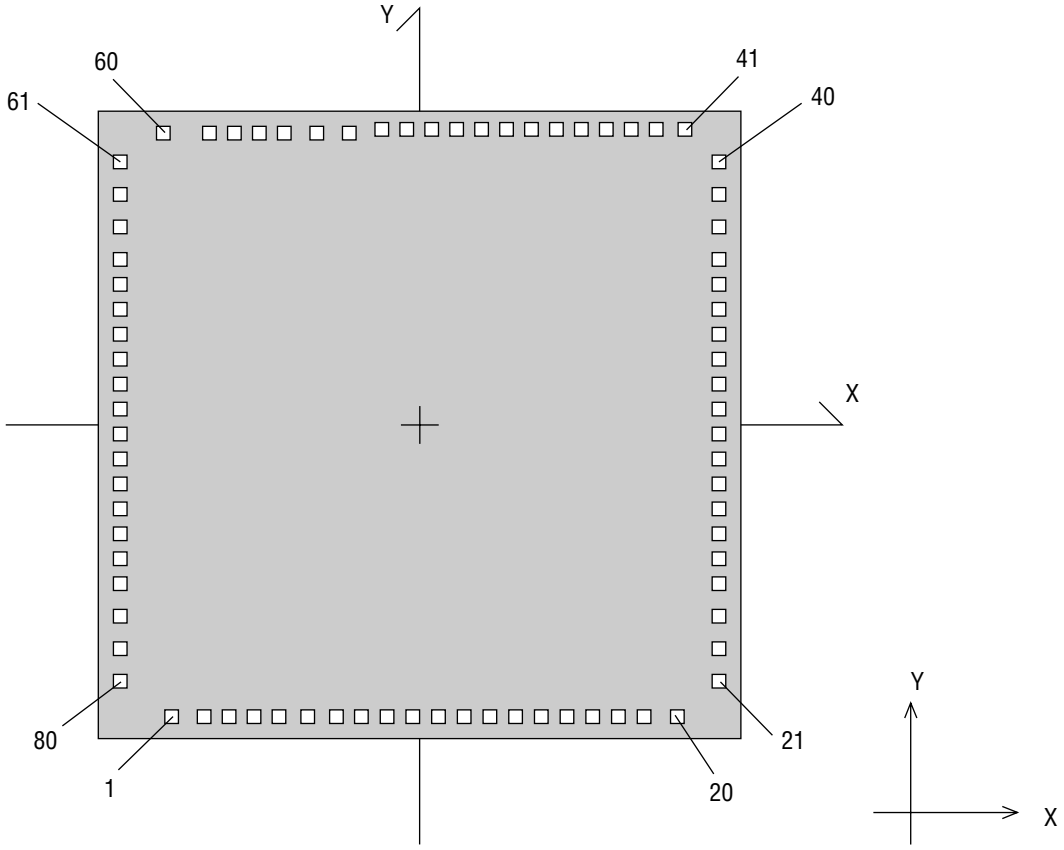


Figure 1-5 ML64168 Chip Exterior Figure

1.5 Pin Description

1.5.1 Description of Each Pin

The basic functions of each pin of the ML64168 are shown in Table 1-1 and their secondary functions are shown in Table 1-2.

Table 1-1 (A) Description of Pin (Basic Function)

Classification	Pin name	Pin No.		Pad No.	Input/ Output	Function
		GP	GA, TB			
Power supply	V_{SS}	32	30	30	—	0 V power supply
	V_{DD}	67	65	65	—	Positive side power supply
	V_{DD1}	42	40	40	—	Bias output for driving LCD (1.2 V/1.5 V)
	V_{DD2}	44	42	42	—	Bias output for driving LCD (2.4 V/3.0 V)
	V_{DD3}	45	43	43	—	Bias output for driving LCD (3.6 V/4.5 V)
	V_{DDI}	43	41	41	—	Positive side power supply for input/ output port interface
	C1	46	44	44	—	Capacitor connection pins for LCD driving bias generation
	C2	47	45	45	—	
	V_{DDL}	31	29	29	—	Positive side power supply pin for internal logic (internally generated constant voltage)
Oscillation	XT	69	67	67	Input	Low speed side clock oscillation input pin: Connects to the crystal oscillator (32.768 kHz)
	$\overline{XT}$	68	66	66	Output	Low speed side clock oscillation output pin: Connects to the crystal oscillator (32.768 kHz)
	OSC1	66	64	64	Input	High speed side clock oscillation pins: Connect to the external resistance of oscillation (R_{OS}).
	OSC2	65	63	63	Output	
Test	$\overline{TST1}$	71	69	69	Input	Input pins for test: Pulled-up to V_{DD} inernally.
	$\overline{TST2}$	72	70	70	Input	
Reset	$\overline{RESET}$	70	68	68	Input	System reset input: When this pin becomes "H" level from "L" level, the internal state is initialized and execution of an instruction starts from address 000H. Pulled-up to V_{DD} internally.

Table 1-1 (B) Pin Description (Basic Functions)

Classification	Pin name	Pin No.		Pad No.	Input/ Output	Function
		GP	GA, TB			
Port	P0.0	77	75	75	Input	4-bit input port (P0): Can select (1) input with pull-up resistance, (2) input with pull-down resistance or (3) input with high impedance by the port 01 control register (P01CON). As a secondary function, P0.0 to P0.3 are assigned external interrupt functions and P0.0 and P0.1 are assigned a capture trigger function.
	P0.1	78	76	76	Input	
	P0.2	79	77	77	Input	
	P0.3	80	78	78	Input	
	P1.0	73	71	71	Output	4-bit output port (P1): Can select NMOS open drain output or CMOS output by the port 01 control register (P01CON). P1.0 is a large current drive output port.
	P1.1	74	72	72	Output	
	P1.2	75	73	73	Output	
	P1.3	76	74	74	Output	
	P2.0	18	16	16	Input/ Output	4-bit input/output port (P2): Can select (1) pull-up or pull-down resistance input, (2) high impedance input, (3) NMOS open drain output or (4) CMOS output by the port 2 control registers 0 to 3 (P20CON to P23CON). As secondary functions, P2.0 to P2.3 are assigned external interrupt functions.
	P2.1	19	17	17	Input/ Output	
	P2.2	20	18	18	Input/ Output	
	P2.3	21	19	19	Input/ Output	
	P3.0	22	20	20	Input/ Output	4-bit input/output port (P3): Can select (1) pull-up or pull-down resistance input, (2) high impedance input, (3) NMOS open drain output or (4) CMOS output by the port 3 control registers 0 to 3 (P30CON to P33CON). As secondary functions, P3.0 to P3.3 are assigned external interrupt functions, and P3.3 is assigned a serial port function.
	P3.1	23	21	21	Input/ Output	
	P3.2	24	22	22	Input/ Output	
	P3.3	25	23	23	Input/ Output	
	P4.0	26	24	24	Input/ Output	4-bit input/output port (P4): Can select (1) pull-up or pull-down resistance input, (2) high impedance input, (3) NMOS open drain output or (4) CMOS output by the port 4 control registers 0 to 3 (P40CON to 43CON). As secondary functions, P4.0 to P4.3 are assigned external interrupt functions, P4.0 to P4.2 are assigned a serial port function and P4.3 is assigned a monitor function for the A/D converter RC oscillation clock.
	P4.1	27	25	25	Input/ Output	
	P4.2	28	26	26	Input/ Output	
	P4.3	29	27	27	Input/ Output	

Table 1-1 (C) Pin Description (Basic Functions)

Classification	Pin name	Pin No.		Pad No.	Input/ Output	Function
		GP	GA, TB			
Buzzer	BD	30	28	28	Output	Output pin for the buzzer drive
A/D converter	RT0	33	31	31	Output	Resistance sensor connection pin for measurement of Channel 0
	CRT0	34	32	32	Output	Resistance/capacitance sensor connection pin for measurement of Channel 0.
	RS0	35	33	33	Output	Reference resistance connection pin of Channel 0
	CS0	36	34	34	Output	Reference capacitance connection pin of Channel 0
	IN0	37	35	35	Input	Input pin of RC oscillation circuit of Channel 0
	RT1	41	39	39	Output	Resistance sensor connection pin for measurement of Channel 1
	RS1	40	38	38	Output	Reference resistance connection pin of Channel 1
	CS1	39	37	37	Output	Reference capacitance connection pin of Channel 1
	IN1	38	36	36	Input	Input pin of RC oscillation circuit of Channel 1

Table 1-1 (D) Pin Description (Basic Functions)

Classification	Pin name	Pin No.		Pad No.	Input/ Output	Function
		GP	GA, TB			
LCD driver	L0	1	79	79	Output	LCD segment/common signal output pins.
	L1	2	80	80	Output	
	L2	3	1	1	Output	
	L3	4	2	2	Output	
	L4	5	3	3	Output	
	L5	6	4	4	Output	
	L6	7	5	5	Output	
	L7	8	6	6	Output	
	L8	9	7	7	Output	
	L9	10	8	8	Output	
	L10	11	9	9	Output	
	L11	12	10	10	Output	
	L12	13	11	11	Output	
	L13	14	12	12	Output	
	L14	15	13	13	Output	
	L15	16	14	14	Output	
	L16	17	15	15	Output	
	L17	48	46	46	Output	
	L18	49	47	47	Output	
	L19	50	48	48	Output	
	L20	51	49	49	Output	
	L21	52	50	50	Output	
	L22	53	51	51	Output	
	L23	54	52	52	Output	
	L24	55	53	53	Output	
	L25	56	54	54	Output	
	L26/P5.0	57	55	55	Output	LCD segment/common signal output pins. Can function as output ports by the mask option.
	L27/P5.1	58	56	56	Output	
	L28/P5.2	59	57	57	Output	
	L29/P5.3	60	58	58	Output	
	L30/P6.0	61	59	59	Output	
	L31/P6.1	62	60	60	Output	
	L32/P6.2	63	61	61	Output	
	L33/P6.3	64	62	62	Output	

Table 1-2 Pin Description (Secondary Functions)

Classification	Pin name	Pin No.		Pad No.	Input/ Output	Function
		GP	GA, TB			
External interrupt	P0.0	77	75	75	Input	Secondary function: An external interrupt input pin. Can receive interrupt by level change.
	P0.1	78	76	76		
	P0.2	79	77	77		
	P0.3	80	78	78		
	P2.0	18	16	16	Input	Secondary function: An external interrupt input pin. Can receive interrupt by level change.
	P2.1	19	17	17		
	P2.2	20	18	18		
	P2.3	21	19	19		
	P3.0	22	20	20		
	P3.1	23	21	21		
	P3.2	24	22	22		
	P3.3	25	23	23		
	P4.0	26	24	24		
	P4.1	27	25	25		
	P4.2	28	26	26		
	P4.3	29	27	27		
Capture trigger	P0.0	77	75	75	Input	Secondary function: Trigger input pin of the capture circuit.
	P0.1	78	76	76		
Serial port	P3.3	25	23	23	Input	Secondary function: Assigned to data input (SIN) of the serial port.
	P4.0	26	24	24	Output	Secondary function: Assigned to data output (SOUT) of the serial port.
	P4.1	27	25	25	Output	Secondary function: Assigned to ready output (SPR) of the serial port.
	P4.2	28	26	26	Input/ Output	Secondary function: Assigned to clock input/output (SCLK) of the serial port.
RC oscillation monitor	P4.3	29	27	27	Input	Secondary function: Monitor output pin of the RC oscillation clock for the system clock and the RC oscillation clock for the A/D converter.

1.5.2 Unused Pin Description

Table 1-3 shows processing of unused pins.

Table 1-3 Processing of Unused Pins

Pin	Recommended pin connection
OSC1	Open
OSC2	Open
$\overline{TST1}$, $\overline{TST2}$	Open
P0.0 to P0.3	"L" level, "H" level or open (depends on input mode selection)
P1.0 to P1.3	Open
P2.0 to P2.3	At input: "L" level, "H" level or open (depends on input mode selection) At output: Open
P3.0 to P3.3	At input: "L" level, "H" level or open (depends on input mode selection) At output: Open
P4.0 to P4.3	At input: "L" level, "H" level or open (depends on input mode selection) At output: Open
BD	Open
RT0	Open
CRT0	Open
RS0	Open
CS0	Open
IN0	Open
RT1	Open
RS1	Open
CS1	Open
IN1	Open
L0 to L33	Open

1.6 Basic Timing

The ML64168 generates a system clock (CLK) by one of two methods, a 32.768 kHz crystal oscillator or a 700 kHz RC oscillator.

A phase of CLK correspondes with a phase of $\overline{XT}$ or OSC1.

Each instruction is processed/executed between one machine cycle (minimum) and five machine cycles (maximum).

The S1 state of the first machine cycle (M1) of an instruction is M1•S1.

Figure 1-6 shows the relationship among system clock (CLK), the three states (S1, S2 and S3) and machine cycles.

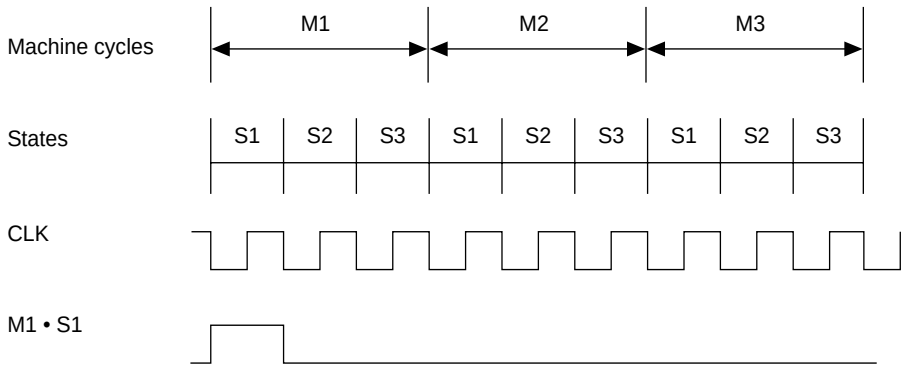


Figure 1-6 Machine Cycle Definition

Chapter 2

CPU

Chapter 2 CPU

2.1 Overview

The instruction set of the ML64168 is composed of 148 different instructions that contain byte operations. The address space of the ML64168 is divided into 8-bit width program memory area and a 4-bit width data memory area.

Program data and 32-byte test data are assigned to the program memory area inside the chip. The data memory area has 512-nibble RAM in Bank 7 and Bank 6 and the special function registers (SFRs) in Bank 0.

Stacks for subroutines and interrupts are placed in the 128 nibbles from address 780H to address 7FFH in Bank 7 by the stack pointer. Figure 2-1 shows each register and memory space.

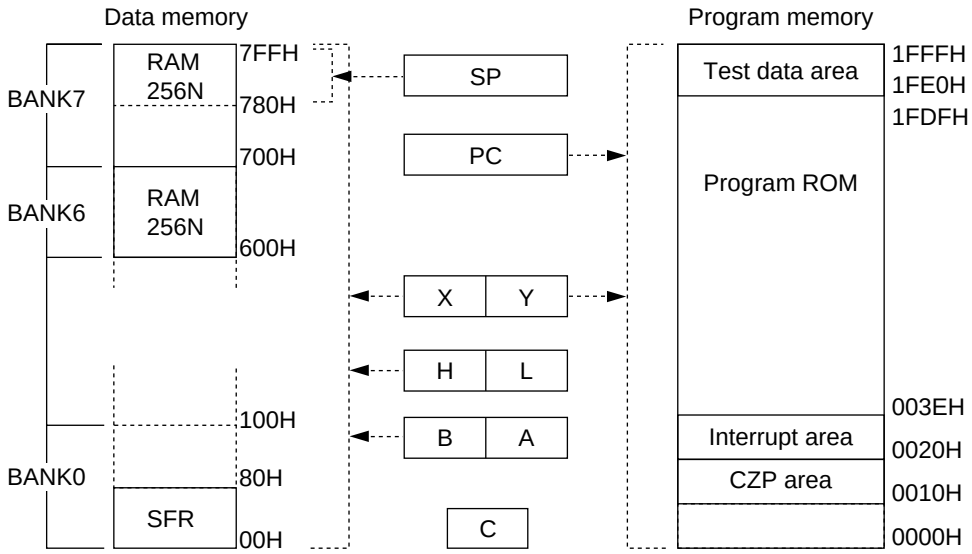


Figure 2-1 Registers and Memory Space

Notes:

(1) Banks in data memory can be specified by the contents of the bank select registers (BSR0 and BSR1) and the state of the bank control flags (BCF and BEF).

(2) The 32 bytes of address 1FE0H to 1FFFH in the program memory are for a factory test data area and cannot be used for a program data area.

2.2 Layout of Registers

Figure 2-2 shows the layout of registers of the ML64168.

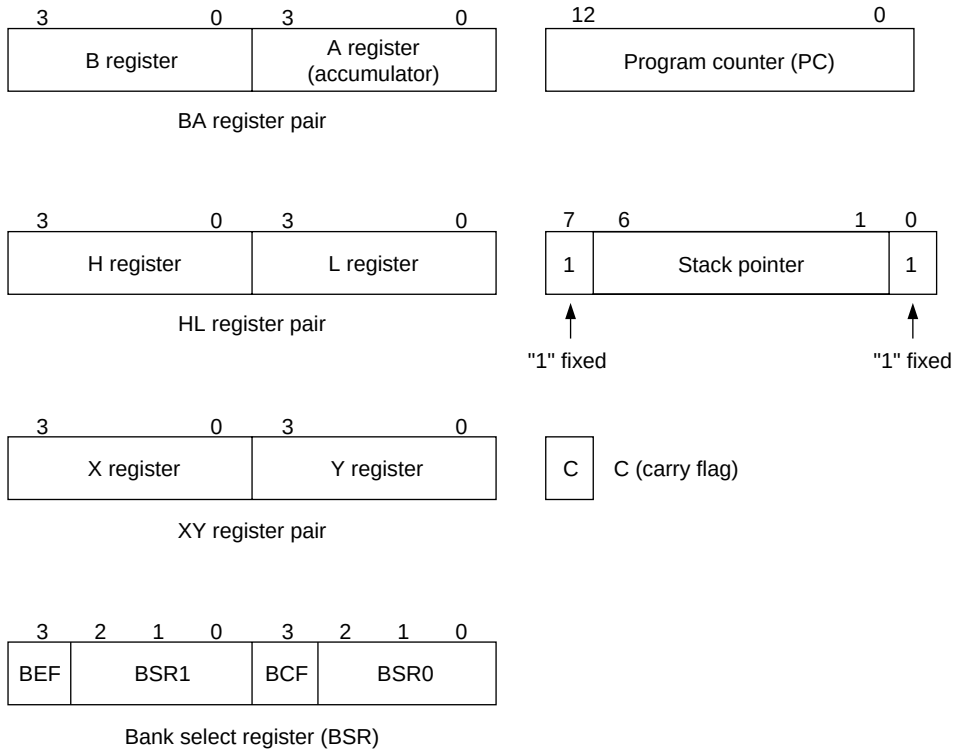
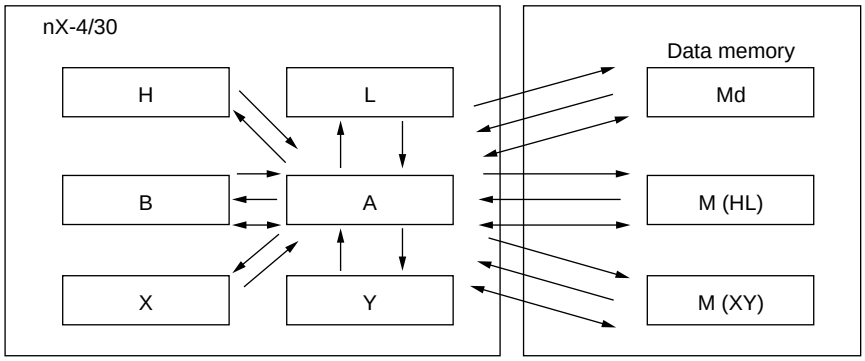


Figure 2-2 Register Layout of ML64168

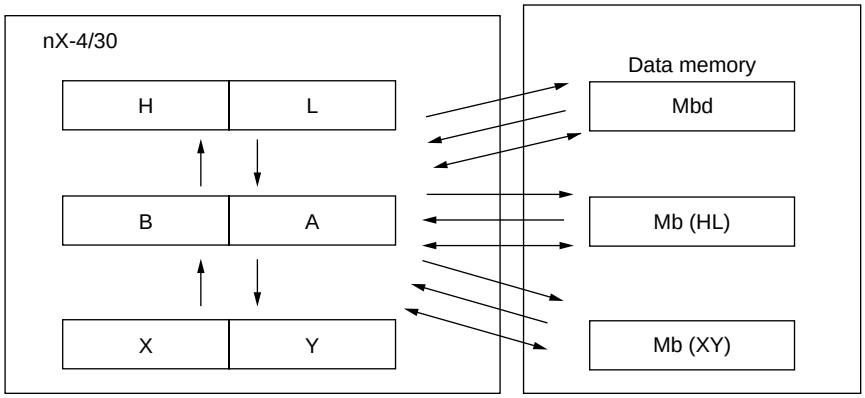
2.2.1 Registers A, B, H, L, X and Y

The A register (accumulator) is a central register of each operation processing. There are five working registers of B, H, L, X and Y. The B register combined with the A register plays a central role for processing byte data. H and L registers and X and Y registers are used for indirect addressing of data memory and for working registers of byte processing when they are used in pair. Figure 2-3 shows the possible combination of data transfer among each register and data memory.

(a) 4-bit transfer



(b) 8-bit transfer



Note: → , ← : data transfer instruction
↔ : data exchange instruction

Figure 2-3 Combination of Data Transfer among Registers

Here, "M" refers to data memory, index "d" refers to direct addressing mode, "(HL)" and "(XY)" refer to indirect addressing mode and "b" refers to byte data. The arrow indicates the data transfer direction.
When an interrupt is generated, the register pairs of BA and HL are automatically saved to the stack.

2.2.2 Program Counter (PC)

This is a counter of 13 bits and can select a program area of internal 8K bytes.

2.2.3 Stack Pointer (SP)

The stack pointer (SP) is a register to indicate the top address of the stack assigned from 7EH to 7FH on data memory bank 0.

SP is a 6-bit byte-processing-only up/down counter in which the lowest and the highest bits are fixed as "1". SP is counted down when data was saved to the stack and is counted up when data was returned from the stack.

At system reset, SP becomes "0FFH" and the stack addresses become 0FFH and 0FEH in Bank 7.

Please use a byte processing instruction for modification and read-out of the contents of SP. 4-bit processing instructions cannot read/write the contents of SP.

Bits 0 and 7 of SP are ignored at data write instructions and "1" is always read out by data read instructions.

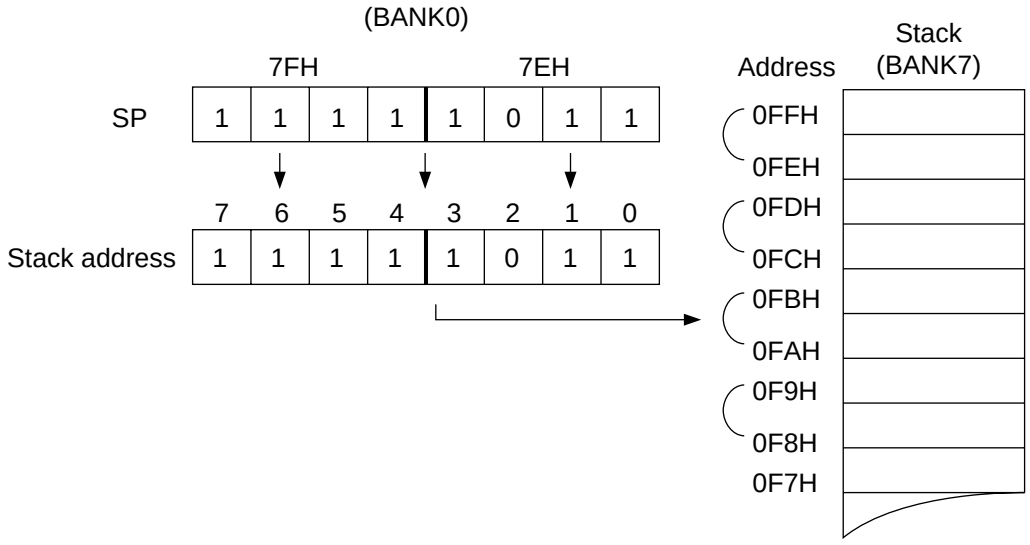


Figure 2-4 Relation between Stack Pointer (SP) and Stack Address

2.2.4 Carry Flag (C)

This is a one-bit flag and is loaded with a carry at the add instruction and is loaded with a borrow at the subtraction instruction. When an interrupt is generated, it is automatically saved to a stack.

2.3 Memory Space

2.3.1 Program Memory Space

The program memory space is a memory area for program data, the interrupt vector table, the CZP area, the start address area and the test data area.

The data length is 8 bits and is assigned from address 0 to address 8191.

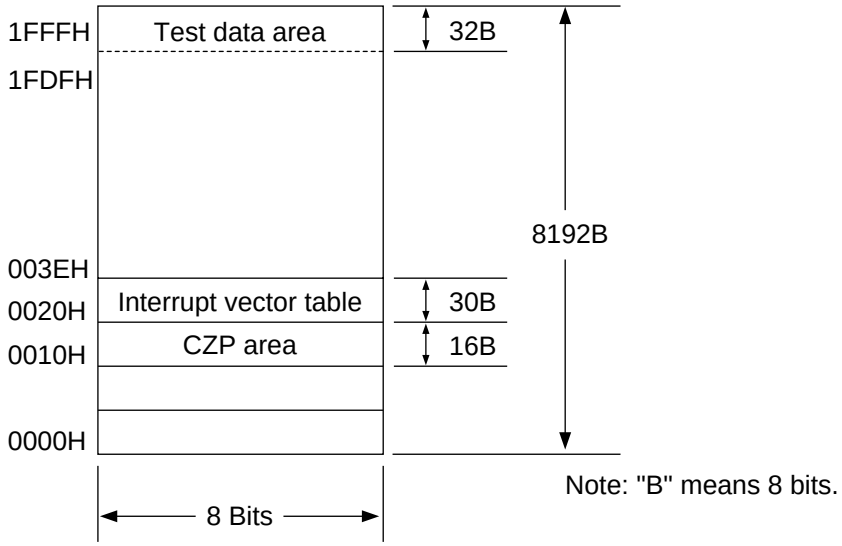


Figure 2-5 Program Memory Address Space

The address space of program memory is shown in Figure 2-5.

Address 0H is the start address of the instruction execution at system reset. The "CZP area" from address 10H to 1FH is the start address range of a CZP subroutine of one byte call instruction and maximum of 8 instructions can be placed. The interrupt vector table is assigned from address 020H to 03DH. 32 bytes from address 1FE0 to 1FFF are a test data area and cannot be used as a program memory area.

For details of interrupts, refer to Chapter 4 "Interrupt" and related chapters for peripheral functions.

2.3.2 Data Memory Space

2.3.2.1 Data Memory Space

The data memory space is assigned data memory and special function registers (SFRs) and is located in a different address space from the program memory space. The data length is 4 bits. The data memory space uses two bank areas with 256 nibbles as one bank unit; one for the SFR area of Bank 0; the other for the data/stack area from address 600H to address 7FF in Bank 6/Bank 7.

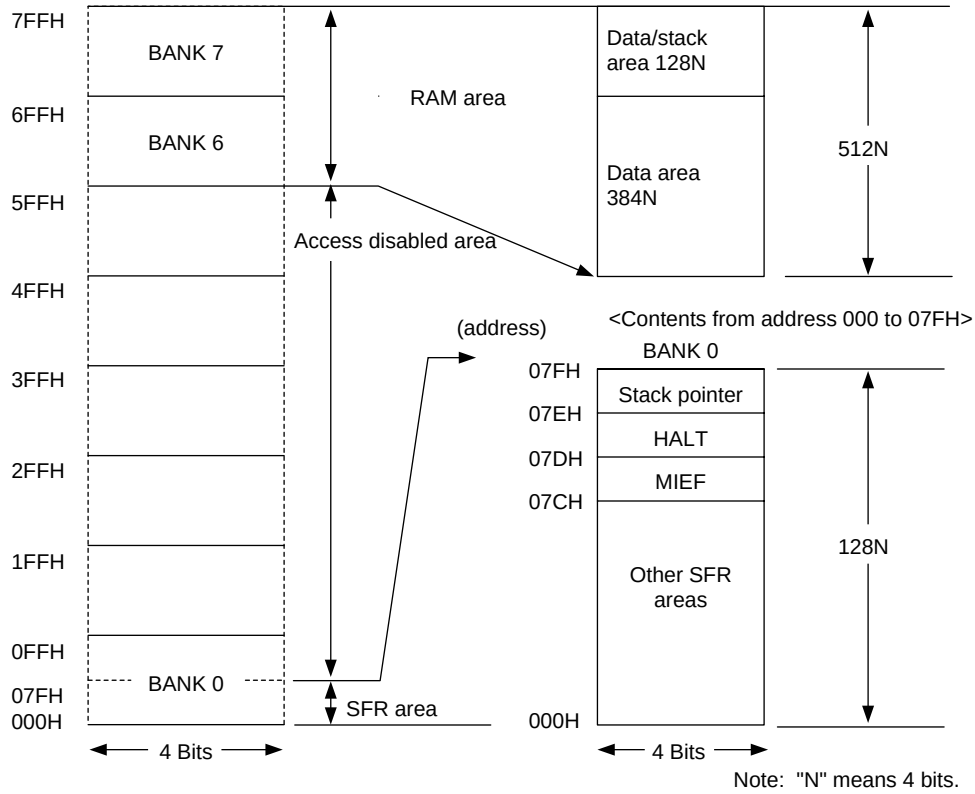


Figure 2-6 Data Memory Address Space

Figure 2-6 shows the address space of data memory. The "stack area" is a data-escape area used by subroutines and interrupts and is valid up to a maximum of 128 N in the direction toward lower addresses starting from the highest address of 7FFH of data memory.

Special function registers (SFRs) are assigned from address 07FH in Bank 0 in the direction toward lower addresses. For addressing mode of the data memory space, the upper 3 bits of the 11 bits of the data memory address can be determined by specifying the bank while the lower 8 bits are determined by either the HL indirect addressing mode, the XY indirect addressing mode or the direct addressing mode.

However, addresses 0H to 7FH of Bank 0 are an exception and if this area is selected by setting the bank common flag (BCF) to 1 in direct addressing mode, Bank 0 is always selected unconditionally. Bank selection is ignored for this case.

2.3.2.2 Bank Selection of Data Memory

Bank selection in data memory can be performed by the bank select registers (BSR0 and BSR1), the bank common flag (BCF) and the bank enable flag (BEF). These registers and flags can be saved and resorted to the stack altogether by the "PUSH BSR" and "POP BSR" instructions.

The HL indirect addressing mode, the XY indirect addressing mode, the direct addressing mode and the stack indirect addressing mode are available for intra-bank addressing in data memory. How each bank can be selected depends on the above mode.

Table 2-1 shows the functions of BCF and BEF. As shown in this table, the bank can be selected by BCF, BEF and addressing mode. "BSR0" and "BSR1" in the table indicate that a bank can be selected by BSR0 and BSR1, respectively. In direct addressing mode, Bank 0 can be selected unconditionally only when BCF = 1 and the addresses are specified as 0 to 7FH.

Table 2-2 shows the correspondence between the contents of BSR0 and BSR1 and the bank number.

Table 2-1 Relation between BCF, BEF and Bank Specification by Addressing Mode

BCF	BEF	HL indirect addressing	XY indirect addressing	Direct addressing	SP indirect addressing
0	0	BSR0	BSR0	BSR0	<BANK7>
0	1	BSR0	BSR1	BSR1	
1	0	BSR0	BSR0	• When addresses in bank are 0 to 7FH:<BANK0> • When addresses in bank are 80 to FFH:BSR0	
1	1	BSR0	BSR1	• When addresses in bank are 0 to 7FH:<BANK0> • When addresses in bank are 80 to FFH:BSR1	

Table 2-2 Correspondence between Contents of BSR0, BSR1 and Bank Number

BSR0, BSR1	Bank number	BSR0, BSR1	Bank number
0	BANK0	4	BANK4
1	BANK1	5	BANK5
2	BANK2	6	BANK6
3	BANK3	7	BANK7

Note : BANK1 to BANK5 cannot be accessed.

2.3.2.3 Addressing Modes of Data Memory

(1) HL indirect addressing mode

Addresses within a bank can be specified by the HL register pair.

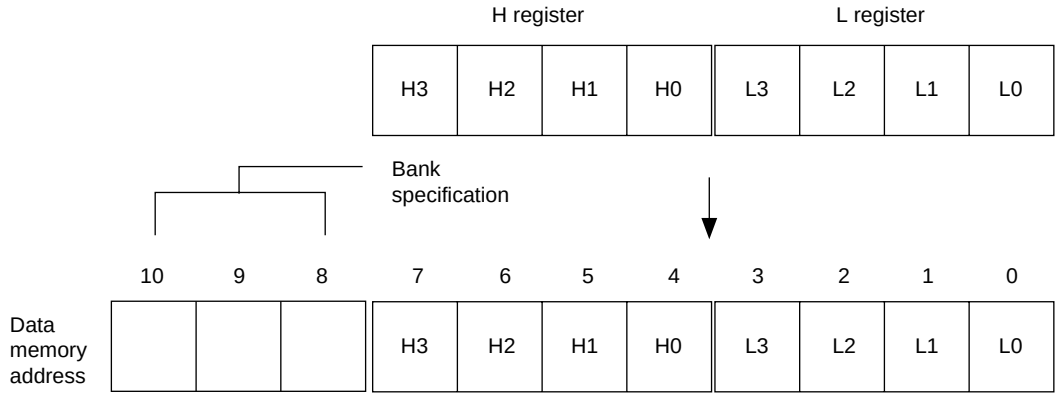


Figure 2-7 Data Memory Address of HL Indirect Addressing

(2) XY indirect addressing mode

Addresses within a bank can be specified by the XY register pair.

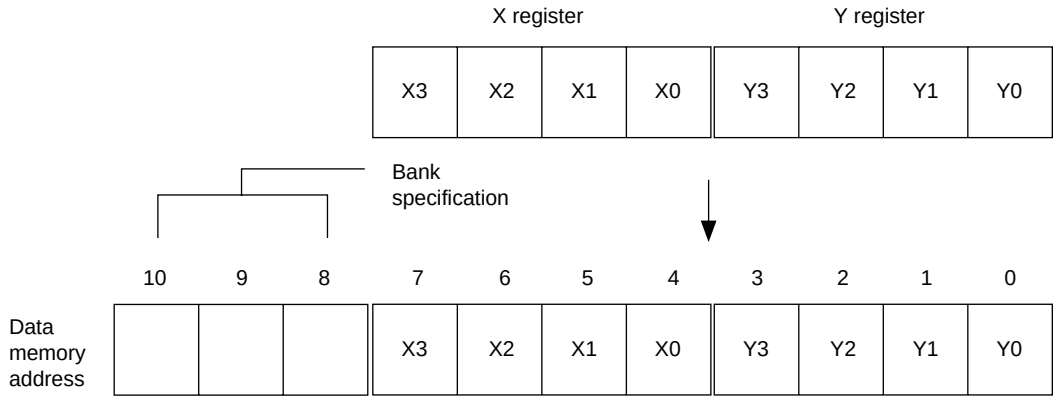


Figure 2-8 Data Memory Address of XY Indirect Addressing

(3) Direct addressing mode

Addresses in a bank can be specified by 8-bit immediate data contained in the instruction code.

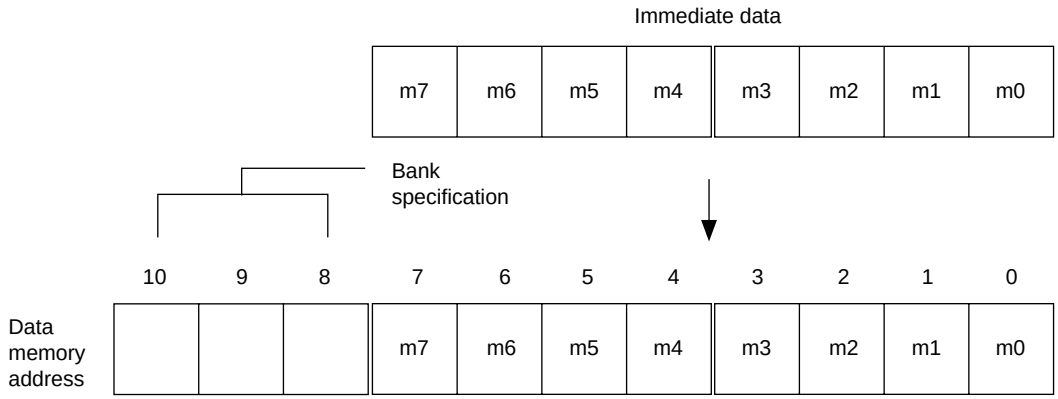


Figure 2-9 Data Memory Address of Direct Addressing

(4) Stack pointer indirect addressing mode

Addresses within Bank 7 can be specified by the stack pointer (SP). This mode is used when manipulating stacks such as the "PUSH" and "POP" instructions and subroutine call, return instructions and interrupts.

In this mode, Bit 0 of the address is not valid as data are always handled in 8 bits (two nibbles). Although SP is an 8 bit register, the highest and the lowest bits always are fixed as "1" and the remaining 6 bits function as an up/down counter.

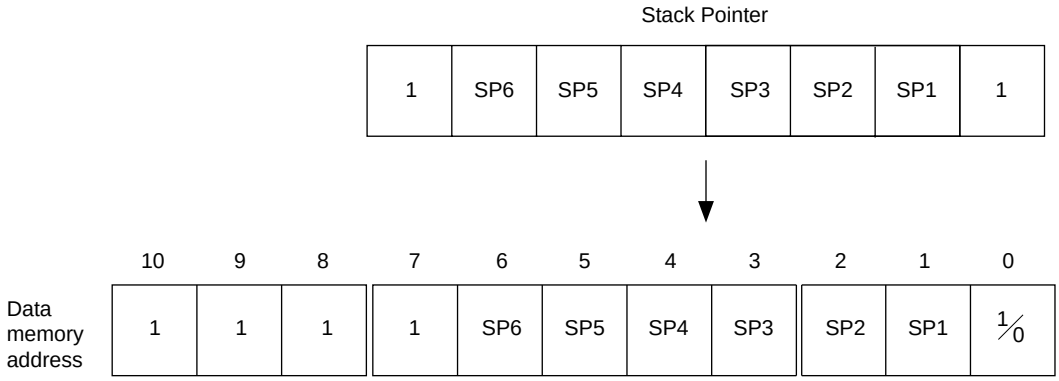


Figure 2-10 Data Memory Address by Stack Pointer Indirect Addressing

Chapter 3

CPU Control Functions

Chapter 3 CPU Control Functions

3.1 Overview

The ML64168 has halt mode besides operation mode. Operation status can be classified as follows including system reset mode:

- Normal operation mode
- System reset mode
- Halt mode

Figure 3-1 shows transition among each state.

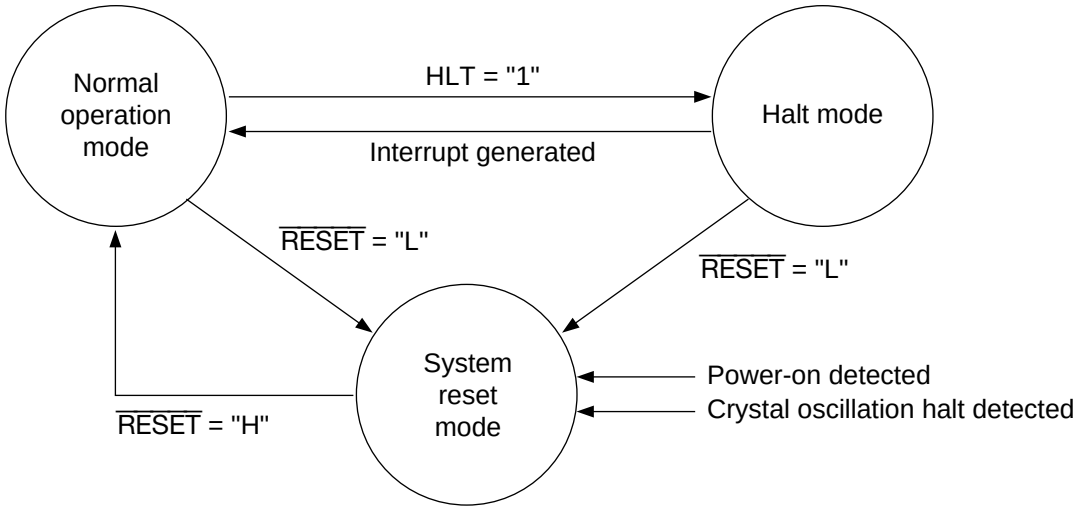


Figure 3-1 Operation Transition Diagram

Normal operation mode is a state that the CPU executes instructions successively. System reset mode is a state starting when the CPU begins system reset processing until each register and each pin are initialized to start execution of the instruction.

Halt mode is a state that the CPU repeats fetching the next instruction only and suspends the execution of instruction. Count-up to the PC is not performed in halt mode. Although the execution of the instruction is suspended in halt mode, internal peripheral functions continue to operate. Transition to this state begins by setting the HLT flag to "1". Halt mode does not influence the functions of ports and peripheral functions.

3.2 System Reset Function

3.2.1 System Reset Operation by $\overline{\text{RESET}}$ Input Pin

System reset mode is started when either power is turned on, crystal oscillation stops or the $\overline{\text{RESET}}$ pin becomes "L" level. In system reset mode, the following take place:

(1) The CPU is initialized.

(2) The power supply V_{DDL} for the crystal oscillation circuit and the logic circuit is set to the V_{DD} voltage level.

At 0.5 second after crystal oscillation starts, V_{DDL} is switched to a constant voltage level which is output of the power supply generation circuit for logic (VR).

(3) The power supply generation circuit for logic (VR) is activated.

(4) The output from the LCD driver is turned off at the V_{SS} level. At about 63 ms after the crystal oscillation starts, waveforms are output to the LCD driver.

(5) All the special function registers (SFRs) are initialized. After the system reset processing, the execution of an instruction is started from address 000H.

Figures 3-2 and 3-3 show the system reset generation circuit and each signal at system reset.

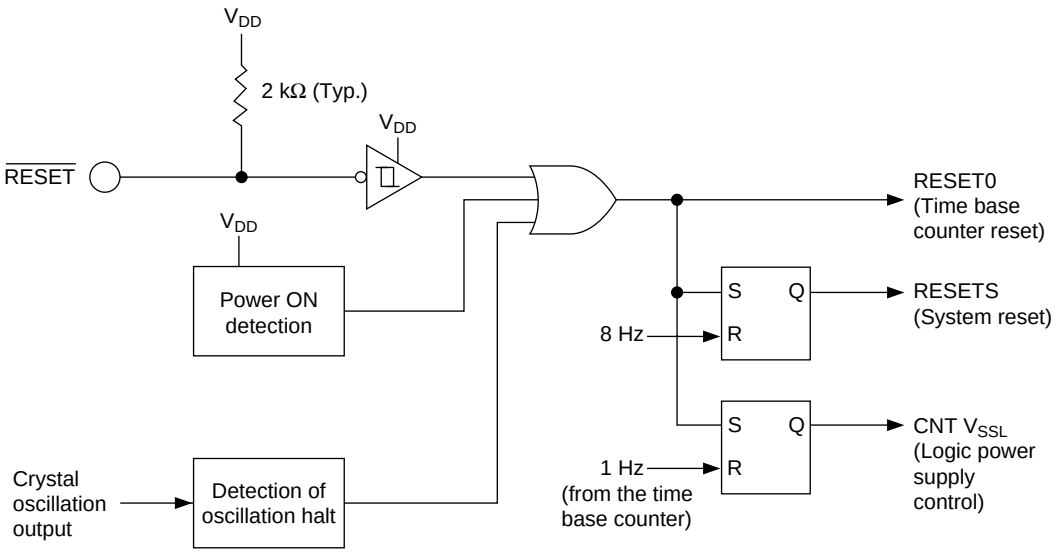


Figure 3-2 System Reset Generation Circuit

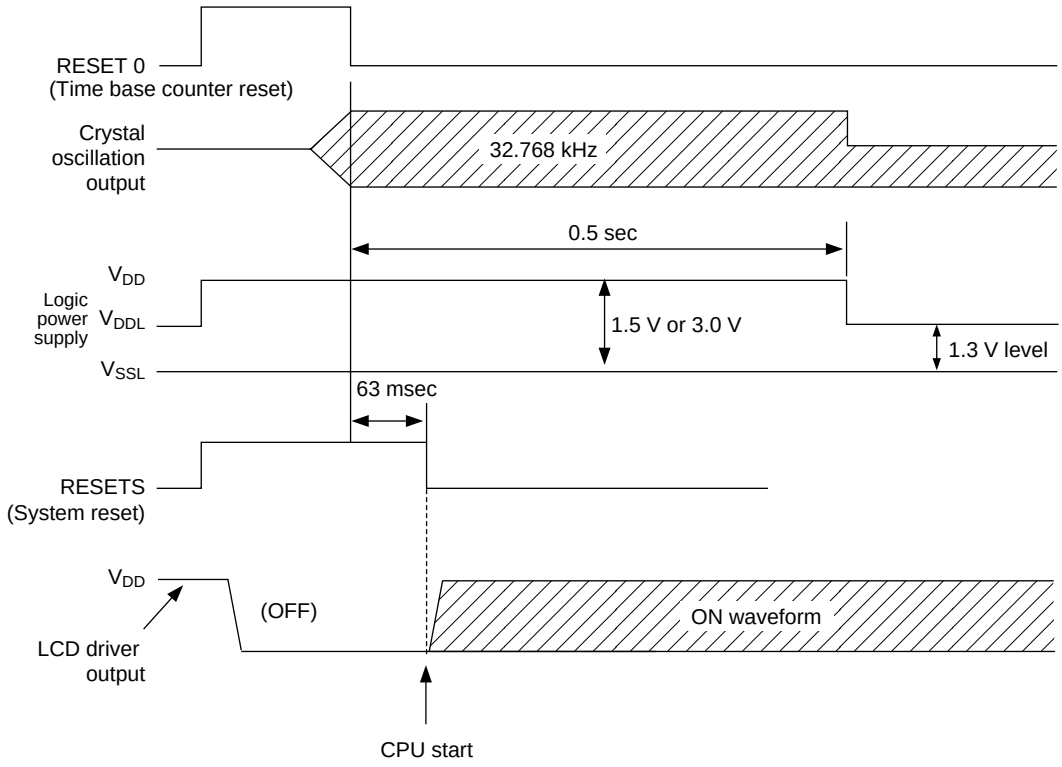


Figure 3-3 Each Signal at System Reset Generation

3.2.2 State at System Reset

Table 3-2 shows the state of the registers after system reset.

Table 3-2 (a) Initial Values at System Reset

Register/Flag	Value at system reset	Note
Program counter (PC)	000H	
A register (A)	0H	
B register (B)	0H	
Carry flag (C)	0	
HL register pair (HL)	00H	
XY register pair (XY)	00H	
Stack pointer (SP)	0FFH	
Bank select register 0 (BSR0)	0H	
Bank select register 1 (BSR1)	0H	
Bank common flag (BCF)	0	
Bank enable flag (BEF)	0	
Port 1 register (P1)	0H	
Port 2 register (P2)	0H	
Port 3 register (P3)	0H	
Port 4 register (P4)	0H	
Port 20 control register (P20CON)	0H	Input mode, input with pull-up/pull-down resistance, 64 Hz sampling, interrupt disabled
Port 21 control register (P21CON)	0H	Input mode, input with pull-up/pull-down resistance, 64 Hz sampling, interrupt disabled
Port 22 control register (P22CON)	0H	Input mode, input with pull-up/pull-down resistance, 64 Hz sampling, interrupt disabled
Port 23 control register (P23CON)	0H	Input mode, input with pull-up/pull-down resistance, 64 Hz sampling, interrupt disabled

Table 3-2 (b) Initial Values at System Reset

Register/Flag	Value at system reset	Note
Port 30 control register (P30CON)	0H	Input mode, input with pull-up/pull-down resistance, 64 Hz sampling, interrupt disabled
Port 31 control register (P31CON)	0H	Input mode, input with pull-up/pull-down resistance, 64 Hz sampling, interrupt disabled
Port 32 control register (P32CON)	0H	Input mode, input with pull-up/pull-down resistance, 64 Hz sampling, interrupt disabled
Port 33 control register (P33CON)	0H	Input mode, input with pull-up/pull-down resistance, interrupt disabled
Port 40 control register (P40CON)	0H	Input mode, input with pull-up/pull-down resistance, interrupt disabled
Port 41 control register (P41CON)	0H	Input mode, input with pull-up/pull-down resistance, interrupt disabled
Port 42 control register (P42CON)	0H	Input mode, input with pull-up/pull-down resistance, interrupt disabled
Port 43 control register (P43CON)	0H	Input mode, input with pull-up/pull-down resistance, interrupt disabled
Port 01 control register (P01CON)	8H	P1 CMOS output mode, P0, P2, P3, P4 input with pull-up resistance
Serial port control register (SCON)	0H	MSB head, internal clock, transfer disabled
Serial port buffer lower register (SBUFL)	0H	
Serial port buffer upper register (SBUFH)	0H	
Frequency control register (FCON)	0EH	Crystal oscillation clock
Buzzer driver control register (BDCON)	0H	Positive logic output, buzzer disabled, discontinuous sound 1 output
Buzzer frequency control register (BFCON)	0H	Output halt
Capture control register (CAPCON)	0H	Capture 0,1 halt
Capture register 0 (CAPR0)	0H	
Capture register 1 (CAPR1)	0H	
Display control register (DSPCON)	0CH	1/4 duty
Display registers 0 to 30 (DSPR0 to 30)	0H	

Table 3-2 (C) Initial Values at System Reset

Register/Flag	Value at system reset	Note
A/D converter control register 0 (ADCON0)	0CH	Counter A select, RC oscillation halt
A/D converter control register 1 (ADCON1)	0H	IN0 clock input mode
A/D converter counter A register 0 (CNTA0)	0H	
A/D converter counter A register 1 (CNTA1)	0H	
A/D converter counter A register 2 (CNTA2)	0H	
A/D converter counter A register 3 (CNTA3)	0H	
A/D converter counter A register 4 (CNTA4)	8H	
A/D converter counter B register 0 (CNTB0)	0H	
A/D converter counter B register 1 (CNTB1)	0H	
A/D converter counter B register 2 (CNTB2)	0H	
A/D converter counter B register 3 (CNTB3)	0CH	
Watchdog timer control register (WDTCON)	—	Reset the watchdog timer counter
Backup control register (BUPCON)	8H	1.3 V level
Interrupt request register 0 (IRQ0)	0H	
Interrupt request register 1 (IRQ1)	0H	
Interrupt request register 2 (IRQ2)	0CH	
Interrupt enable register 0 (IE0)	0H	Interrupt disabled
Interrupt enable register 1 (IE1)	0H	Interrupt disabled
Interrupt enable register 2 (IE2)	0EH	Interrupt disabled
Helt mode register (HALT)	0EH	Normal operation mode
Master interrupt enable register (MIEF)	0EH	Interrupt disabled

Note: System reset has the highest priority over all other processing and all the processes are suspended at system reset. Consequently, there is no guarantee for the contents of RAM that is initialized at system reset.

3.3 Halt Mode

3.3.1 Halt Mode Register (HALT)

This is a special function register (SFR) that controls transition to halt mode.

HALT (7DH) (R/W)

b_3	b_2	b_1	b_0
-----*	-----*	-----*	HLT

Halt mode transition selection flag
- 0: Normal operation mode (initial value)
- 1: Halt mode

*Reserved bit: "1" is always read out. Not valid for write.

Bit 0: HLT

This is a flag to enter halt mode. By setting the HLT flag to "1", the CPU enters halt mode at the first machine cycle of the next instruction.

3.3.2 Operation of Halt Mode

When executing an instruction to set the HLT flag to "1", the CPU enters halt mode at the first machine cycle of the next instruction. However, since the condition for the release of halt mode is an interrupt request, the CPU does not enter halt mode in interrupt request state.

In halt mode, operation of oscillation and the time base counter is still continued and the CPU halts at fetching state S1 for the next instruction.

System reset or an interrupt can release halt mode (reset of the HLT flag). To release halt mode by an interrupt, it is necessary to set the interrupt enable flag to "1" before entering halt mode. Figure 3-4 shows timing to enter halt mode and release timing of halt mode by an interrupt.

Execution of instructions after the release of halt mode depends on the status of the master interrupt enable flag (MI). When the MI flag is "1", execution of instructions is resumed after one dummy cycle by an interrupt process routine as shown in Figure 3-4. When the MI flag is "0", execution of instructions is resumed with a dummy cycle after the following address that the halt instruction is placed as shown in Figure 3-5.

Note: To release halt mode, it is necessary to set an individual interrupt enable flag to "1" regardless of the state of the MI flag. When halt mode is released while the MI flag is "0", the individual interrupt request flag is set to "1".

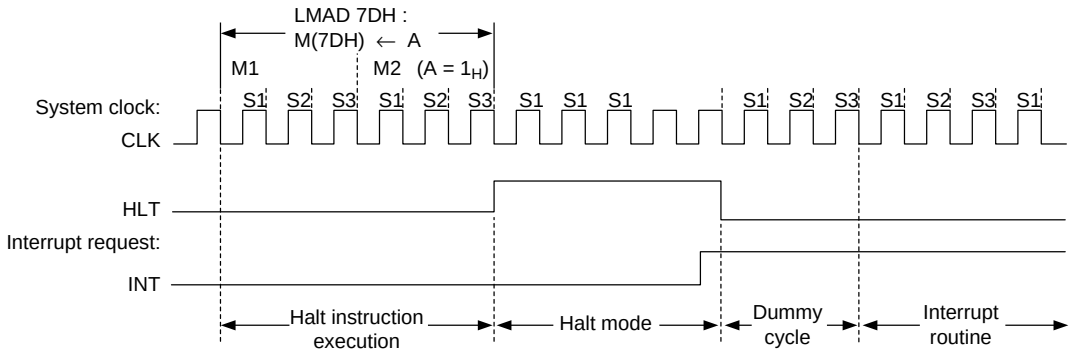


Figure 3-4 Timing of Halt Mode Set and Halt Mode Reset by Interrupt (when the MI flag = "1")

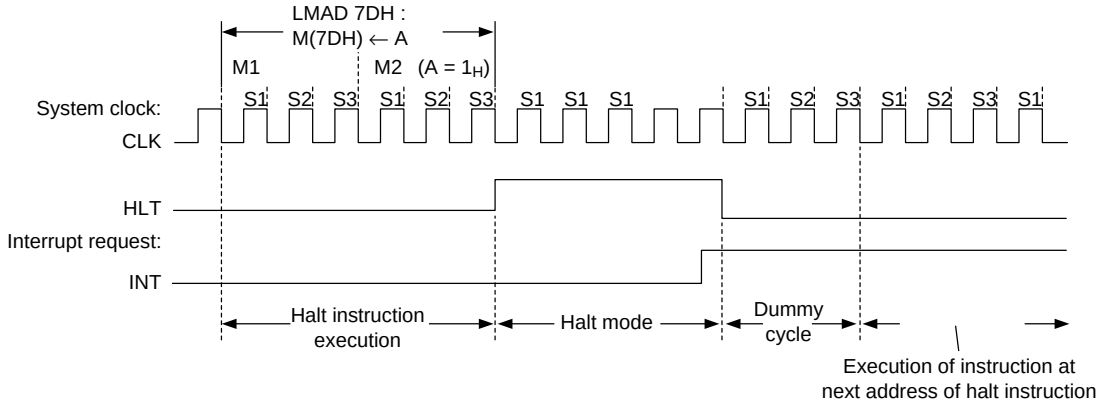


Figure 3-5 Timing of Halt Mode Set and Halt Mode Reset by Interrupt (when the MI flag = "0")

Chapter 4

Interrupt (INTC)

Chapter 4 Interrupt (INTC)

4.1 Overview

The ML64168 has ten interrupt causes (10 vector addresses), two of which are external interrupts from ports and 8 are internal interrupts.

Of the ten interrupt causes, only the watchdog interrupt cannot be disabled (non-maskable interrupt) and other 9 interrupts are controlled by the master interrupt enable flag (MI) and each interrupt enable register (IE0, IE1 and IE2) for enabling/disabling interrupts. When an interrupt condition is met, CPU branches to a vector address corresponding to the interrupt cause.

Table 4-1 shows the list of interrupt causes and vector addresses and Figure 4-1 shows the interrupt control equivalent circuit.

Table 4-1 List of Interrupt Causes

No.	Interrupt cause	Mnemonic	Vector address
1	Watchdog timer interrupt	WDTINT	03BH
2	External 0 interrupt (P2, P3, P4)	XI0INT	038H
3	Serial port interrupt	SIOINT	035H
4	External 1 interrupt (P0)	XI1INT	032H
5	A/D converter interrupt	ADINT	02FH
6	256 Hz interrupt	256HzINT	02CH
7	32 Hz interrupt	32HzINT	029H
8	16 Hz interrupt	16HzINT	026H
9	1 Hz interrupt	1HzINT	023H
10	0.1 Hz interrupt	01HzINT	020H

When two interrupt causes are generated simultaneously, the interrupt with the higher vector address (WDTINT has the highest priority) is given the priority and is executed accordingly.

For details of each interrupt operation, refer to Chapter 6 "Time Base Counter," Chapter 7 "Ports," Chapter 8 "Serial Port," and Chapter 12 "A/D Converter".

(Notes)

The interrupt requests which are generated in the following cases are temporarily held.

1) As a result which executed an instruction with skip, when the skip condition is established.

(The skip action expends the same time as the executive machine cycle of the instruction to be skipped. For this reason, the interrupt requests are held during the same as the executive machine cycle of the instruction to be skipped.)

2) When LAI and LLI instructions (vertical stack instruction) are executed.

3) When ADCS and SUBCS instructions are executed.

The interrupt requests which are temporarily held in the abovementioned cases are received after the execution of the instructions is finished if the next coming instructions are not fitted to the aforementioned conditions.

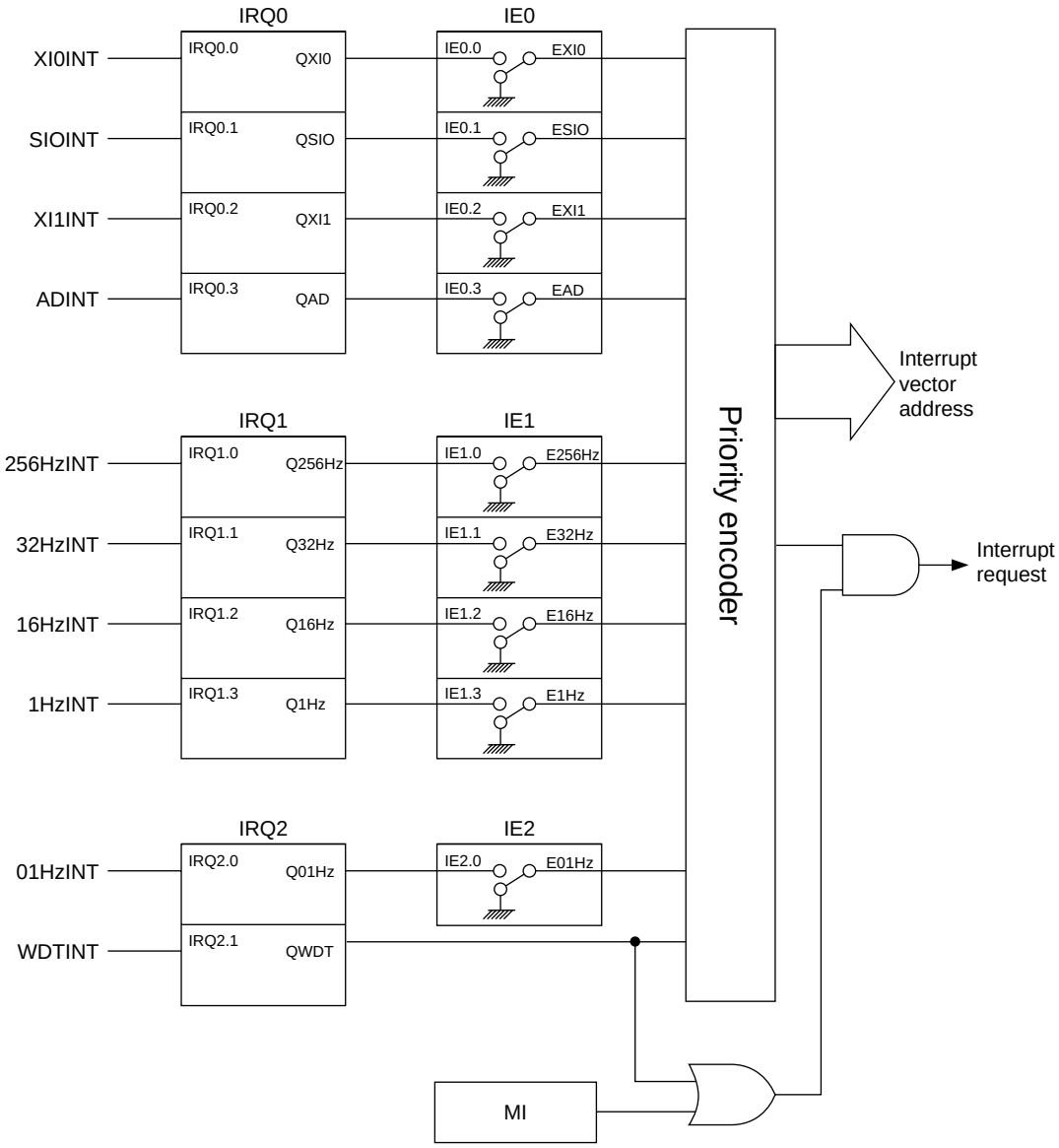


Figure 4-1 Interrupt Control Equivalent Circuit

4.2 Interrupt Sequence

Transition to interrupt processing is performed by generating an individual interrupt cause while the MI flag is set to "1".

An interrupt transition cycle is equivalent to 5 machine cycles and the following are executed:

(1) The MI flag is reset to "0".

(2) The contents of PC, A, B, H and L registers and the carry flag (C) are saved to stack.

(3) The stack pointer (SP) is decremented by 4 (SP ← SP–4).

(4) The program counter (PC) is loaded with the head address of the vector address. At the same time, the interrupt request flag for that interrupt is reset.

Figure 4-1 shows the contents of the stack after the generation of an interrupt.

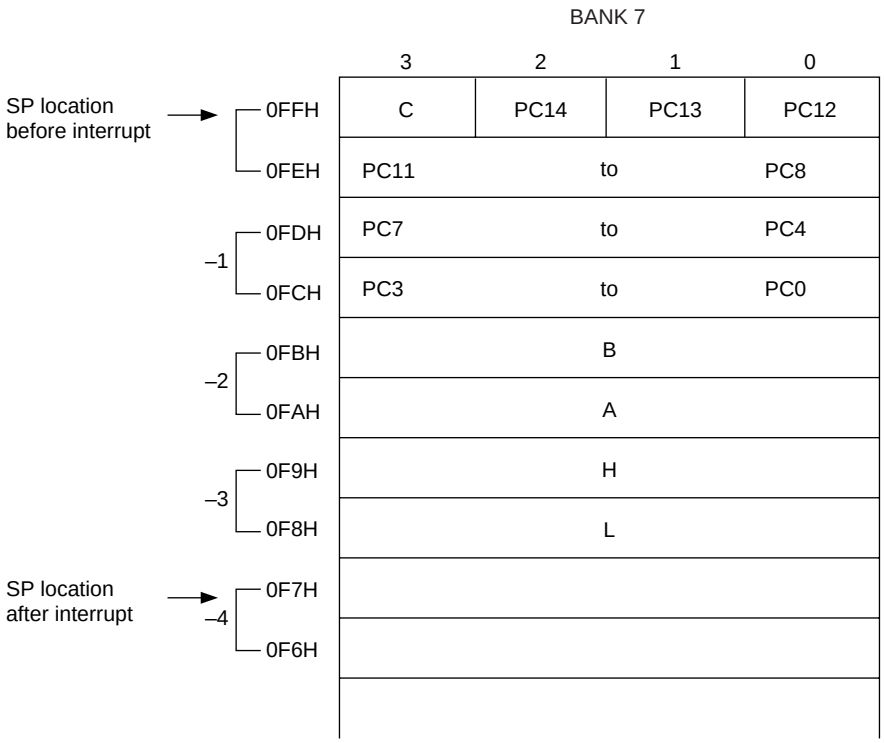


Figure 4-2 Contents of Stack after Interrupt Generation

Return from the interrupt routine is performed by the "RTI" instruction.
The return cycle is equivalent to 5 machine cycles and the following are carried out:

(1) The contents of PC, A, B, H and L registers and the carry flag (C) are restored from the stack.

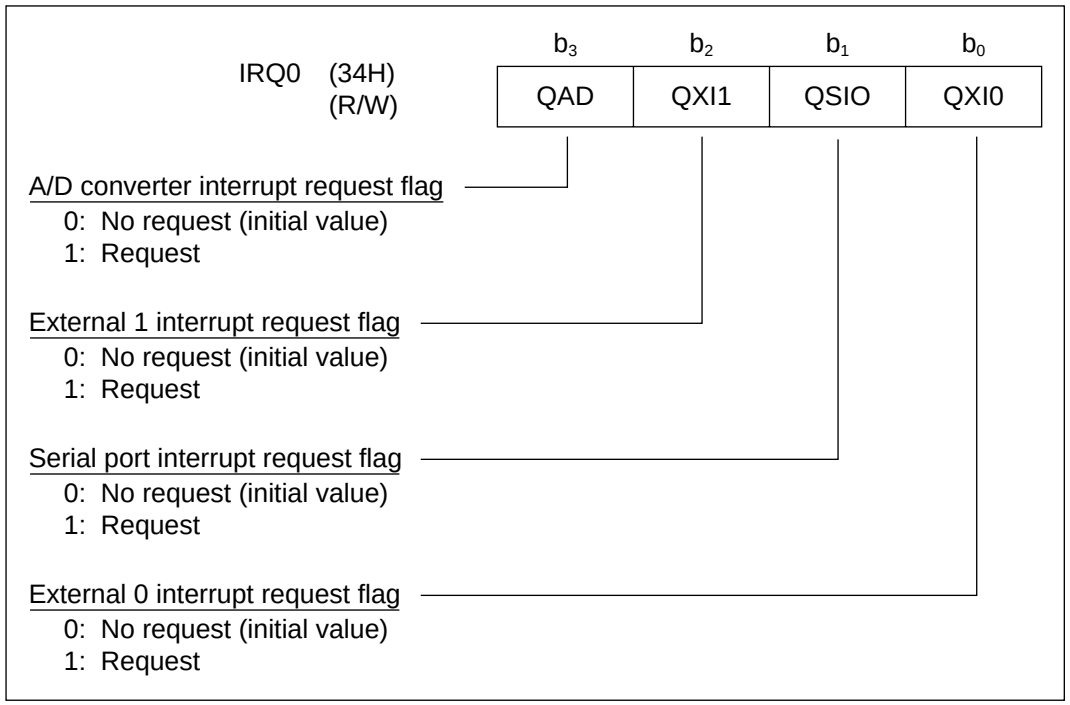
(2) The stack pointer (SP) is incremented by 4 (SP ← SP+4).

(3) The MI flag is set to "1".

4.3 Interrupt Control Registers

4.3.1 Interrupt Request Registers (IRQ0, IRQ1 and IRQ2)

Each interrupt request register (IRQ0, IRQ1 and IRQ2) is composed of a 4-bit register. When an interrupt request is generated, a corresponding bit is set to "1" in the S1 state of the first machine cycle. When an interrupt is enabled by the interrupt enable register (IE0 to 2), the interrupt is requested to the CPU. The watchdog timer interrupt does not have an interrupt mask function caused by the interrupt enable register. By writing "1" to the interrupt request register, it is possible to generate a soft interrupt. When an interrupt is received, the corresponding bits of IRQ0, IRQ1 and IRQ2 are reset to "0" by hardware. IRQ0, IRQ1 and IRQ2 are initialized to 0H at system reset.



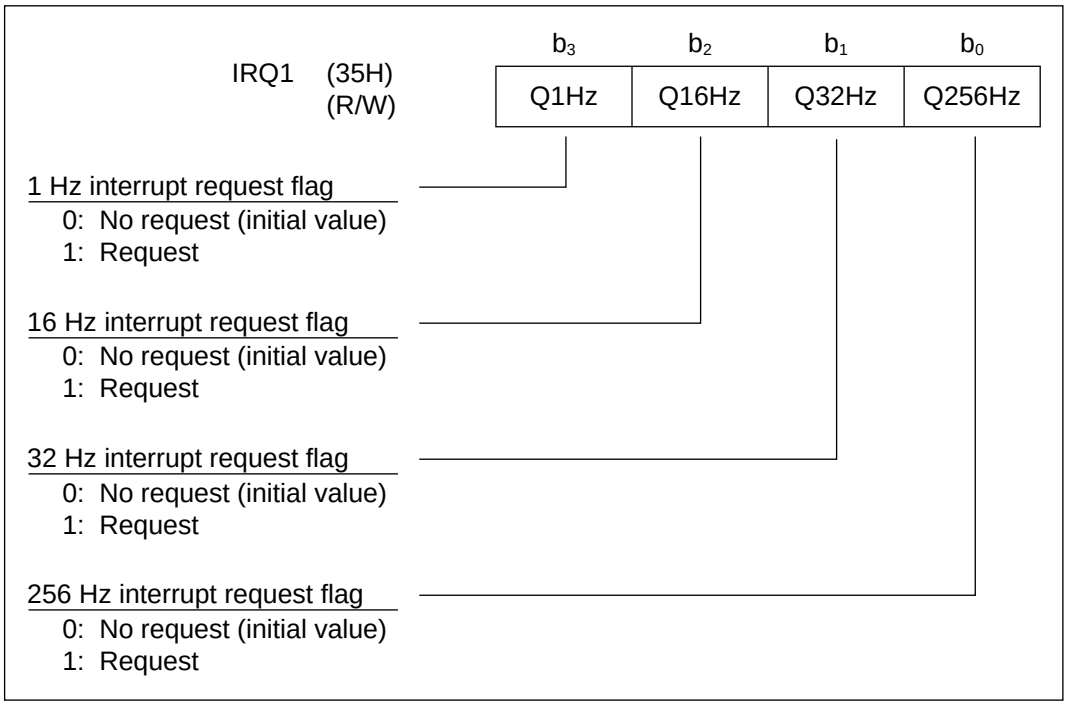
Bit 3: QAD

This bit is set to "1" by the counter overflow signal of the A/D converter.

Bit 2: QXI1
This bit is set to "1" by the change of input level of P0.0 to P0.3.

Bit 1: QSIO
This bit is set to "1" when data transfer of 8 bits of the serial port is finished.

Bit 0: QXI0
This bit is set to "1" by the change of input level of P2.0 to P.2.3, P3.0 to P3.3 and P4.0 to P4.3.

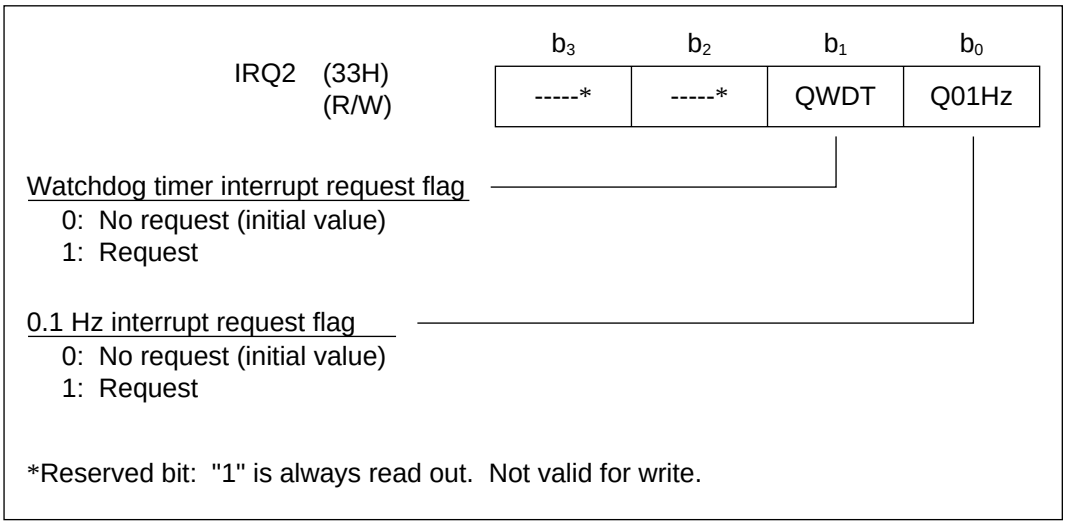


Bit 3: Q1Hz
This bit is set to "1" by falling of the 1 Hz output of the time base counter.

Bit 2: Q16Hz
This bit is set to "1" by falling of the 16 Hz output of the time base counter.

Bit 1: Q32Hz
This bit is set to "1" by falling of the 32 Hz output of the time base counter.

Bit 0: Q256Hz
This bit is set to "1" by falling of the 256 Hz output of the time base counter.



Bit 1: QWDT
This bit is set to "1" by overflow of the watchdog timer. Interrupt disable cannot be allowed by the interrupt enable register.

Bit 0: Q01Hz
This bit is set to "1" by falling of the 0.1 Hz output of the time base counter.

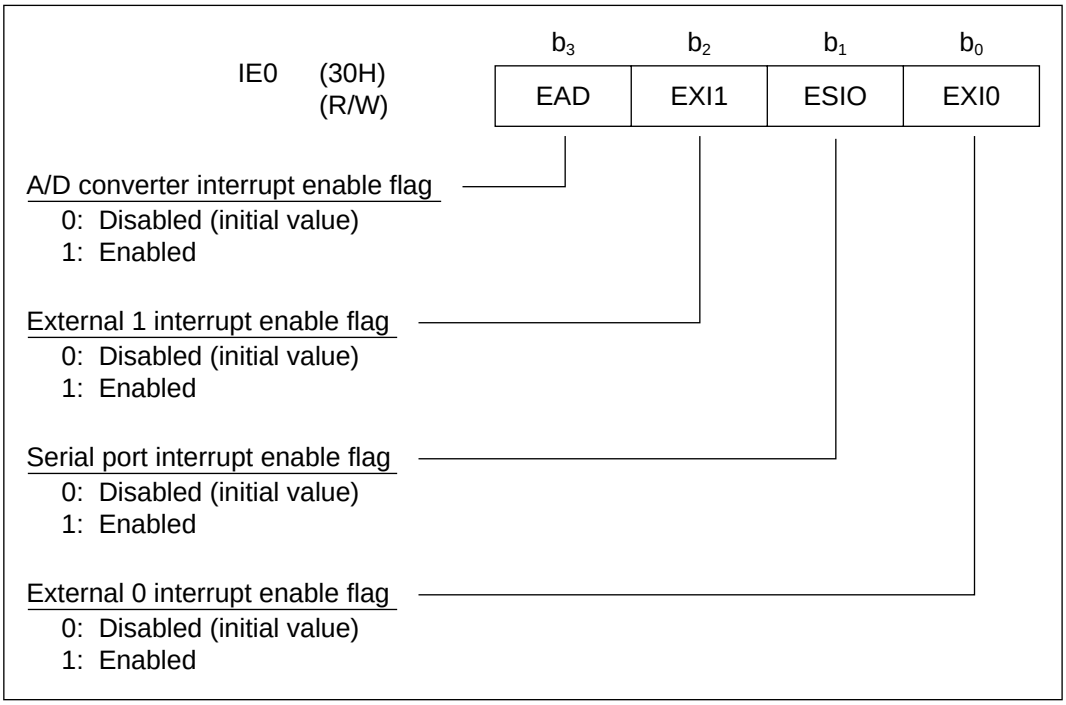
4.3.2 Interrupt Enable Registers (IE0, IE1 and IE2)

Each interrupt enable register (IE0, IE1 and IE2) is composed of a 4-bit register and determines whether a request is sent to the CPU or not by AND with a corresponding bit of the interrupt request registers (IRQ0, IRQ1 and IRQ2).

When multiple interrupts are requested to the CPU, those interrupts with higher priority (higher vector address) as shown in Table 4-1 are processed first and the interrupts with lower priority are held up during that time.

Although the master interrupt enable flag (MI) is cleared to "0" during an interrupt transition cycle, each bit of IE0 to IE2 is not cleared.

The interrupt enable registers (IE0 to 2) can be rewritten only when the master interrupt enable flag (MI) is reset to "0".



IE1 (31H) (R/W)

b_3	b_2	b_1	b_0
E1Hz	E16Hz	E32Hz	E256Hz

1 Hz interrupt enable flag
- 0: Disabled (initial value)
- 1: Enabled

16 Hz interrupt enable flag
- 0: Disabled (initial value)
- 1: Enabled

32 Hz interrupt enable flag
- 0: Disabled (initial value)
- 1: Enabled

256 Hz interrupt enable flag
- 0: Disabled (initial value)
- 1: Enabled

IE2 (32H) (R/W)

b_3	b_2	b_1	b_0
-----*	-----*	-----*	E01Hz

0.1 Hz interrupt enable flag
- 0: Disabled (initial value)
- 1: Enabled

*Reserved bit: "1" is always read out. Not valid for write.

4.3.3 Master Interrupt Enable Register (MIEF)

The MI flag of the master interrupt enable register (MIEF) is to control disabling/enabling of all the interrupts excepting watchdog timer interrupt. When set to "1", interrupt is enabled and when set to "0", interrupt is disabled.

When an interrupt is received, the MI flag is reset to "0" during the interrupt transition cycle and is set to "1" by executing the RTI instruction which is a return instruction from the interrupt process routine.

It is also possible to do multiple interrupt processing by setting this flag to "1" during an interrupt process routine.

MIEF (7CH) (R/W)

b_3	b_2	b_1	b_0
-----*	-----*	-----*	MI

Master interrupt enable flag
- 0: Interrupt disabled (initial value)
- 1: Interrupt enabled

*Reserved bit: "1" is always read out. Not valid for write.

Table 4-2 shows the list of interrupt-related registers.

Table 4-2 List of Interrupt Related Registers

Register name	Symbol	Address	Read/Write	Byte access	Value at system reset
Interrupt enable register 0	IE0	30H	R/W	Yes	0H
Interrupt enable register 1	IE1	31H	R/W		0H
Interrupt enable register 2	IE2	32H	R/W	Yes	0EH
Interrupt request register 2	IRQ2	33H	R/W		0CH
Interrupt request register 0	IRQ0	34H	R/W	Yes	0H
Interrupt request register 1	IRQ1	35H	R/W		0H
Master interrupt enable register	MIEF	7CH	R/W	No	0EH

Chapter 5

Clock Generation Circuit (2CLK)

Chapter 5 Clock Generation Circuit (2CLK)

5.1 Overview

The clock generation circuit (2CLK) of the ML64168 is composed of a 32.768 kHz crystal oscillation circuit, a 700 kHz RC oscillation circuit and a clock control part. It generates the system clock (CLK) and the time base clock (32.768 kHz).

The system clock is the basic operation clock of the CPU while the time base clock is the basic operation clock of the time base counter and the buzzer driver.

By the contents of the frequency control register (FCON) the system clock can be switched at between 32.768 kHz which is output of the crystal oscillation circuit and 700 kHz which is output of the RC oscillation circuit.

Note: The oscillation frequency of the RC oscillation circuit varies depending on the value of external resistance (R_{OS}), operating power supply voltage (V_{DD}) and ambient temperatures (Ta). In this manual, the output of the RC oscillation circuit is taken as 700 kHz for convenience.

5.2 Layout of Clock Generation Circuit

Figure 5-1 shows layout of the clock generation circuit.

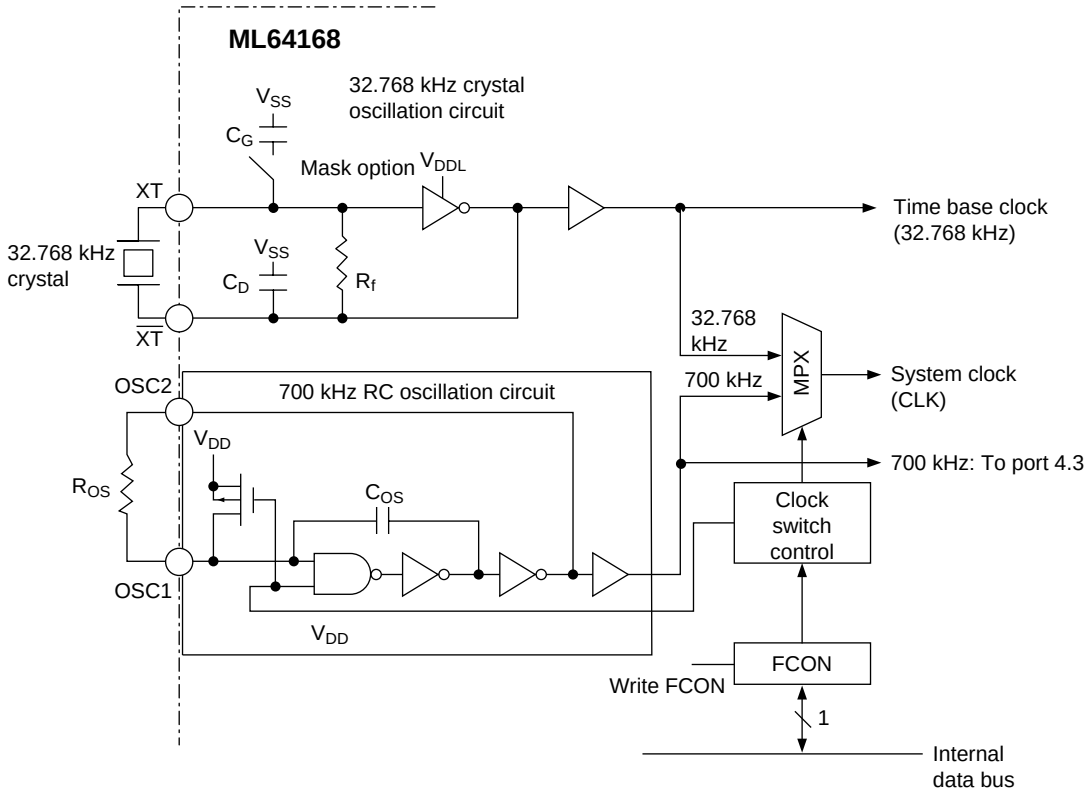


Figure 5-1 Layout of Clock Generation Circuit

5.3 Operation of Clock Generation Circuit

The 32.768 kHz crystal oscillation circuit oscillates by installing a 32.768 kHz crystal externally. When micro-tuning the 32.768 kHz frequency by an external capacitor, the built-in capacitance (C_G) can be cut off by selecting a mask option.

The 700 kHz oscillation circuit oscillates by installing a resistance (R_{OS}) externally. The RC oscillation circuit operates only when the system clock is set to the 700 kHz RC oscillation clock or when it is set to CPU clock output mode for high speed system clock by test functions. Otherwise it halts oscillation. For details of the test functions, refer to Chapter 15 "Test Circuit".

Selection of the system clock is performed by the frequency control register (FCON). When Bit 0 of FCON (CPUCLK) is reset to "0", output of the crystal oscillation circuit (32.768 kHz) becomes the system clock and when CPUCLK is set to "1", output of the RC oscillation circuit (700 kHz) becomes the system clock. Even though the 700 kHz oscillation circuit is selected, the crystal oscillation circuit is not halted.

When the crystal oscillation circuit is chosen as the system clock, oscillation of the RC oscillation circuit is halted and power consumption of the RC oscillation circuit becomes "0". Consequently, it is possible to lower power consumption by writing software in such a way that output of the RC oscillation circuit is selected (CPUCLK = 1) only when high speed operation is needed and that output of the crystal oscillation circuit (CPUCLK = 0) is selected otherwise.

Since the OSC1 pin is pulled up to V_{DD} when the 700 kHz RC oscillation circuit is not selected, leave OSC1/OSC2 open when not using output from the RC oscillation circuit (700 kHz).

5.4 Frequency Control Register (FCON)

The frequency control register (FCON) is a 4-bit special function register (SFR) to select a system clock.

FCON (09H) (R/W)

b_3	b_2	b_1	b_0
-----*	-----*	-----*	CPUCLK

System clock selection
- 0: Cyrstal oscillation output (initial value)
- 1: 700 kHz RC oscillation output

*Reserved bit: "1" is always read out. Not valid for write.

Bit 0: CPUCLK
This bit is to select a system clock. At system reset, it is reset to "0" and the crystal oscillation output is selected.

5.5 System Clock Switch Timing

When the CPUCLK bit of the frequency control register (FCON) is set to "1", the system clock is switched from crystal oscillation output (32.768 kHz) to RC oscillation output (700 kHz) and the internal logic power supply is switched from the V_{DDL} level to the applied power supply voltage level (V_{DD}) simultaneously.

Figure 5-2 shows the system clock switch timing and the internal logic power supply.

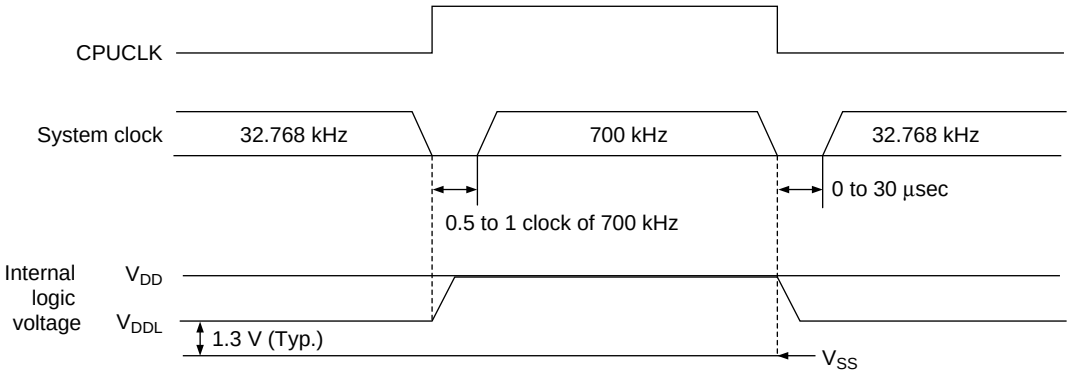


Figure 5-2 System Clock Switch Timing

Table 5-1 shows the clock generation circuit related pins. Table 5-2 shows typical values of oscillation frequencies of the RC oscillation circuit.

Table 5-1 Clock Generation Circuit-Related Pins

Pin name	Pin No.		Pad No.	Input/ Output	Note
	GP	GA, TB			
XT	69	67	67	Input	Low speed side clock oscillation input pin: This pin is connected to the crystal oscillator (32.768 kHz).
$\overline{XT}$	68	66	66	Output	Low speed side clock oscillation output pin: This pin is connected to the crystal oscillator (32.768 kHz).
OSC1	66	64	64	Input	High speed side clock oscillation pin: This pin is connected to the external resistance (R_{OS}) for oscillation.
OSC2	65	63	63	Output	

Table 5-2 Typical Values of Oscillating Frequencies of RC Oscillation Circuit (Ta = 25°C)

V_{DD} (V)	R_{OS} (kΩ)	f_{OSC} (kHz)
3.0	60	700
1.5	160	280

Chapter 6

Time Base Counter (TBC)

Chapter 6 Time Base Counter (TBC)

6.1 Overview

The ML64168 has a built-in time base counter (TBC) that generates clocks to be supplied to internal peripheral circuits. The time base counter is composed of 15 binary counters and a 1/10 frequency dividing circuit. The count clock of the time base is supplied with the oscillation clock (32.768 kHz) of the crystal oscillation circuit. Output of the time base counter is used for the buzzer driver, the system reset circuit, the watchdog timer, the time base interrupt, sampling clocks of each port and the capture circuit.

6.2 Layout of Time Base Counter

Figure 6-1 shows the layout of the time base counter (TBC).

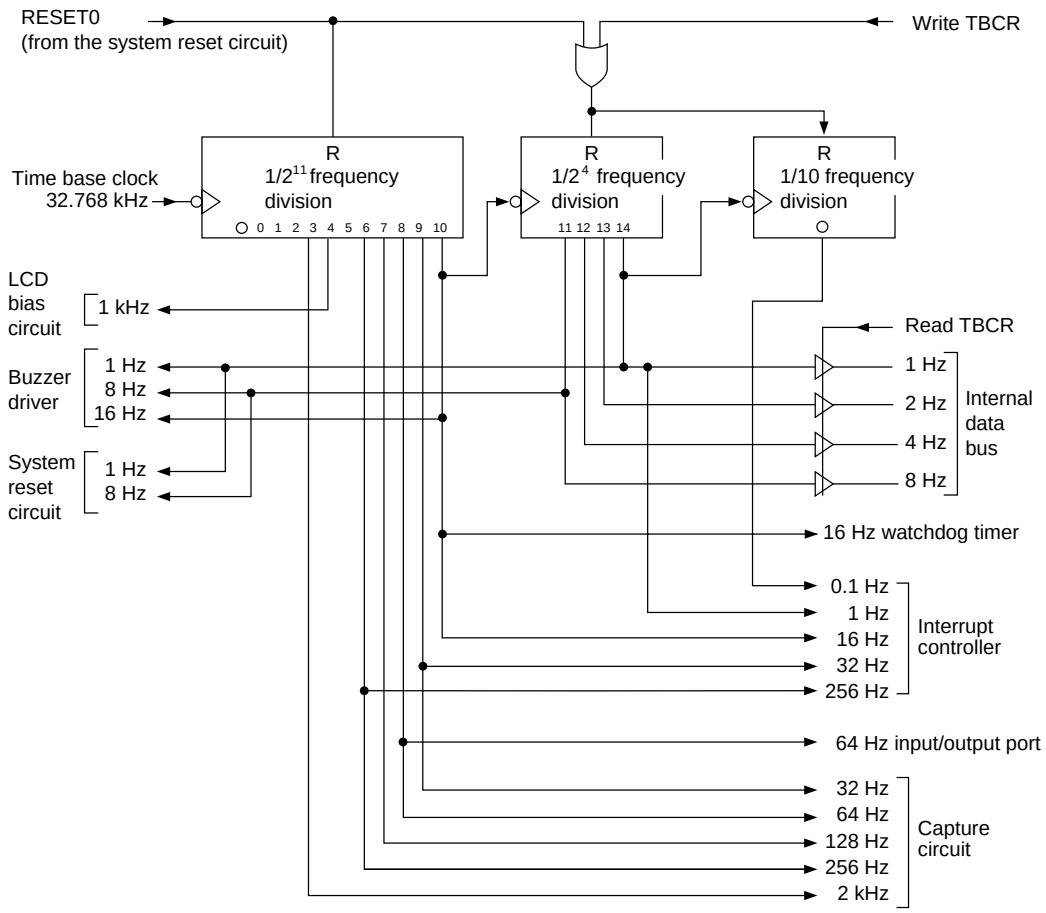


Figure 6-1 Layout of Timer Base Counter

6.3 Operation of Time Base Counter

The time base counter (TBC) starts count-up from 0000H after system reset. Count-up is started by falling of the time base clock (32.768 kHz).

256 Hz/32 Hz/16 Hz/1 Hz/0.1 Hz output of the time base counter is used as the timer base interrupt and a time base interrupt request is generated at falling of each output.

The 16 Hz output of the time base counter is output to the watchdog timer. The output of 1 Hz/8 Hz/16 Hz is used by the buzzer driver and various buzzer sounds are output. The 64 Hz output is used as a sampling clock of input ports. The 1 Hz/8 Hz output is input to the system reset circuit and is used to generate reset timing at system reset and to switch a logic power supply. The output of 256 Hz/128 Hz/64 Hz/32 Hz becomes input data for the capture circuit.

The output of 1 Hz/2 Hz/4 Hz/8 Hz of the time base counter can be read by the time base counter register (TBCR). When a write operation is performed on TBCR, the counters of 0.1 Hz/1 Hz/2 Hz/4 Hz/8 Hz are reset to "0".

Figure 6-2 shows interrupt timing of the time base counter and reset timing by writing to TBCR.

Note: Output of 8 Hz to 1 Hz of the time base counter can be read by the time base counter register (TBCR) and they are reset to "0" by writing to TBCR. In this write operation, data to write have no significance. For example, writing by the "LMAD TBCR" instruction does not depend on the contents of the A register at all. When writing to TBCR and resetting 8 Hz to 1 Hz of the time base counter, a time base interrupt is generated when each output is "1". For example, when the 1 Hz output is "1", a 1 Hz interrupt request is generated. When an interrupt is invalidated, please write to TBCR and reset the interrupt request flag (Q1Hz) to "0" after resetting the master interrupt enable flag (MI) or the interrupt enable flag (E1Hz) to "0".

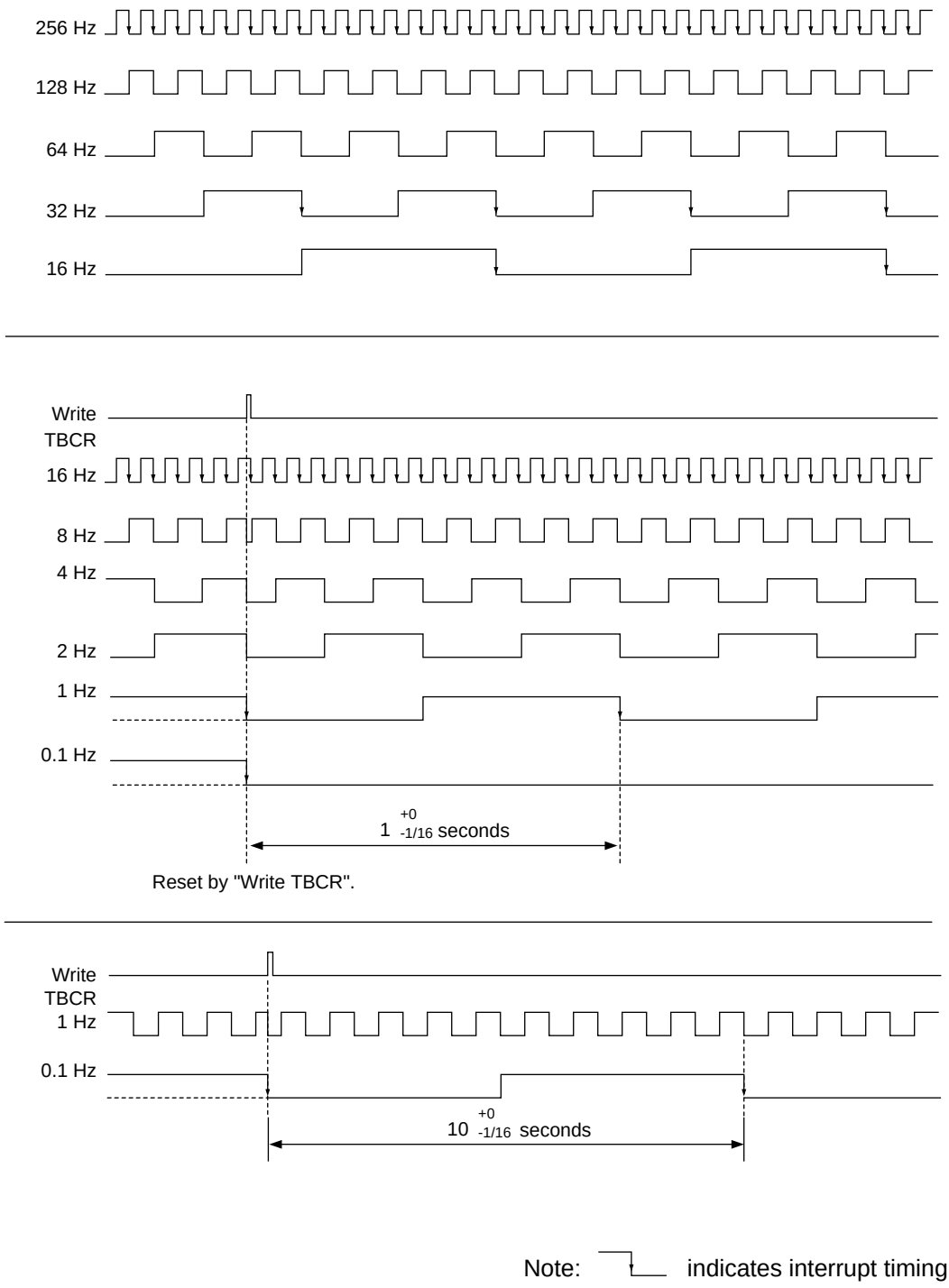
6.4 Time Base Counter Register (TBCR)

This register is a 4-bit special function register (SFR) to read 8 Hz to 1 Hz output of the time base counter. When writing, it resets the 8 Hz to 1 Hz output and the 0.1 Hz output.

TBCR (0FH) (R/W)

b_3	b_2	b_1	b_0
1Hz	2Hz	4Hz	8Hz

Values of 8 Hz to 1 Hz of the time base counter



Note: ⌐¬ indicates interrupt timing.

Figure 6-2 Time Base Counter Interrupt Timing and Reset Timing by TBCR Writing

Chapter 7

Ports (P0, P1, P2, P3 and P4)

Chapter 7 Ports (P0, P1, P2, P3 and P4)

7.1 Overview

The ML64168 has one 4-bit input port, three 4-bit input/output ports and one 4-bit output port built-in.

Table 7-1 shows the list of functions of each port. For secondary functions of the capture timer, the A/D converter and the serial port, refer to Chapter 10 "Capture Circuit", Chapter 12 "A/D Converter", and Chapter 8 "Serial Port", respectively.

Table 7-1 List of Functions of Each Port

Pin name	Pin No.		Pad No.	Input/ Output	Function
	GP	GA, TB			
P0.0	77	75	75	Input	4-bit input port (P0): Can select (1) pull-up resistance input, (2) pull-down resistance input or (3) high-impedance input by the port 01 control register (P01CON). As a secondary function, P0.0 to P0.3 are assigned external interrupt functions and P0.0 and P0.1 are assigned a capture trigger function.
P0.1	78	76	76	Input	
P0.2	79	77	77	Input	
P0.3	80	78	78	Input	
P1.0	73	71	71	Output	4-bit output port (P1): Can select NMOS open drain output or CMOS output by the port 01 control register (P01CON). P1.0 is a large current drive output port.
P1.1	74	72	72	Output	
P1.2	75	73	73	Output	
P1.3	76	74	74	Output	
P2.0	18	16	16	Input/Output	4-bit input/output port (P2): Selection of (1) pull-up/pull-down resistance input, (2) high-impedance input, (3) NMOS open drain output and (4) CMOS output by the port 2 control registers 0 to 3 (P20CON to P23CON) is possible. As a secondary function, an external interrupt function is assigned.
P2.1	19	17	17	Input/Output	
P2.2	20	18	18	Input/Output	
P2.3	21	19	19	Input/Output	
P3.0	22	20	20	Input/Output	4-bit input/output port (P3): Selection of (1) pull-up/pull-down resistance input, (2) high-impedance input, (3) NMOS open drain output and (4) CMOS output by the port 3 control registers 0 to 3 (P30CON to P33CON) is possible. As a secondary function, P3.0 to P3.3 are assigned an external interrupt function and P3.3 is assigned a serial port function.
P3.1	23	21	21	Input/Output	
P3.2	24	22	22	Input/Output	
P3.3/SIN	25	23	23	Input/Output	
P4.0/SOUT	26	24	24	Input/Output	4-bit input/output port (P4): Selection of (1) pull-up/pull-down resistance input, (2) high-impedance input, (3) NMOS open drain output and (4) CMOS output by the port 4 control registers 0 to 3 (P40CON to P43CON) is possible. As a secondary function, P4.0 to P4.3 are assigned an external interrupt function, P4.0 to P4.2 are assigned a serial port function and P4.3 is assigned a monitor function of the RC oscillation clock for A/D conversion.
P4.1/SPR	27	25	25	Input/Output	
P4.2/SCLK	28	26	26	Input/Output	
P4.3/MON	29	27	27	Input/Output	

7.2 Port 0 and Port 1 (P0.0 to P0.3 and P1.0 to P1.3)

7.2.1 Layout of Port 0 and Port 1

Port 0 is a 4-bit input only port. Port 0 can be switched to either pull-up resistance input, pull-down resistance input or high-impedance input by the port 01 control register (P01CON). As a secondary function, an external interrupt function is assigned by level change. P0.0 and P0.1 are also assigned as trigger input pins of the capture circuit. For details of the capture circuit, refer to Chapter 10 "Capture Circuit".

Port 1 is a 4-bit output only port. Port 1 can be switched to either CMOS output or NMOS open drain output by the port 01 control register (P01CON).

Figure 7-1 shows the layout of Port 0 and Port 1.

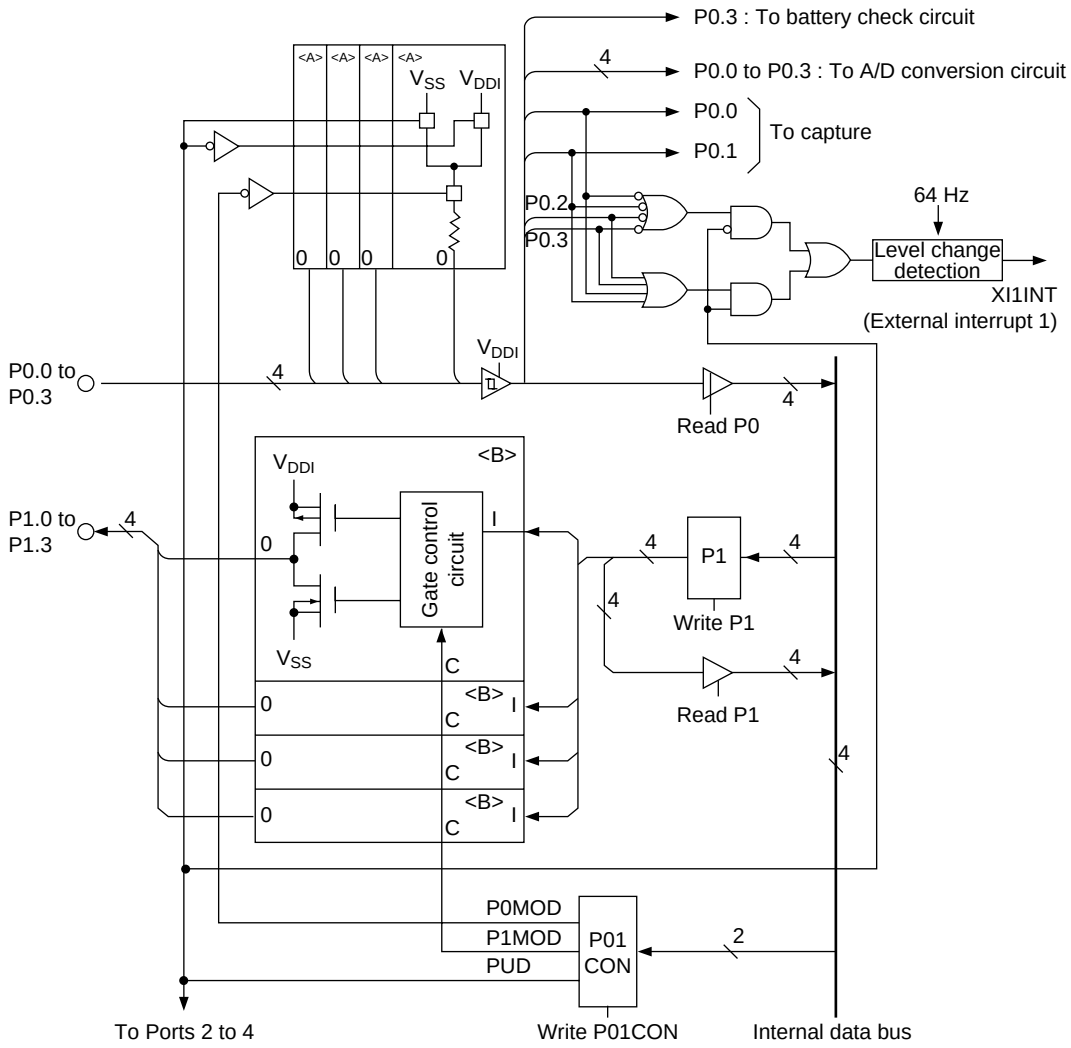


Figure 7-1 Layout of Port 0 and Port 1

The power supply for the input circuit of Port 0 and the output circuit of Port 1 is at V_{DDI}–V_{SS} level. When connecting Port 0 and Port 1 to equipment operated by a different power supply externally, supply power to the external equipment between the V_{DDI}–V_{SS} pins is shown in Figure 7-2.

When all the signal levels of all the ports of Port 0, Port 1 and Ports 2 to 4 can be the same as the power supply voltage of the IC, connect the V_{DDI} pin to V_{DD}.

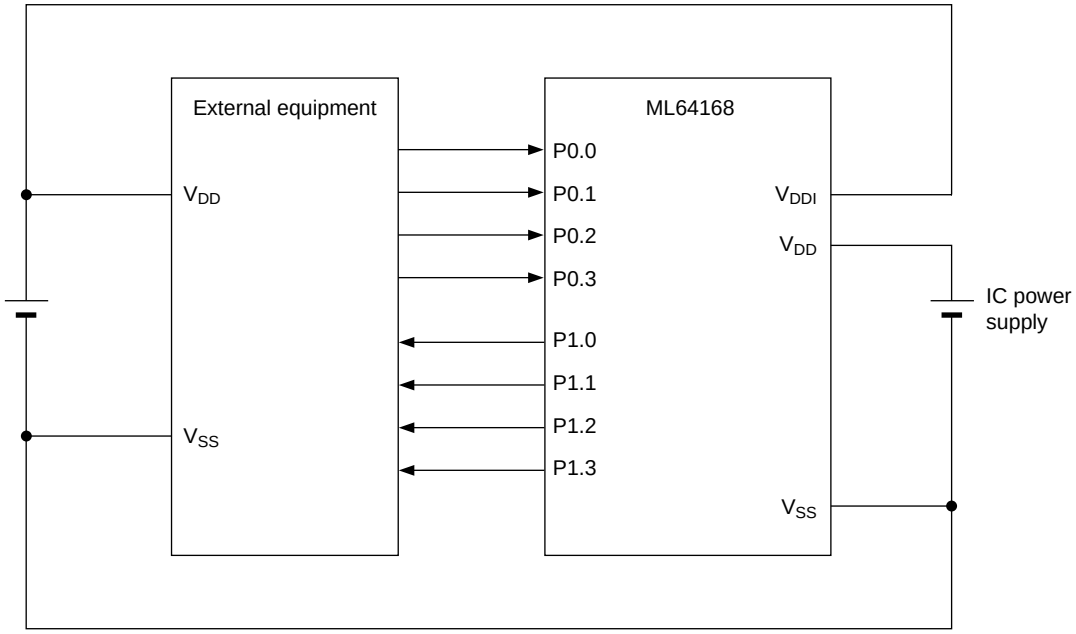


Figure 7-2 Connection of Port 0 and Port 1 to External Equipment with Different Power Supply

7.2.2 Registers Related to Port 0 and Port 1

(1) Port 0 register (P0)

The port 0 register is a 4-bit read only special function register (SFR) to read out the level of each port of Port 0.

P0 (03H) (R)

b_3	b_2	b_1	b_0
P03	P02	P01	P00

Pin level of each bit of Port 0
0: "L" level
1: "H" level

(2) Port 1 register (P1)

The port 1 register is a 4-bit special function register (SFR) to set the output value of Port 1.

P1 (04H) (R/W)

b_3	b_2	b_1	b_0
P13	P12	P11	P10

At system reset, P1 is reset to "0".

When writing data to the port 1 register, actual timing of the change of the pin is the second half of State 3 of the last machine cycle of the write instruction. Figure 7-3 shows an example of varying timing of the port.

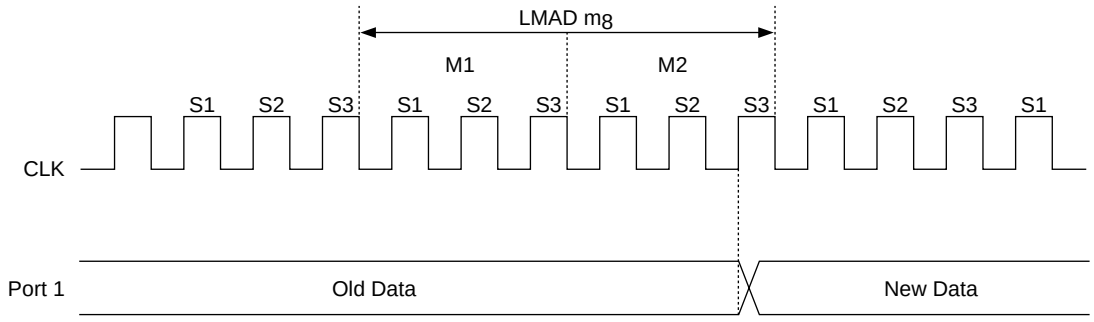


Figure 7-3 Example of Writing to Port Data Register by "LMAD m8" Instruction

When data is read from the port, the data is taken in the accumulator (A Register) or the BA register pair at the latter half of the state 2 (S2) of the last machine cycle of the read instruction.

Figure 7-4 shows an example of timing.

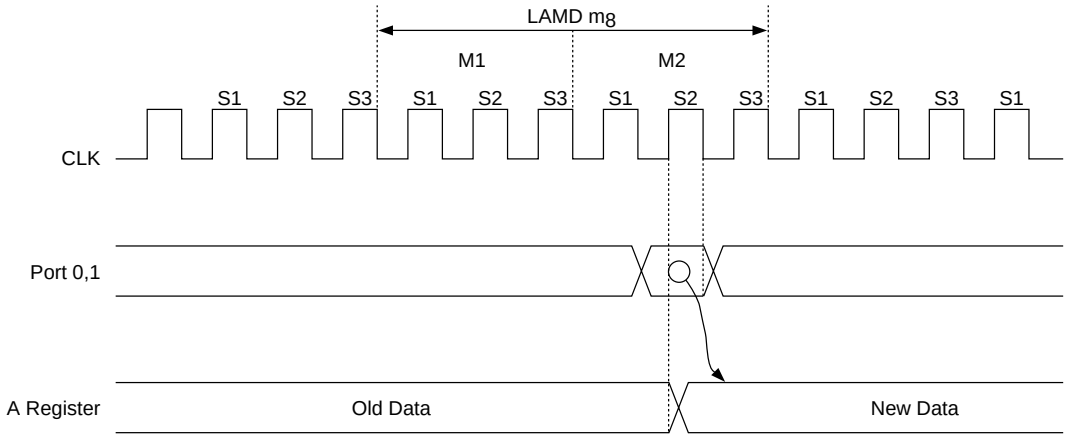
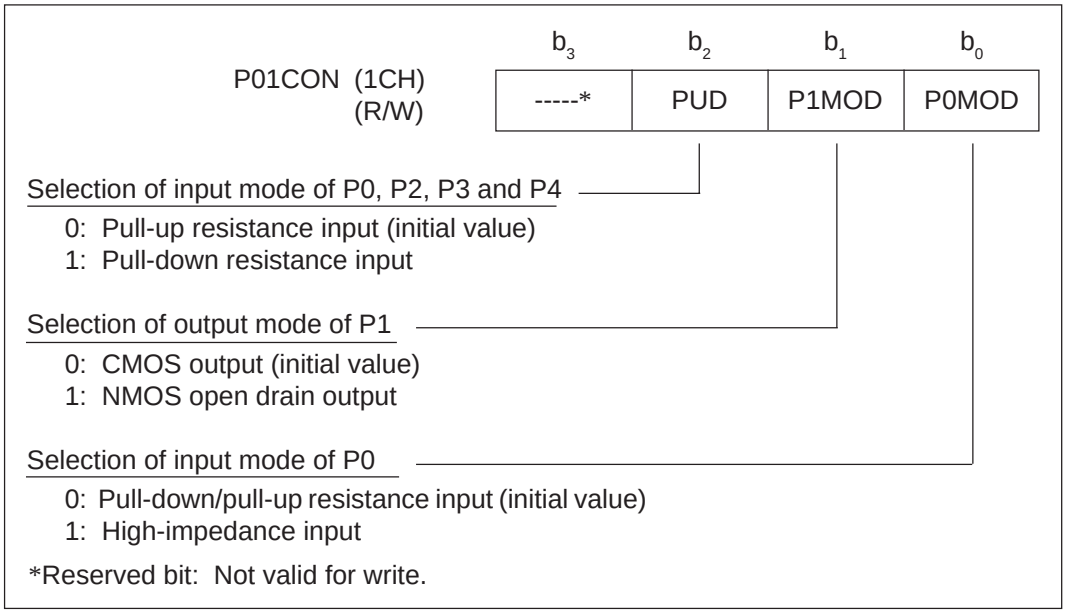


Figure 7-4 Example of Reading the Data from the Port by the "LAMD mg" Instruction

(3) Port 01 control register (P01CON)

The Port 01 control register (P01CON) is a 4-bit special function register (SFR) to control input mode of Port 0, output mode of Port 1 and pull-down/pull-up resistance input when Ports 2 to 4 are selected as input. Since P01CON is a write-only register, bit manipulation and increment/decrement instructions cannot be used.



Bit 2: PUD
This bit is to select a pull-down/pull-up resistance when P0MOD is reset to "0" and Port 0 is selected as pull-down/pull-up resistance input. When PUD is reset to "0", Port 0 becomes pull-up resistance input and when PUD is set to "1", Port 0 becomes pull-down resistance input. When Ports 2 to 4 are set as input and pull-down/pull-up resistance input, PUD can select either pull-up resistance input or pull-down resistance input. At system reset, PUD is reset to "0".

Note: Input setting of Ports 2 to 4 and selection of pull-down/pull-up resistance input can be done by resetting the DIR bits and the MOD bits of the control registers of Ports 2 to 4 (P20CON to P23CON, P30CON to P33CON and P40CON to P43CON).

It is not possible to specify pull-up resistance input and pull-down resistance input of Port 0 and Ports 2 to 4 separately.

Bit 1: P1MOD
This bit is to select output mode of Port 1. By resetting P1MOD to "0", Port 1 becomes CMOS output and by setting P1MOD to "1", Port 1 becomes NMOS open drain output. At system reset, P1MOD is reset to "0". (It is not possible to control P1.0 to P1.3 separately.)

Bit 0: P0MOD
This bit is to select input mode of Port 0. By resetting P0MOD to "0", Port 0 becomes pull-down/pull-up resistance input and by setting P0MOD to "1", Port 0 becomes high-impedance input. When selecting pull-down/pull-up resistance input, either pull-down resistance input or pull-up resistance input is selected by the PUD bit. At system reset, P0MOD is reset to "0". (It is not possible to control P0.0 to P0.3 separately).

7.2.3 External Interrupt Generation Timing of Port 0

External interrupt generation of Port 0 is triggered by the falling of the 64 Hz output of the time base counter which is the sampling clock.

Delay time until the External 1 interrupt request flag (QXI1) is set after the level of P0.n is changed to output XI1INT signal is a maximum period of 64 Hz (15.625 ms). Since the External 1 interrupt request flag (QXI1) is set by level change of OR signal of Port 0 ports, which port the interrupt request comes from is judged by reading out Port 0.

The External 1 interrupt is generated by OR of P0.0 to P0.3. When the PUD bit is set to "1", the External 1 interrupt is generated when (1) input to all the ports is set to the "L" level when all the ports is in "H" and (2) input to any one of the ports is set to the "H" level when all the ports is in "L".

When the PUD bit is reset to "0", the External 1 interrupt is generated when (1) input to any one of the ports is set to the "L" level when all the ports is in "H" and (2) input to all the ports is set to the "H" level when all the ports is in "L".

The interrupt vector address of the External 1 interrupt is address 032H.

Figure 7-5 shows the generation circuit of External 1 interrupt. Figure 7-6 and Figure 7-7 show generation timing of the External 1 interrupt according to the PUD bit.

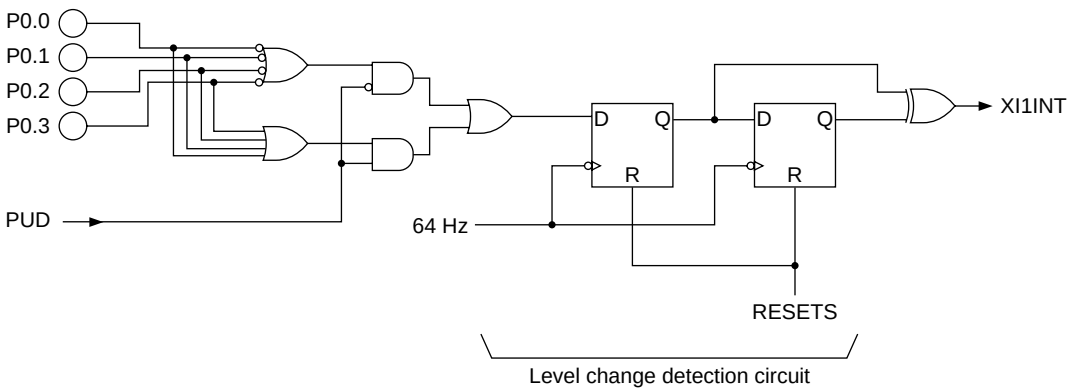


Figure 7-5 External 1 Interrupt Generation Circuit

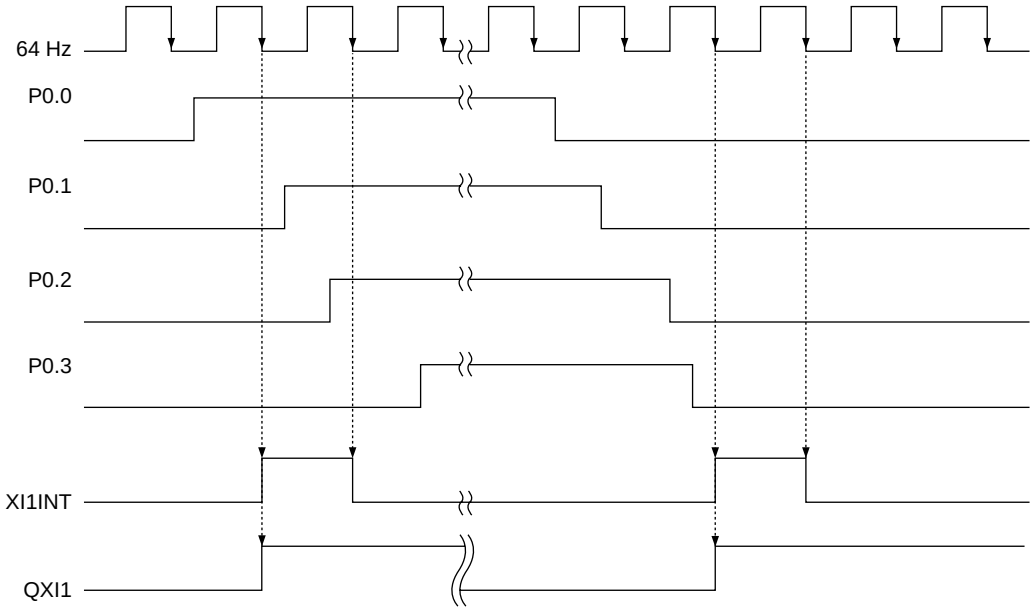


Figure 7-6 External 1 Interrupt Generation Timing (When PUD = "1")

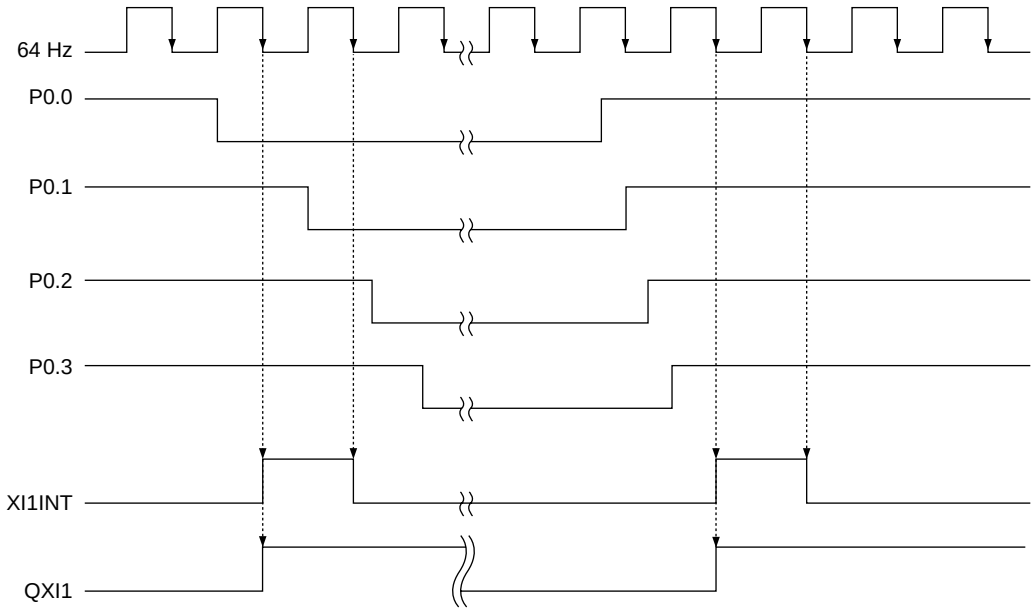


Figure 7-7 External 1 Interrupt Generation Timing (When PUD ="0")

7.3 Port 2, Port 3 and Port 4 (P2.0 to P2.3, P3.0 to P3.3 and P4.0 to P4.3)

7.3.1 Layout of Port 2, Port 3 and Port 4

Ports 2 to 4 are 4-bit input/output ports. Each bit can be switched to either pull-up resistance input/pull-down resistance input, high-impedance input, CMOS output or NMOS open drain output by the Control registers of Ports 2 to 4 (P20CON to P23CON, P30CON to P33CON and P40CON to P43CON). Pull-up resistance input or pull-down resistance input can be selected by the PUD bit of the Port 01 control register (P01CON).

These ports are assigned an external interrupt function by level change as a secondary function. A serial port input/output function is assigned for P3.3, P4.0 to P4.2 and a monitor function of the RC oscillation clock is assigned for P4.3. For details of the serial port input/output functions and the monitor functions of the RC oscillation clock, refer to Chapter 8 "Serial Port", Chapter 12 "A/D Converter" and Chapter 15 "Test Circuit".

Figure 7-8 shows the layout of Port 2, Port 3 and Port 4.

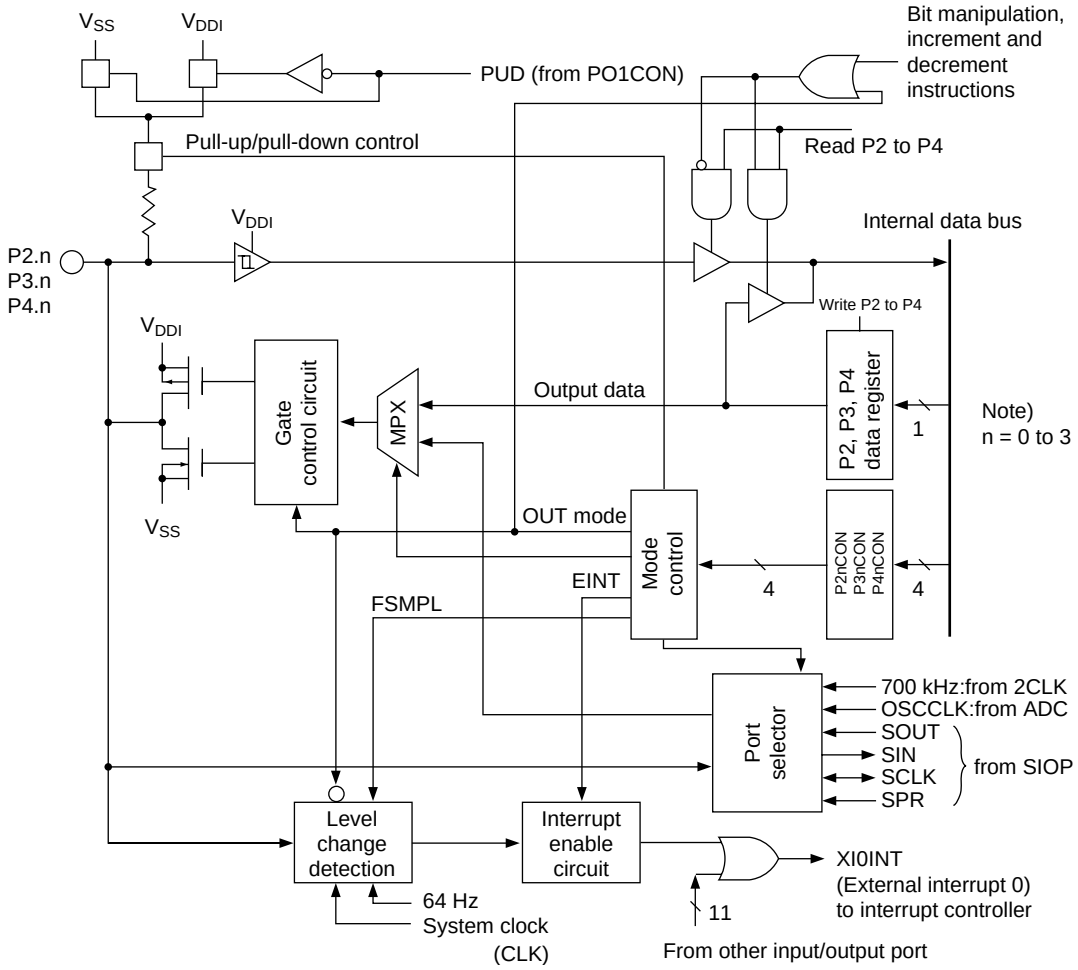


Figure 7-8 Layout of Port 2, Port 3 and Port 4

The power supply of Port 2, Port 3 and Port 4 is at the V_{DDI}–V_{SS} level. When connecting Ports 2 to 4 to external equipment operated by a different power supply, please supply the power of the external equipment to the V_{DDI}–V_{SS} pins, as shown in Figure 7-9.

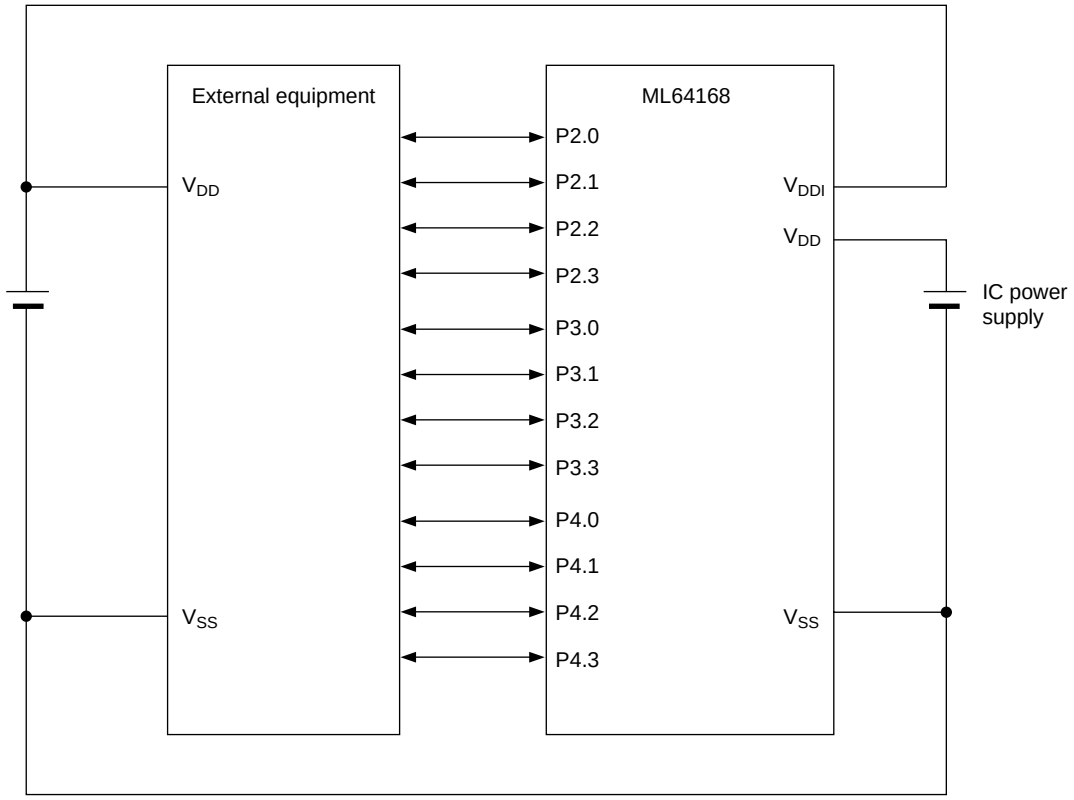


Figure 7-9 Connection of Ports 2 to 4 to External Equipment of Different Power Supply

When the signal level of all the ports of Port 0, Port 1 and Ports 2 to 4 can be the power supply voltage of the IC, connect the V_{DDI} pin to V_{DD}.

7.3.2 Registers Related to Port 2, Port 3 and Port 4

(1) Port 2 register (P2)

The Port 2 register is a 4-bit special function register to set the output value of the port. When bit 1 (P20DIR to P23DIR) of the Port 2 control register (P20CON to P23CON) is set to "1" to select output mode, the contents of the Port 2 register are output to the port.

When reading out P2 while output mode is selected (P20DIR to P23DIR = 1), the contents of the Port 2 register are read. However, when P2 is read while input mode is selected (P20DIR to P23DIR = 0), the pin level of Port is read out.

P2 (00H) (R/W)

b_3	b_2	b_1	b_0
P23	P22	P21	P20

(2) Port 3 register (P3)

The Port 3 register is a 4-bit special function register to set the output value of the port. When bit 1 (P30DIR to P33DIR) of the Port 3 control register (P30CON to P33CON) is set to "1" to select output mode, the contents of the Port 3 register are output to the port.

When reading out P3 while output mode is selected (P30DIR to P33DIR = 1), the contents of the Port 3 register are read. However, when P3 is read while input mode is selected (P30DIR to P33DIR = 0), the pin level of port is read out.

P3 (01H) (R/W)

b_3	b_2	b_1	b_0
P33	P32	P31	P30

(3) Port 4 register (P4)

The Port 4 register is a 4-bit special function register to set the output value of the port. When bit 1 (P40DIR to P43DIR) of the Port 4 control register (P40CON to P43CON) is set to "1" to select output mode, the contents of the Port 4 register are output to the port.

When reading out P4 while output mode is selected (P40DIR to P43DIR = 1), the contents of the Port 4 register are read. However, when P4 is read while input mode is selected (P40DIR to P43DIR = 0), the pin level of port is read out.

P4 (02H) (R/W)

b_3	b_2	b_1	b_0
P43	P42	P41	P40

It is possible to specify input/output bitwise by each Port control register for Ports 2 to 4. Consequently, depending on how each DIR bit is specified, contents of each register are read for some bits while the level of each pin are read for other bits.

At system reset, the Port 2 to Port 4 register (P2 to P4) is reset to "0".

When writing data to each register, actual timing of each pin is the second half of State 3 of the last machine cycle of the write instruction. Figures 7-10 shows an example of varying timing of the ports.

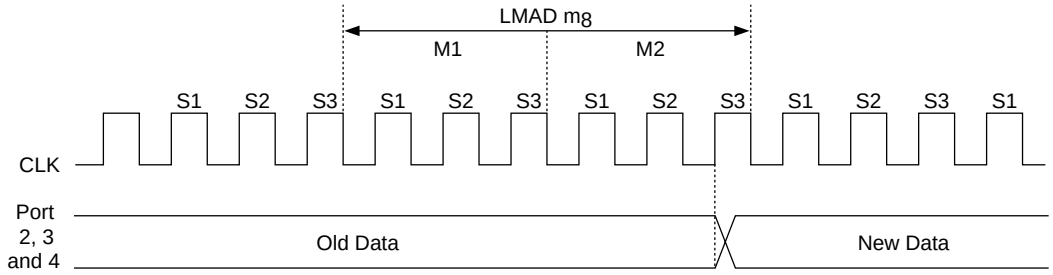


Figure 7-10 Example of Writing of Port Data Register by the "LMAD mB" Instruction

In case the data is read from the port, the data is taken in the accumulator (A Register) and the BA register pair at the latter half of the state 2 (S2) of the last machine cycle of the read instruction. Figure 7-11 shows an example of timing.

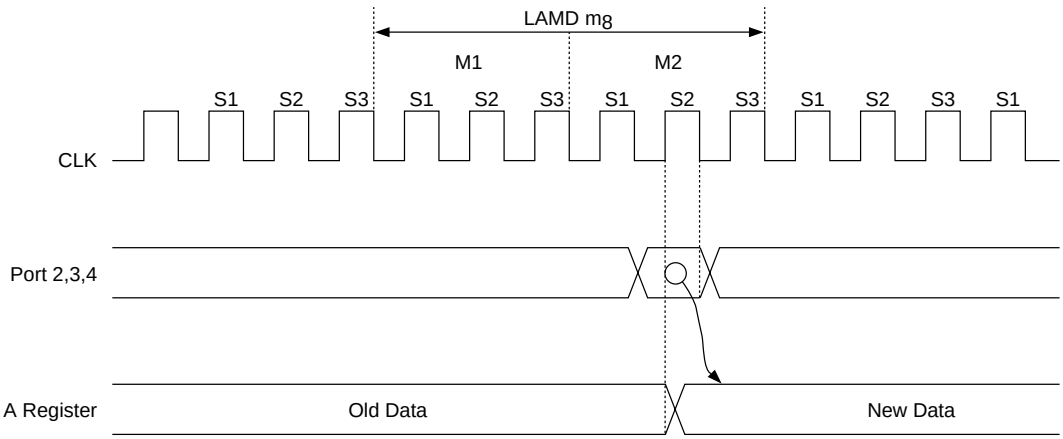


Figure 7-11 Example of Reading the Data from the Port by the "LAMD mB" Instruction

(4) Port 2 control registers (P20CON to P23CON)

The Port 2 control registers (P20CON to P23CON) are 4-bit special function registers (SFRs) to perform selection of input/output mode, selection of pull-down/pull-up resistance input or high impedance input in input mode, selection of CMOS output or NMOS open drain output in output mode, selection of external interrupt disable or enable and selection of sampling clocks of external interrupts. Since P20CON to P23CON are write-only registers, it is not possible to use bit manipulation instructions and increment/decrement instructions.

P20CON (10H) (W)

b_3	b_2	b_1	b_0
P20IE	P20F	P20DIR	P20MOD

Selection of P2.0 external interrupt disable/enable

0: Interrupt disabled (initial value)
1: Interrupt enabled

Selection of P2.0 external interrupt sampling clock

0: 64 Hz (initial value)
1: System clock

Selection of P2.0 input/output mode

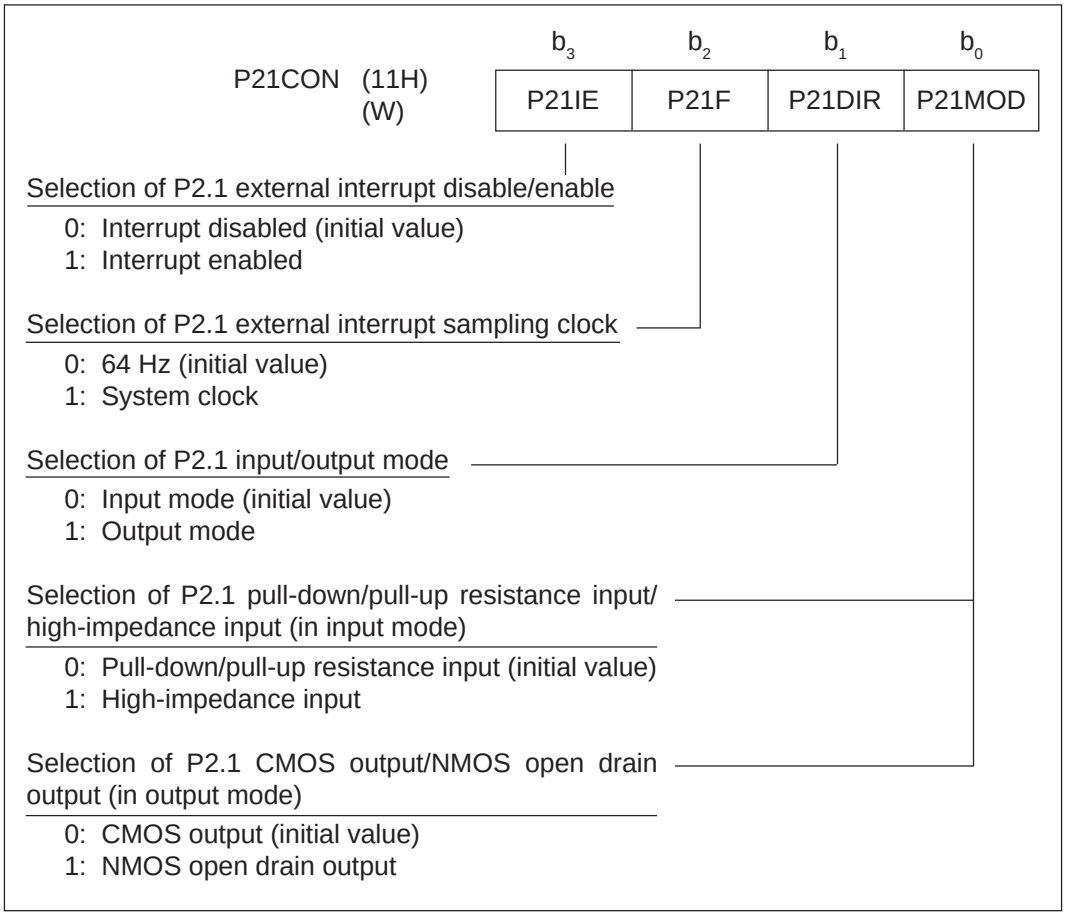
0: Input mode (initial value)
1: Output mode

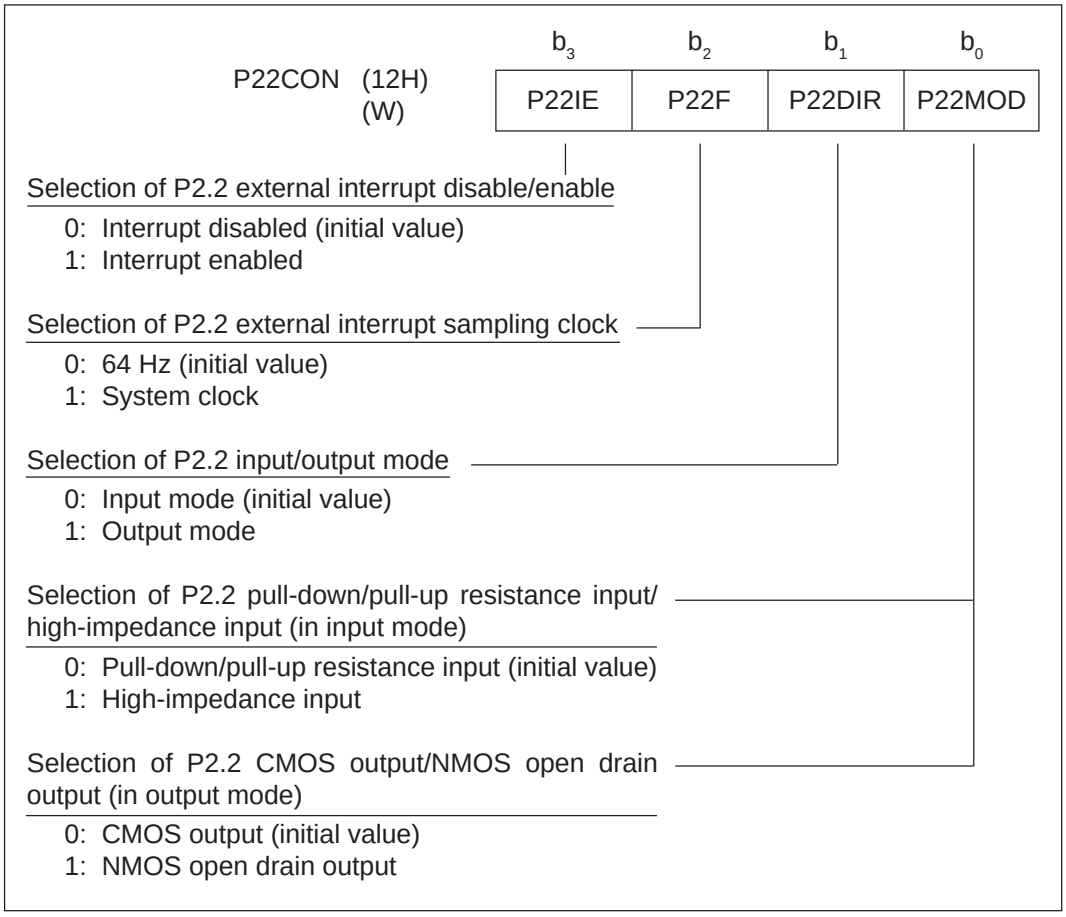
Selection of P2.0 pull-down/pull-up resistance input/ high-impedance input (in input mode)

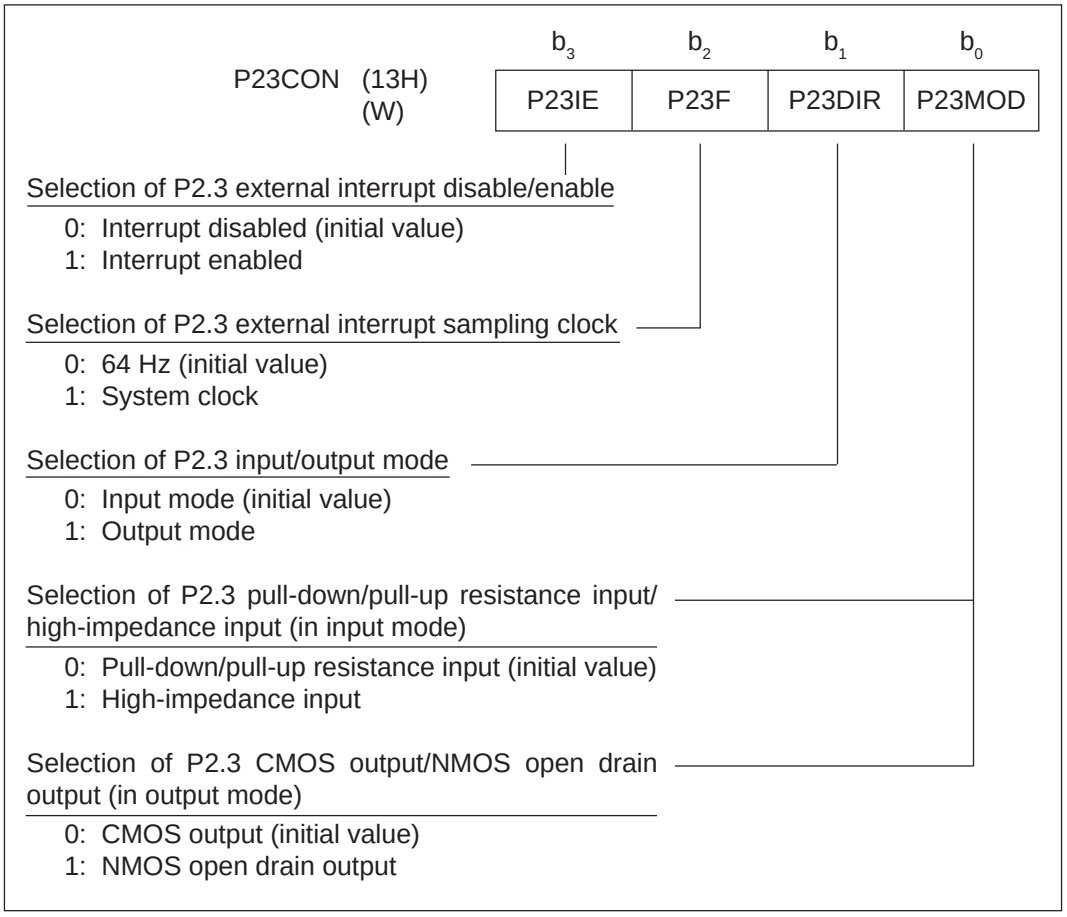
0: Pull-down/pull-up resistance input (initial value)
1: High-impedance input

Selection of P2.0 CMOS output/NMOS open drain output (in output mode)

0: CMOS output (initial value)
1: NMOS open drain output


P21CON (11H)
(W)
b3
b2
b1
b0
P21IE
P21F
P21DIR
P21MOD
Selection of P2.1 external interrupt disable/enable
0: Interrupt disabled (initial value)
1: Interrupt enabled
Selection of P2.1 external interrupt sampling clock
0: 64 Hz (initial value)
1: System clock
Selection of P2.1 input/output mode
0: Input mode (initial value)
1: Output mode
Selection of P2.1 pull-down/pull-up resistance input/ high-impedance input (in input mode)
0: Pull-down/pull-up resistance input (initial value)
1: High-impedance input
Selection of P2.1 CMOS output/NMOS open drain output (in output mode)
0: CMOS output (initial value)
1: NMOS open drain output


P22CON (12H)
(W)
b3
b2
b1
b0
P22IE
P22F
P22DIR
P22MOD
Selection of P2.2 external interrupt disable/enable
0: Interrupt disabled (initial value)
1: Interrupt enabled
Selection of P2.2 external interrupt sampling clock
0: 64 Hz (initial value)
1: System clock
Selection of P2.2 input/output mode
0: Input mode (initial value)
1: Output mode
Selection of P2.2 pull-down/pull-up resistance input/ high-impedance input (in input mode)
0: Pull-down/pull-up resistance input (initial value)
1: High-impedance input
Selection of P2.2 CMOS output/NMOS open drain output (in output mode)
0: CMOS output (initial value)
1: NMOS open drain output


P23CON (13H)
(W)
b3
b2
b1
b0
P23IE
P23F
P23DIR
P23MOD
Selection of P2.3 external interrupt disable/enable
0: Interrupt disabled (initial value)
1: Interrupt enabled
Selection of P2.3 external interrupt sampling clock
0: 64 Hz (initial value)
1: System clock
Selection of P2.3 input/output mode
0: Input mode (initial value)
1: Output mode
Selection of P2.3 pull-down/pull-up resistance input/ high-impedance input (in input mode)
0: Pull-down/pull-up resistance input (initial value)
1: High-impedance input
Selection of P2.3 CMOS output/NMOS open drain output (in output mode)
0: CMOS output (initial value)
1: NMOS open drain output

(5) Port 3 control registers (P30CON to P33CON)

The Port 3 control registers (P30CON to P33CON) are 4-bit special function registers (SFRs) to perform selection of input/output mode, selection of pull-down/pull-up resistance input or high impedance input in input mode, selection of CMOS output or NMOS open drain output in output mode, selection of external interrupt disable or enable and selection of sampling clocks of external interrupts. There is no selection bit of sampling clock of an external interrupt for Port 3.3 and selection of the SIN function is assigned which is a secondary function of the serial port. Since P30CON to P33CON are write-only registers, it is not possible to use bit manipulation instructions and increment/decrement instructions.

P30CON (14H) (W)

b_3	b_2	b_1	b_0
P30IE	P30F	P30DIR	P30MOD

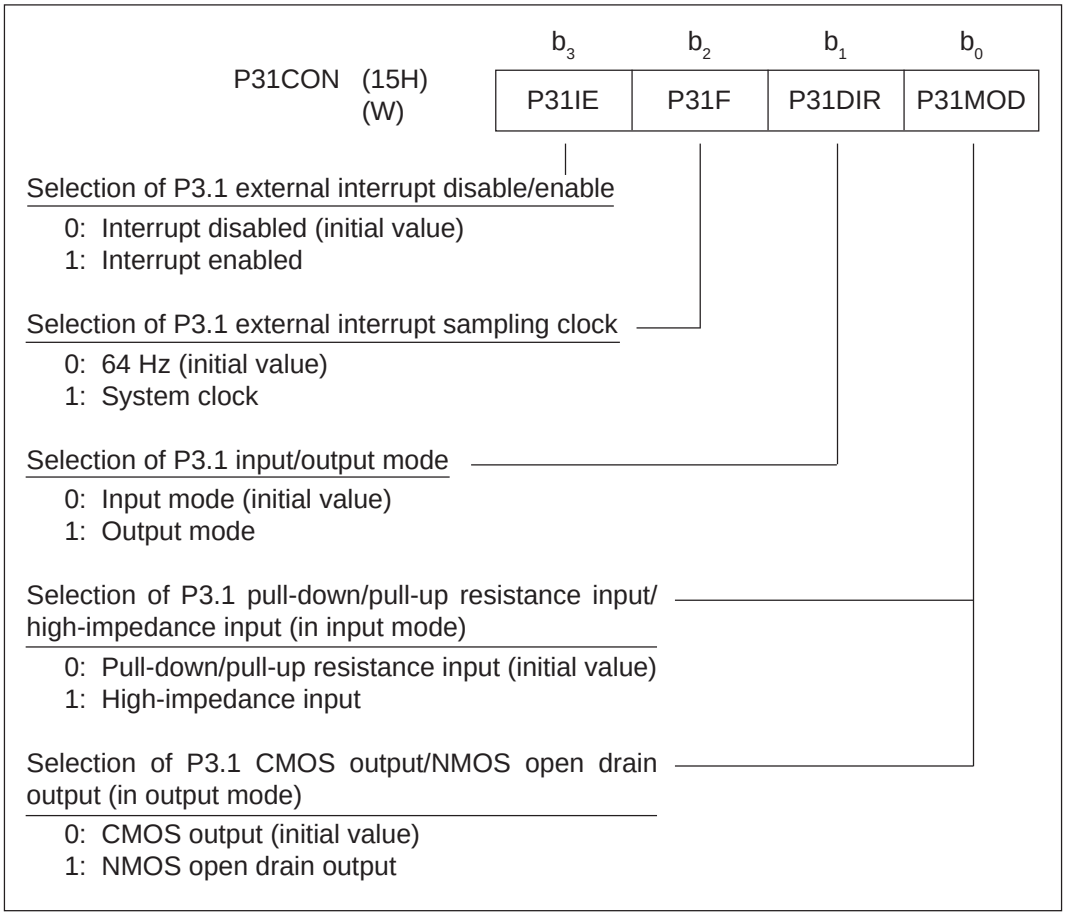
Selection of P3.0 external interrupt disable/enable
- 0: Interrupt disabled (initial value)
- 1: Interrupt enabled

Selection of P3.0 external interrupt sampling clock
- 0: 64 Hz (initial value)
- 1: System clock

Selection of P3.0 input/output mode
- 0: Input mode (initial value)
- 1: Output mode

Selection of P3.0 pull-down/pull-up resistance input/ high-impedance input (in input mode)
- 0: Pull-down/pull-up resistance input (initial value)
- 1: High-impedance input

Selection of P3.0 CMOS output/NMOS open drain output (in output mode)
- 0: CMOS output (initial value)
- 1: NMOS open drain output


P31CON (15H)
(W)
b3
b2
b1
b0
P31IE
P31F
P31DIR
P31MOD
Selection of P3.1 external interrupt disable/enable
0: Interrupt disabled (initial value)
1: Interrupt enabled
Selection of P3.1 external interrupt sampling clock
0: 64 Hz (initial value)
1: System clock
Selection of P3.1 input/output mode
0: Input mode (initial value)
1: Output mode
Selection of P3.1 pull-down/pull-up resistance input/ high-impedance input (in input mode)
0: Pull-down/pull-up resistance input (initial value)
1: High-impedance input
Selection of P3.1 CMOS output/NMOS open drain output (in output mode)
0: CMOS output (initial value)
1: NMOS open drain output

P32CON (16H) (W)

b_3	b_2	b_1	b_0
P32IE	P32F	P32DIR	P32MOD

Selection of P3.2 external interrupt disable/enable

0: Interrupt disabled (initial value)
1: Interrupt enabled

Selection of P3.2 external interrupt sampling clock

0: 64 Hz (initial value)
1: System clock

Selection of P3.2 input/output mode

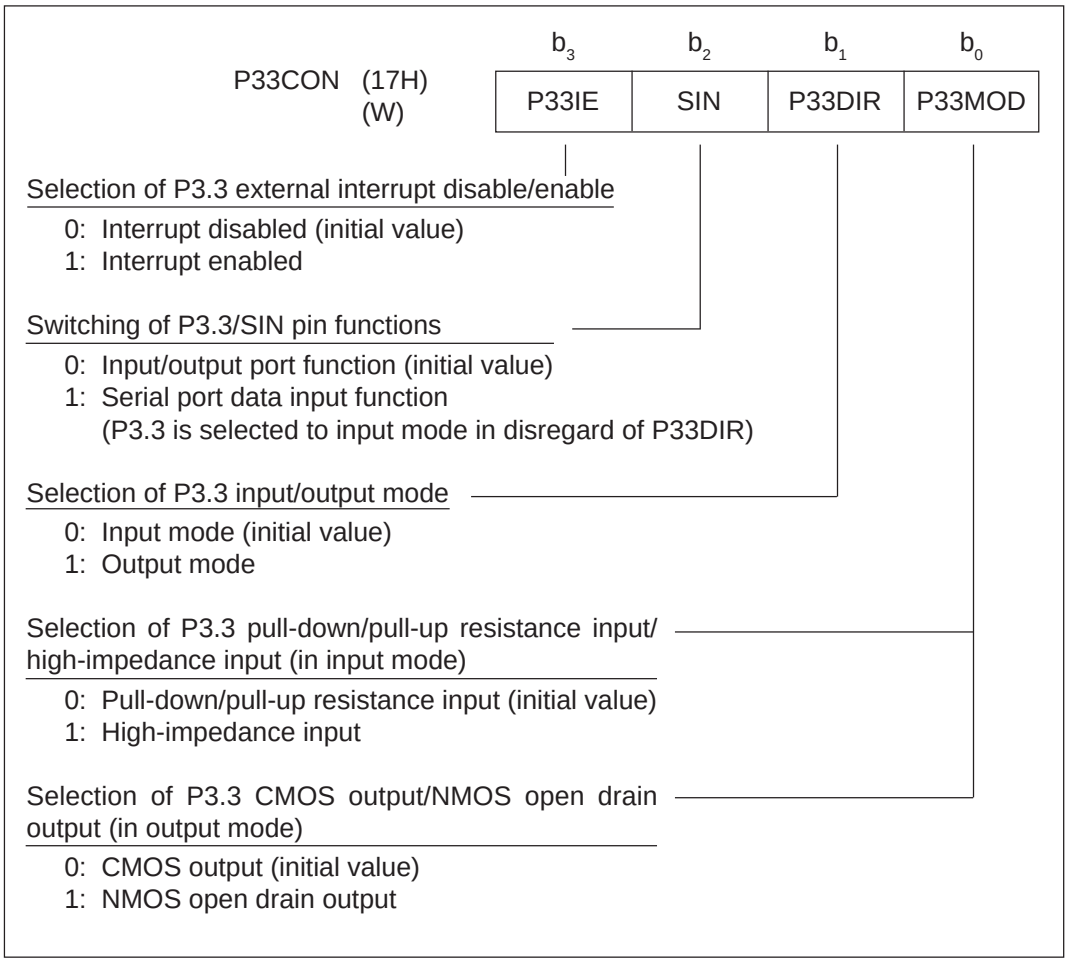
0: Input mode (initial value)
1: Output mode

Selection of P3.2 pull-down/pull-up resistance input/ high-impedance input (in input mode)

0: Pull-down/pull-up resistance input (initial value)
1: High-impedance input

Selection of P3.2 CMOS output/NMOS open drain output (in output mode)

0: CMOS output (initial value)
1: NMOS open drain output


P33CON (17H)
(W)
b3
b2
b1
b0
P33IE
SIN
P33DIR
P33MOD
Selection of P3.3 external interrupt disable/enable
0: Interrupt disabled (initial value)
1: Interrupt enabled
Switching of P3.3/SIN pin functions
0: Input/output port function (initial value)
1: Serial port data input function
(P3.3 is selected to input mode in disregard of P33DIR)
Selection of P3.3 input/output mode
0: Input mode (initial value)
1: Output mode
Selection of P3.3 pull-down/pull-up resistance input/ high-impedance input (in input mode)
0: Pull-down/pull-up resistance input (initial value)
1: High-impedance input
Selection of P3.3 CMOS output/NMOS open drain output (in output mode)
0: CMOS output (initial value)
1: NMOS open drain output

(6) Port 4 control registers (P40CON to P43CON)

The port 4 control registers (P40CON to P43CON) are 4-bit special function registers (SFRs) to perform selection of input/output mode, selection of pull-down/pull-up resistance input or high impedance input in input mode, selection of CMOS output or NMOS open drain output in output mode, selection of external interrupt disable or enable and selection of SOUT, SPR, SCLK functions of the serial port or RC oscillation monitor functions which are a secondary function. Since P40CON to P43CON are write-only registers, it is not possible to use bit manipulation instructions and increment/decrement instructions.

P40CON (18H) (W)

b_3	b_2	b_1	b_0
P40IE	SOUT	P40DIR	P40MOD

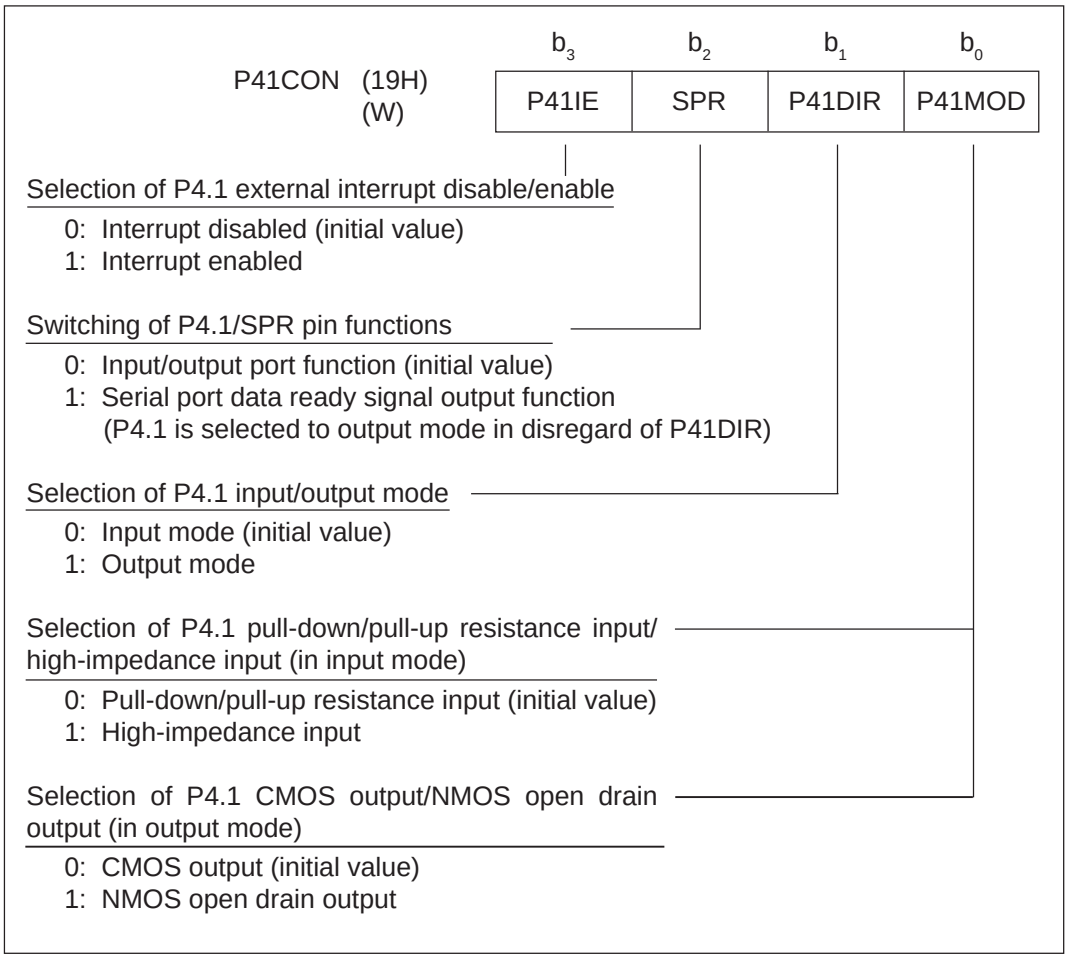
Selection of P4.0 external interrupt disable/enable
- 0: Interrupt disabled (initial value)
- 1: Interrupt enabled

Switching of P4.0/SOUT pin functions
- 0: Input/output port function (initial value)
- 1: Serial port data output function
  (P4.0 is selected to output mode in disregard of P40DIR)

Selection of P4.0 input/output mode
- 0: Input mode (initial value)
- 1: Output mode

Selection of P4.0 pull-down/pull-up resistance input/ high-impedance input (in input mode)
- 0: Pull-down/pull-up resistance input (initial value)
- 1: High-impedance input

Selection of P4.0 CMOS output/NMOS open drain output (in output mode)
- 0: CMOS output (initial value)
- 1: NMOS open drain output


P41CON (19H)
(W)
b3
b2
b1
b0
P41IE
SPR
P41DIR
P41MOD
Selection of P4.1 external interrupt disable/enable
0: Interrupt disabled (initial value)
1: Interrupt enabled
Switching of P4.1/SPR pin functions
0: Input/output port function (initial value)
1: Serial port data ready signal output function
(P4.1 is selected to output mode in disregard of P41DIR)
Selection of P4.1 input/output mode
0: Input mode (initial value)
1: Output mode
Selection of P4.1 pull-down/pull-up resistance input/ high-impedance input (in input mode)
0: Pull-down/pull-up resistance input (initial value)
1: High-impedance input
Selection of P4.1 CMOS output/NMOS open drain output (in output mode)
0: CMOS output (initial value)
1: NMOS open drain output

P42CON (1AH) (W)

b_3	b_2	b_1	b_0
P42IE	SCLK	P42DIR	P42MOD

Selection of P4.2 external interrupt disable/enable

0: Interrupt disabled (initial value)
1: Interrupt enabled

Switching of P4.2/SCLK pin functions

0: Input/output port function (initial value)
1: Serial port clock input/output function
(P4.2 input/output mode is selected by EXSC of Serial port control register (SCON))

Selection of P4.2 input/output mode

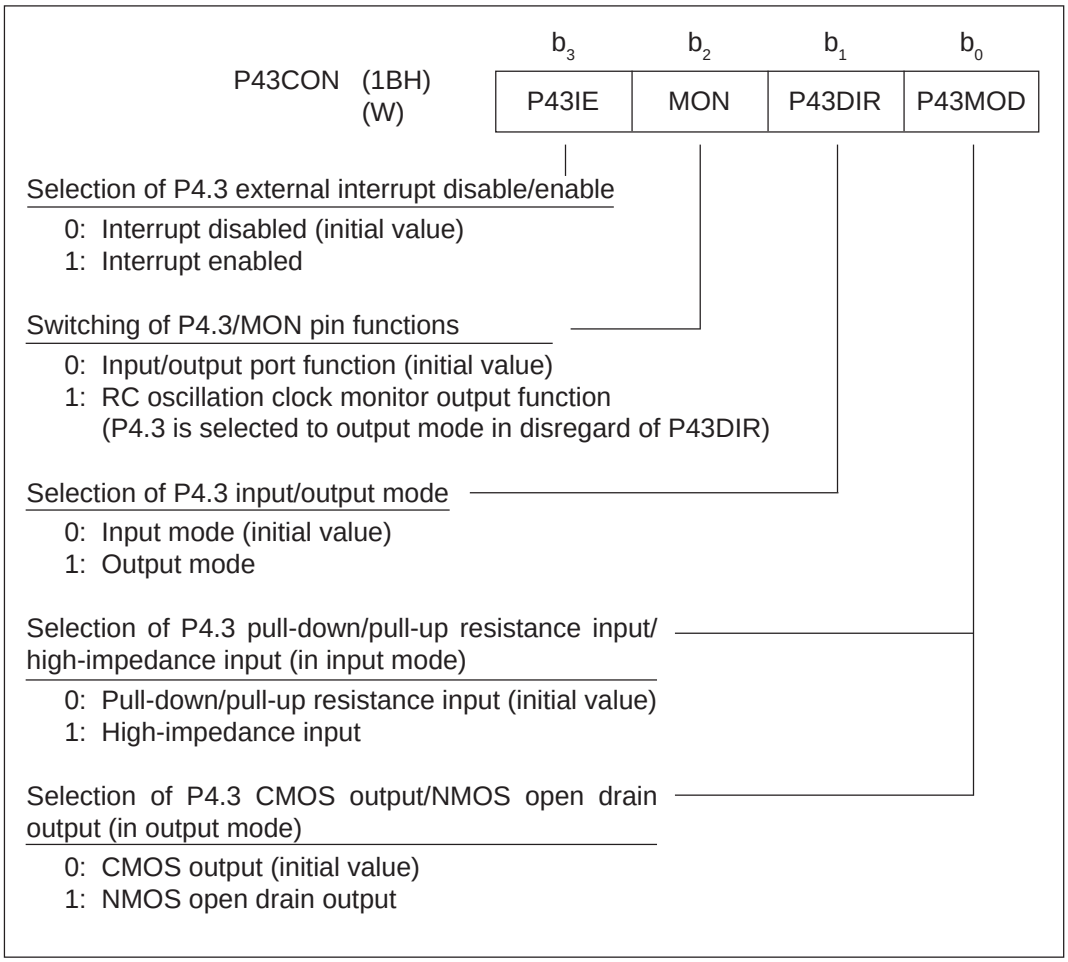
0: Input mode (initial value)
1: Output mode

Selection of P4.2 pull-down/pull-up resistance input/ high-impedance input (in input mode)

0: Pull-down/pull-up resistance input (initial value)
1: High-impedance input

Selection of P4.2 CMOS output/NMOS open drain output (in output mode)

0: CMOS output (initial value)
1: NMOS open drain output



Bit 3: P20IE to P23IE, P30IE to P33IE and P40IE to P43IE
This bit is to select disabling/enabling external interrupts. When each IE bit is reset to "0", external interrupts are disabled and when each IE bit is set to "1", the external 0 interrupt request is generated by detecting the change of input level of the pin if the corresponding port is in input mode. At system reset, each IE bit is reset to "0".

Bit 2: P20F to P23F and P30F to P32F
This bit is to select a sampling clock of an external interrupt. When each F bit is reset to "0", the 64 Hz output of the time base counter is selected as the sampling clock and when each F bit is set to "1", the system clock (32.768 kHz or 700 kHz) is chosen as the sampling clock. At system reset, each F bit is reset to "0". There is no selection function of the sampling clock of external interrupts for P3.3 and P4.0 to P4.3 and it is fixed at 64 Hz.

Bit 2: SIN (P33CON)
This bit selects data input (SIN) of the serial port which is a secondary function of Port 3.3. When SIN is reset to "0", P3.3 becomes a normal port function and when SIN is set to "1", the data input function of the serial port is assigned. When SIN is set to "1", P3.3 is automatically set to input mode. At system reset, SIN is reset to "0".

Bit 2: SOUT (P40CON)
This bit sets data output (SOUT) of the serial port which is a secondary function of Port 4.0. When SOUT is reset to "0", P4.0 becomes a normal port function and when it is set to "1", the data output function of the serial port is assigned. When SOUT is set to "1", P4.0 is set to output mode automatically. At system reset, SOUT is reset to "0".

Bit 2: SPR (P41CON)
This bit sets data ready signal (SPR) of the serial port which is a secondary function of Port 4.1. When SPR is reset to "0", P4.1 becomes a normal port function and when it is set to "1", the data ready signal output function of the serial port is assigned. When SPR is set to "1", P4.1 is set to output mode automatically. At system reset, SPR is reset to "0".

Bit 2: SCLK (P42CON)
This bit sets transfer clock input/output (SCLK) of the serial port which is a secondary function of Port 4.2. When SCLK is reset to "0", P4.2 becomes a normal port function and when it is set to "1", the transfer clock input/output function of the serial port is assigned. When SCLK is set to "1", P4.2 is set to output mode automatically in the mode where the system clock is set as the transfer clock after resetting the EXSC bit of the serial port control register (SCON) to "0". P4.2 is set to input mode in the mode where the EXSC bit is set to "1". At system reset, SCLK is reset to "0".

Bit 2: MON (P43CON)
This bit sets output of the RC oscillation clock (MON) which is a secondary function of Port 4.3. When MON is reset to "0", P4.3 becomes a normal port function and when it is set to "1", the output function of the A/D converter RC oscillation clock is assigned. When MON is set to "1", P4.3 is set to output mode automatically. At system reset, MON is reset to "0".

Bit 1: P20DIR to P23DIR, P30DIR to P33DIR and P40DIR to P43DIR
This bit selects input/output of each port. When each DIR bit is reset to "0", each port becomes input mode and when each DIR bit is set to "1", each port becomes output mode. At system reset, each DIR bit is reset to "0".

Bit 0: P20MOD to P23MOD, P30MOD to P33MOD and P40MOD to P43MOD
When each DIR bit is reset to "0" to select input mode, pull-down/pull-up resistance input or high-impedance input is selected.

When each DIR bit is set to "1" to select output mode, CMOS output or NMOS open drain output is selected.

When each MOD bit is reset to "0", pull-down/pull-up resistance input is selected in input mode and CMOS output mode is selected in output mode. When each MOD bit is set to "1", high-impedance input is selected in input mode and NMOS open drain output mode is selected in output mode. Selection of pull-down/pull-up input is done by bit 2 (PUD) of the Port 01 control register (P01CON). When PUD is reset to "0", it becomes pull-up resistance input and when PUD is set to "1", it becomes pull-down resistance input.

At system reset, each MOD bit is reset to "0".

Table 7-2 shows the relationship among each DIR bit, each MOD bit and each PUD bit.

Table 7-2 Relation among Each DIR Bit, Each MOD Bit and Each PUD Bit

Each DIR	Each MOD	PUD	State of input/output
0	0	0	Pull-up resistance input selected
0	0	1	Pull-down resistance input selected
0	1	—	High-impedance input selected
1	0	—	CMOS output selected
1	1	—	NMOS open drain output selected

7.3.3 External Interrupt Generation Timing of Port 2, Port 3 and Port 4

External interrupt of Ports 2 to 4 is generated when each IE bit (P20IE to P23IE, P30IE to P33IE and P40IE to P43IE) of P2.0 to P2.3, P3.0 to P3.3 and P4.0 to P4.3 are set to "1" and by the change of an input level of those ports for which each DIR bit (P20DIR to P23DIR, P30DIR to P33DIR and P40DIR to P43DIR) is set to "0" (set for interrupt enable and input mode). The External 0 interrupt (XI0INT) is generated by OR signal of each level change detection signal.

Change of input level can be sampled by 64 Hz output of the time base counter which is the sampling clock or by falling of the system clock (32.768 kHz or 700 kHz). Selection of the sampling clock is performed by Bit 2 (P20F to P23F, P30F to P32F) of each port control register and when the F bit is reset to "0", the sampling clock becomes 64 Hz and when the F bit is set to "1", the sampling clock changes to the system clock. There is no function to select the sampling clock for P3.3 and P4.0 to P4.3 and they are fixed at 64 Hz output of the time base counter.

Delay time until the External 0 interrupt request flag (QXI0) is set after the level of Port 2 to Port 4 is changed to output XI0INT signal is one period of the sampling clock or less. Since the External 0 interrupt request flag (QXI0) is set by input level change of one of Port 2 to Port 4, which port the interrupt request comes from should be judged by checking the signal level after reading out each port.

The interrupt vector address of External interrupt XI0INT is address 038H.

Figures 7-12 and 7-13 show the External 0 interrupt generation circuit and timing.

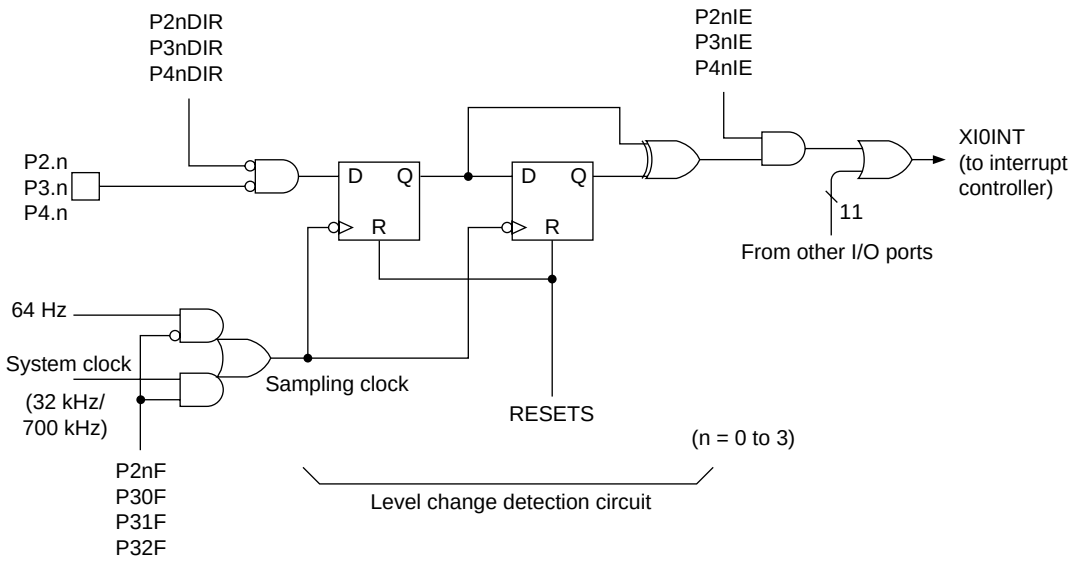


Figure 7-12 External 0 Interrupt Generation Circuit (one bit)

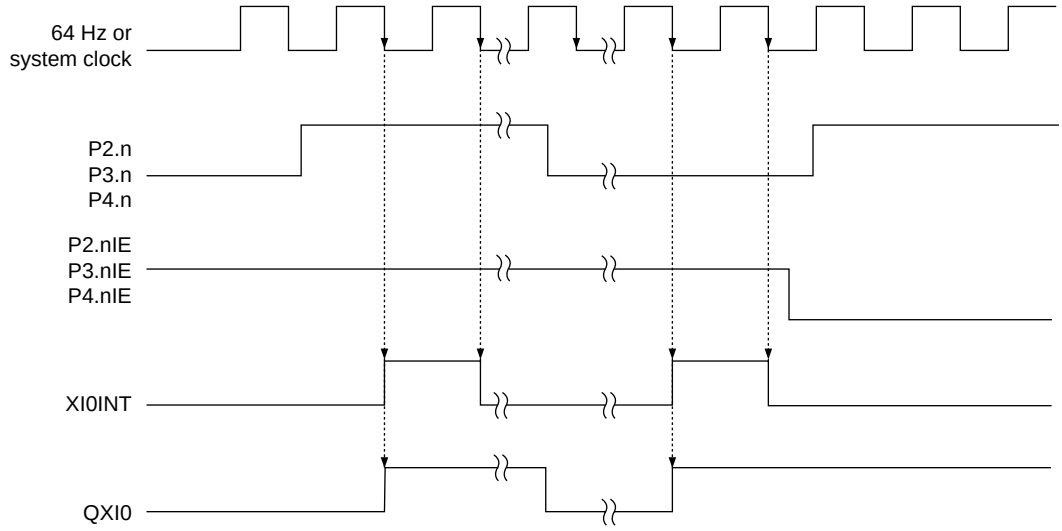


Figure 7-13 External 0 Interrupt Generation Timing

Table 7-3 shows the list of port-related registers.

Table 7-3 List of Port-Related Registers

Register name	Symbol	Address	Read/Write	Byte access	Value at system reset
Port 2 register	P2	00H	R/W	Yes	0H
Port 3 register	P3	01H	R/W		0H
Port 4 register	P4	02H	R/W	Yes	0H
Port 0 register	P0	03H	R		Depends on input value
Port 1 register	P1	04H	R/W	No	0H
Port 20 control register	P20CON	10H	W	Yes	0H
Port 21 control register	P21CON	11H	W		0H
Port 22 control register	P22CON	12H	W	Yes	0H
Port 23 control register	P23CON	13H	W		0H
Port 30 control register	P30CON	14H	W	Yes	0H
Port 31 control register	P31CON	15H	W		0H
Port 32 control register	P32CON	16H	W	Yes	0H
Port 33 control register	P33CON	17H	W		0H
Port 40 control register	P40CON	18H	W	Yes	0H
Port 41 control register	P41CON	19H	W		0H
Port 42 control register	P42CON	1AH	W	Yes	0H
Port 43 control register	P43CON	1BH	W		0H
Port 01 control register	P01CON	1CH	W	No	8H
Interrupt enable register 0	IE0	30H	R/W	Yes	0H
Interrupt request register 0	IRQ0	34H	R/W	Yes	0H

Chapter 8

Serial Port (SIOP)

Chapter 8 Serial Port (SIOP)

8.1 Overview

The ML64168 has an 8-bit synchronous serial port.

Receive/transmit operation of the serial port is performed simultaneously and the serial transfer clock can select either internal or external mode. Direction of transfer data can be either MSB as a head or LSB as a head.

Each pin of the serial port is assigned as secondary functions of P3.3 and P4.0 to P4.2. Setting each bit of SIN, SOUT, SPR and SCLK of P33CON and P40CON to P42CON to "1" makes each pin valid.

8.2 Layout of Serial Port

Figure 8-1 shows the layout of the serial port.

In Figure 8-1, P3.3 is the data receive pin, P4.0 is the data transmit pin, P4.1 is the serial port ready pin and P4.2 is the transfer clock pin.

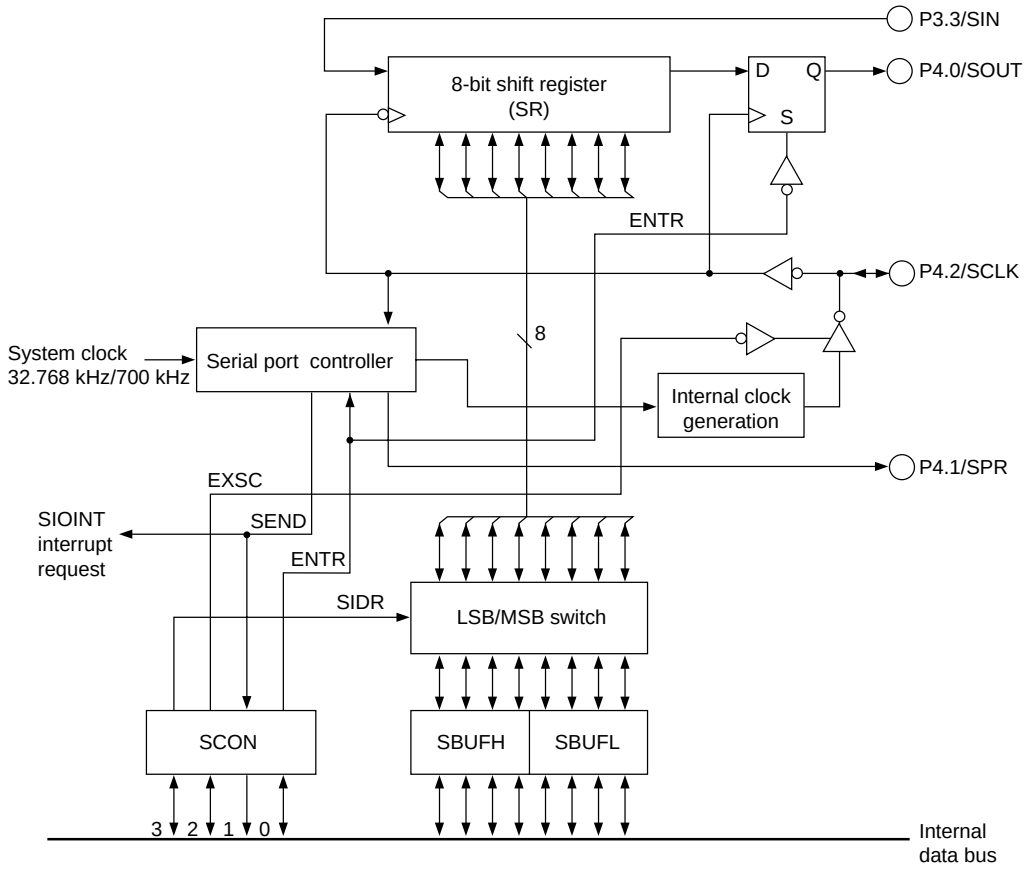


Figure 8-1 Layout of Serial Port

8.3 Operation of Serial Port

By setting the ENTR bit of the Serial port control register (SCON) to "1" after writing send data to the Serial port buffers (SBUFH and SBUFL), serial transfer begins. When serial transfer is finished, the SEND bit of SCON is set to "1" and the Serial port interrupt request SIOINT is generated. The vector address of the Serial port interrupt request is at address 035H.

When serial transfer is finished, receive data is written to SBUFH and SBUFL. It is not necessary to write send data if only the receive operation is performed.

The SDIR bit of SCON is used to select the direction of transfer data and if SDIR is reset to "0", MSB of SBUFH and SBUFL becomes head data and if SDIR is set to "1", LSB becomes head data.

The EXSC bit of SCON is used to select transfer clocks. When EXSC is reset to "0", the system clock is selected as the transfer clock and the system clock is output to the P4.2/SCLK pin. By setting EXSC to "1", the external clock can be selected as the transfer clock and those clocks input from the P4.2/SCLK pin become the transfer clocks.

Figure 8-2 shows the operation time chart of the serial port.

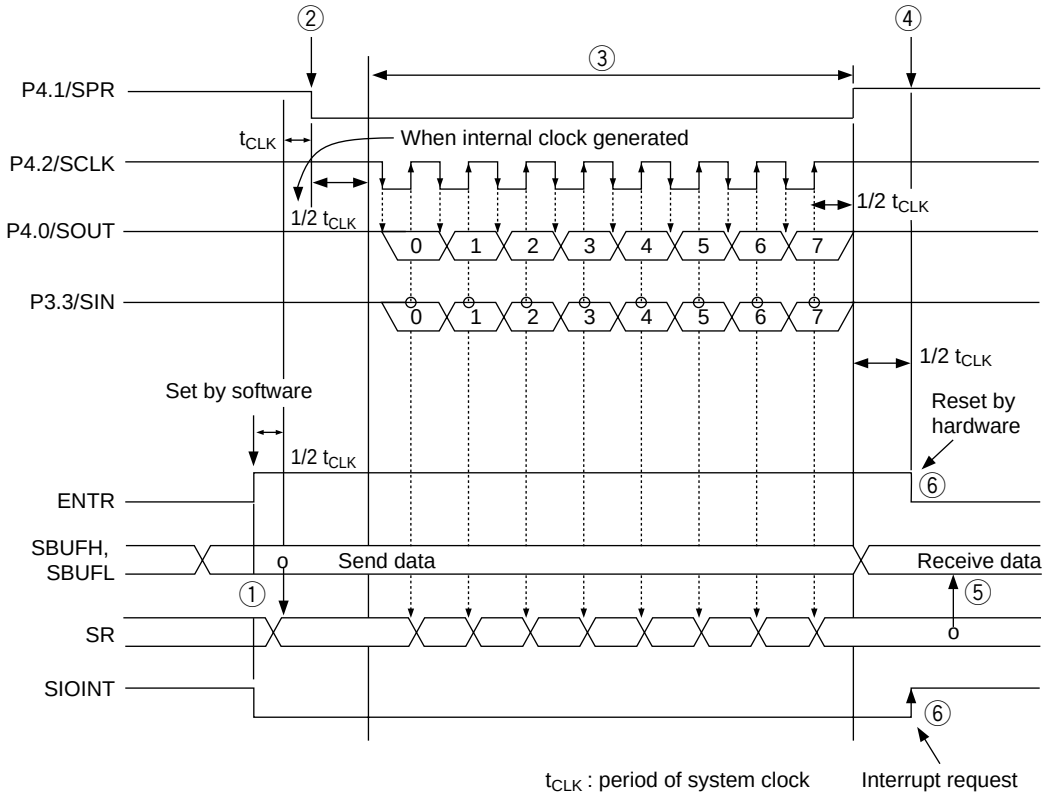


Figure 8-2 Serial Port Operation Time Chart

As shown in Figure 8-2, when serial transfer is started by setting the ENTR bit to "1", the P4.1/SPR pin of the transfer ready pin becomes "L" level. After the other side of the communication detects "L" level of the P4.1/SPR pin, sending data is triggered at the falling of the transfer clock of P4.2/SCLK and receiving data is gotten at the rising. When the external clock is selected, it is necessary to input transfer clocks after detecting "L" level of P4.1/SPR.

Internal operation when the transfer is started by setting the ENTR bit to "1" is shown below:

① The contents of SBUFH and SBUFL are written to the 8-bit shift register (SR).

② "L" level is output to the P4.1/SPR pin.

③ With the falling of the transfer clock of the P4.2/SCLK pin, data in SR is output to the P4.0/SOUT pin and with the rising of the transfer clock, input data of the P3.3/SIN pin are received by SR.

④ When the 8-bit transfer is finished, "H" level is output to the P4.1/SPR pin.

⑤ The contents of SR are written to SBUFH and SBUFL.

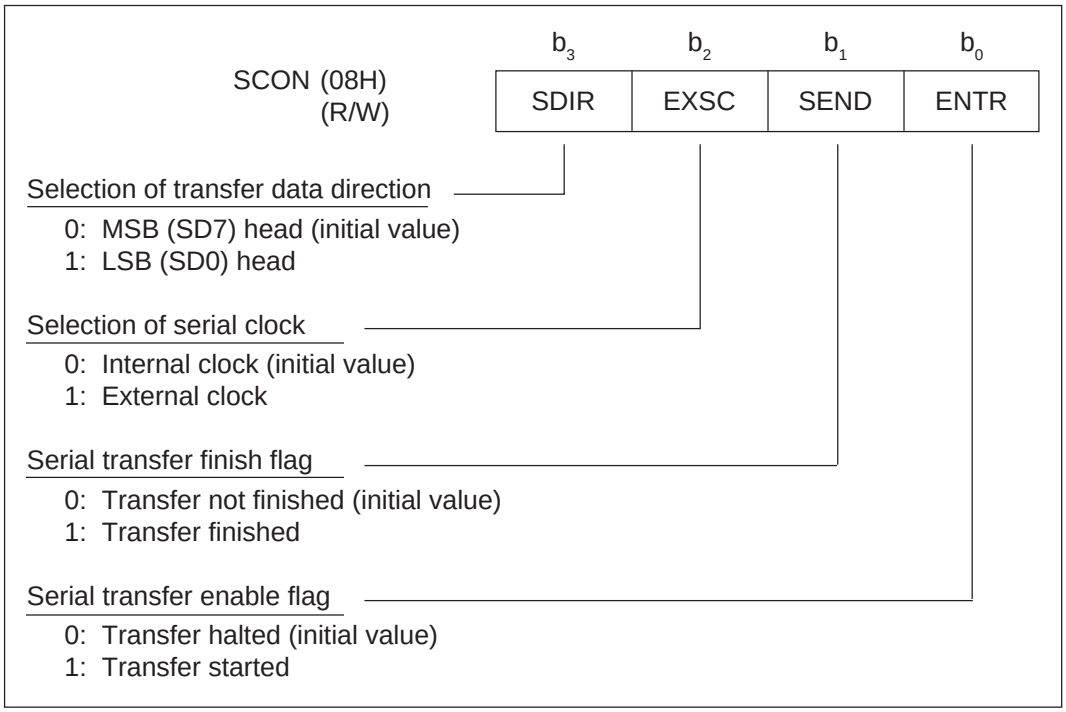
⑥ The ENTR bit is reset to "0", the SEND bit is set to "1" and a Serial port interrupt request (SIOINT) is generated.

When transmission and reception are not made simultaneously, it is possible to do the data signal lines to a single line by connecting SIN and SOUT terminals at external. In this case, we recommend you respectively to set the SOUT terminal to a NMOS open drain mode (P40MOD bit of P40CON is made to "1") and to set the SIN terminal to a pull-up resistance mode. (PUD bit of P01CON is made to "0".) If the PUD bit of P01CON can not be set to "0" for using a pull-down mode in other, do the SIN terminal to a high impedance mode (P33MOD bit of P33CON is made to "1") and pull-up to V_{DDI} at external.

8.4 Registers Related to Serial Port

(1) Serial Port Control Register (SCON)

The Serial port control register (SCON) is a 4-bit special function register (SFR) to control the Serial port.



Bit 3: SDIR
This bit is used to select the direction of serial transfer data. When reset to "0", MSB becomes the head transfer data and when set to "1", LSB becomes the head transfer data. At system reset, it is reset to "0" and is in MSB head mode.

Bit 2: EXSC
This bit is used to select the transfer clock of serial transfer. When reset to "0", the system clock is selected as the transfer clock and when set to "1", the external clock that is input from P4.2/SCLK is selected. At system reset, it is reset to "0" and the system clock is selected as the transfer clock.

Bit 1: SEND
This bit is used to indicate the completion of serial transfer. When serial transfer is completed, the SEND bit is set to "1" and the Serial port interrupt request (SIOINT) is generated.

When reading or writing from/to the serial port control register (SCON), the SEND bit is reset to "0". The SEND bit is a read-only bit and is reset to "0" at system reset.

Bit 0: ENTR
This bit specifies whether serial transfer is enabled or not. When reset to "0", serial transfer is halted and is started when this bit is set to "1". At system reset, it is reset to "0" and serial transfer is halted. When ENTR is set to "1", this bit is automatically reset after serial transfer is completed.

Writing "0" to ENTR during serial transfer (when ENTR = 1) interrupts serial transfer. At that time, the serial port interrupt request (SIOINT) is not generated.

(2) Serial Port Buffer Registers (SBUFH, SBUFL)

The Serial port buffer registers are 4-bit special function registers (SFRs) to write send data or to read receive data.

SBUFL (06H) (R/W)

b_3	b_2	b_1	b_0
SD3	SD2	SD1	SD0
			(LSB)

Value of lower bits of the serial port buffer

SBUFH (07H) (R/W)

b_3	b_2	b_1	b_0
SD7	SD6	SD5	SD4
(MSB)			

Value of upper bits of the serial port buffer

Bit 0 of SBUFL(SD0) is LSB and Bit 3 of SBUFH(SD7) is MSB.

Byte processing is possible for these two registers.
When SBUFL and SBUFH are read after the completion of serial transfer, the contents become receive data.

Figure 8-3 shows the bit composition of serial data output from the SOUT pin as well as input to the SIN pin and the contents of SBUFL and SBUFH.

a) When SIR = "0" (MSB as head)

SD0	SD1	SD2	SD3	SD4	SD5	SD6	SD7	Transfer direction →
							(Head)	

b) When SDIR = "1" (LSB as head)

SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0	Transfer direction →
							(Head)	

Figure 8-3 Bit Composition of Transfer Data

Tables 8-1 and 8-2 show the list of serial port-related registers and pins.

Table 8-1 List of Serial Port-Related Registers

Register name	Symbol	Address	Read/Write	Byte access	Value at system reset
Serial port buffer lower register	SBUFL	06H	R/W	Yes	0H
Serial port buffer upper register	SBUFH	07H	R/W		0H
Serial port control register	SCON	08H	R/W	No	0H
Interrupt enable register 0	IE0	30H	R/W	Yes	0H
Interrupt request register 0	IRQ0	34H	R/W	Yes	0H

Table 8-2 List of Serial Port-Related Pins

Pin name	Pin No.		Pad No.	Input/ Output	Note
	GP	GA, TB			
P3.3	25	23	23	Input	Serial port data input (SIN)
P4.0	26	24	24	Output	Serial port data output (SOUT)
P4.1	27	25	25	Output	Serial port ready output (SPR)
P4.2	28	26	26	Input/Output	Serial port transfer clock input/output (SCLK)

Chapter 9

Buzzer Driver (BD)

Chapter 9 Buzzer Driver (BD)

9.1 Overview

The ML64168 has a built-in buzzer driver with 15 buzzer output frequencies and 4 buzzer output modes. Each buzzer output is selected by the Buzzer control register (BDCON) and the Buzzer frequency control register (BFCON).

9.2 Layout of Buzzer Driver

Figure 9-1 shows the layout of the buzzer driver.

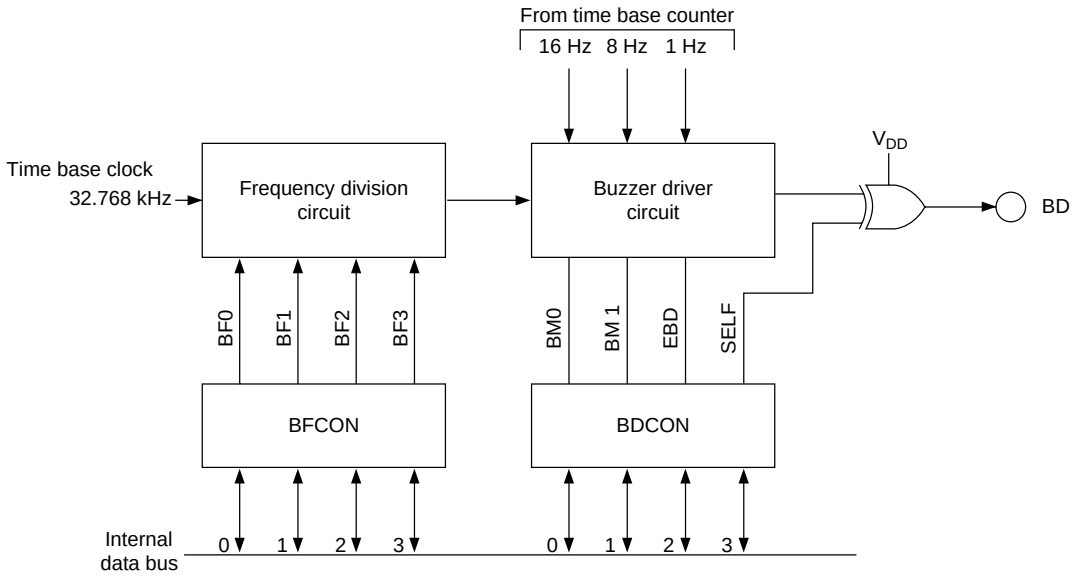


Figure 9-1 Layout of Buzzer Driver

9.3 Operation of Buzzer Driver

When Bit 2 (EBD) of the Buzzer control register (BDCON) is set to "1", buzzer drive signals are output at the buzzer driver pin (BD). The Buzzer frequency control register (BFCON) can select 15 buzzer output frequencies. In buzzer output mode, two kinds of discontinuous sounds, a single sound and a continuous sound can be selected by Bit 1/0 (BM1/BM0) of BDCON. Bit 3 (SELF) of BDCON can select output logic of the BD pin. When the SELF bit is reset to "0", positive logic output ("L" level output at halt) is selected and negative logic output ("H" level output at halt) is selected when it is set to "1". The duty of buzzer output frequencies is 50%.

In (a) discontinuous sound 1 mode, waveforms which are synchronized with 8 Hz output of the time base counter are output. In (b) discontinuous 2 mode, waveforms that are synchronized to the logical AND of 8 Hz signal output and a "L" level of 1 Hz signal are output. In (c) single sound mode, output begins synchronizing with the rising of EBD and stops at the falling of 16 Hz output of the time base counter. In (d) continuous sound mode, output is continued while EBD is "1".

Figure 9-2 shows output waveforms in each output mode. Shaded area in the figure indicates the buzzer output frequency signal.

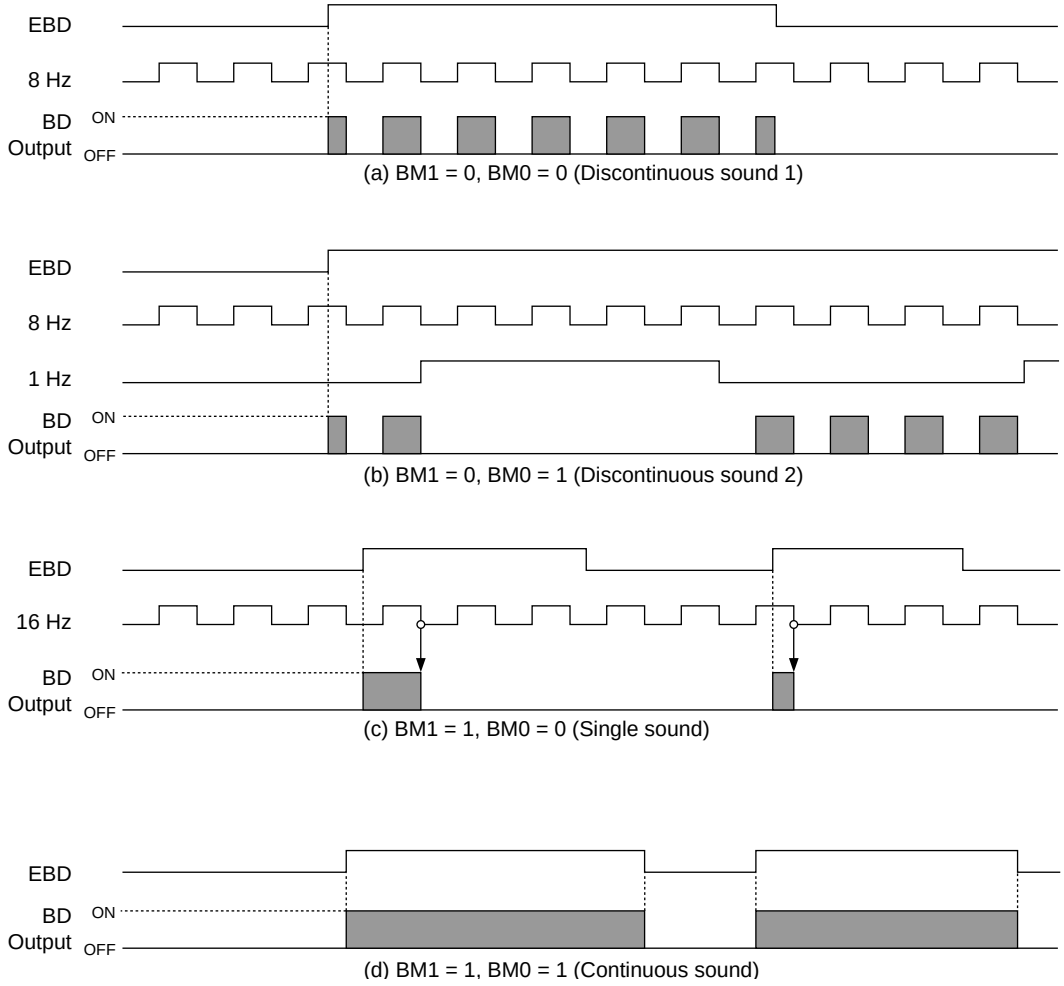
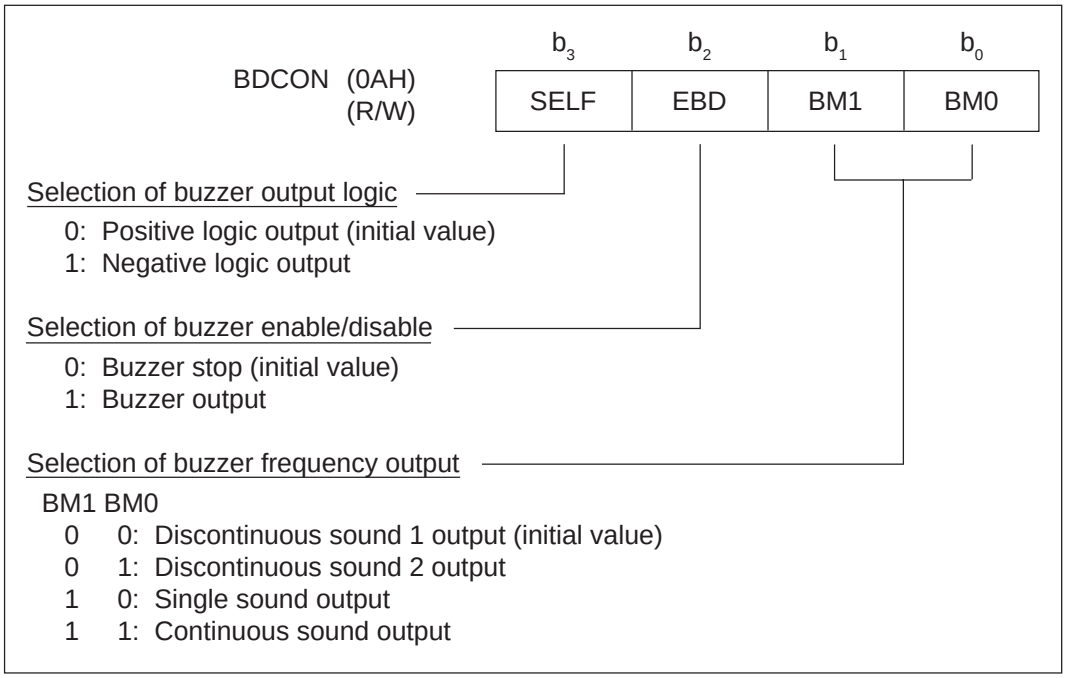


Figure 9-2 Buzzer Driver Output Waveforms in Each Output Mode

9.4 Registers Related to Buzzer Driver

(1) Buzzer control register (BDCON)

The Buzzer control register (BDCON) is a 4-bit special function register (SFR) that controls output logic of the BD pin, 4 types of buzzer output modes and ON/OFF of buzzer output.



Bit 3: SELF
This bit selects output logic of the BD pin. When reset to "0", positive logic output is selected ("L" level output when output is halted) and negative logic output ("H" level output when output is halted) is selected when set to "1". At system reset, it is reset to "0" and positive logic output is selected.

Bit 2:EBD
This bit selects ON/OFF of the buzzer driver output. At system reset, it is reset to "0" so that no buzzer is output.

Bits 1 and 0: BM1 and BM0
This bit selects output mode of the buzzer driver. It can select two types of discontinuous sounds, a single sound and a continuous sound. At system reset, BM1 and BM0 are reset to "0" so that discontinuous sound 1 output is selected.

(2) Buzzer frequency control register (BFCON)

The buzzer frequency control register (BFCON) is a 4-bit special function register (SFR) to control output frequencies of the buzzer.

BFCON (0BH) (R/W)

b_3	b_2	b_1	b_0
BF3	BF2	BF1	BF0

Selection of buzzer output frequencies

BF3	BF2	BF1	BF0	
0	0	0		0: Output stop (initial value)
0	0	0		1: 5.461 kHz
0	0	1		0: 4.096 kHz
0	0	1		1: 3.277 kHz
0	1	0		0: 2.730 kHz
0	1	0		1: 2.341 kHz
0	1	1		0: 2.048 kHz
0	1	1		1: 1.820 kHz
1	0	0		0: 1.638 kHz
1	0	0		1: 1.489 kHz
1	0	1		0: 1.365 kHz
1	0	1		1: 1.260 kHz
1	1	0		0: 1.170 kHz
1	1	0		1: 1.092 kHz
1	1	1		0: 1.024 kHz
1	1	1		1: 0.964 kHz

Bits 3 to 0: BF3 to 0
These bits select buzzer output frequency. At system reset, all are reset to "0" so that output is halted.

Each output frequency is output with 50% duty.

Tables 9-1 and 9-2 show the lists of buzzer driver-related registers and related pins.

Table 9-1 Buzzer Driver-Related Registers

Register name	Symbol	Address	Read/Write	Byte access	Value at system reset
Buzzer driver control register	BDCON	0AH	R/W	Yes	0H
Buzzer frequency control register	BFCON	0BH	R/W		0H

Table 9-2 Buzzer Driver-Related Pins

Pin name	Pin No.		Pad No.	Input/ Output	Note
	GP	GA, TB			
BD	30	28	28	Output	Buzzer driver pin

9.5 BD Output Waveform and External Circuit

Figure 9-3 shows the output waveform of the output pin of the buzzer driver. Output level of V_{DD}–V_{SS} is output at the BD pin.

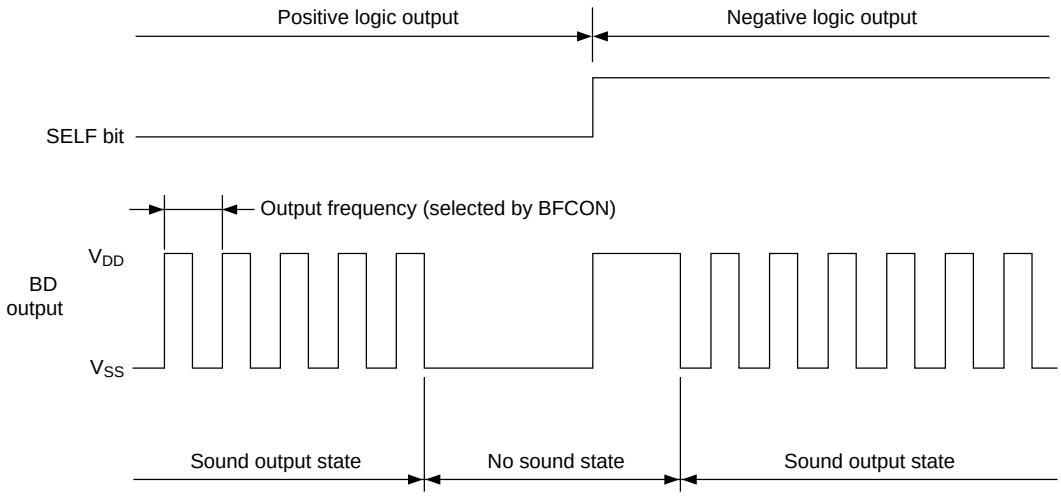
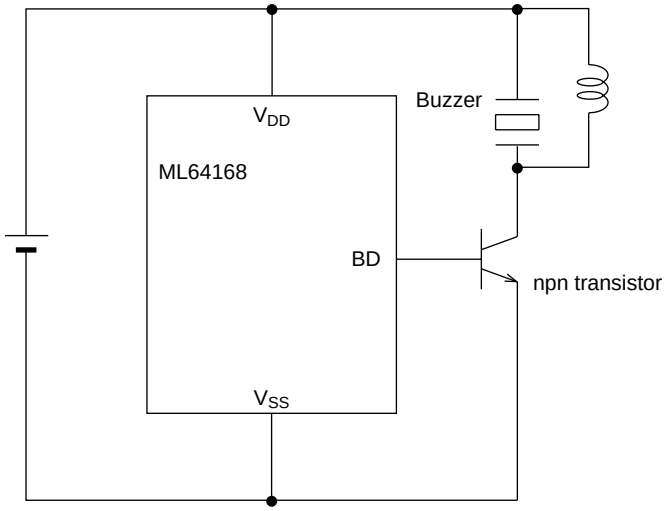
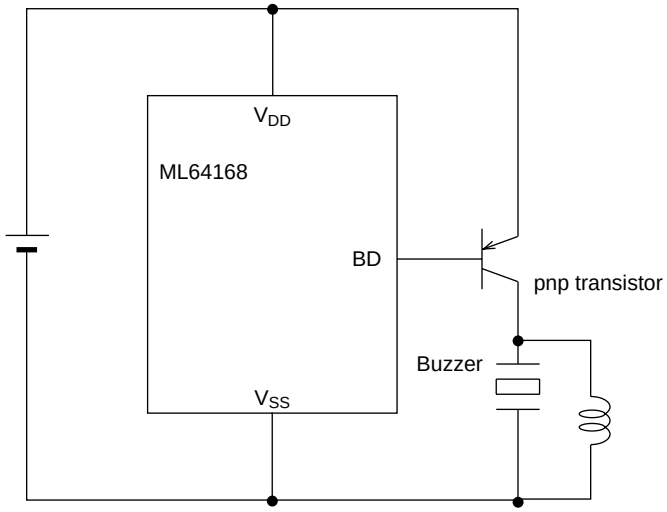


Figure 9-3 Waveform at BD Pin

Figure 9-4 shows a circuit example of a buzzer driver mounted outside. As illustrated blow, the buzzer must be driven through a transistor mounted outside and do not drive the buzzer directly at the BD terminal.



(a) In the case of SELF bit = "0"



(b) In the case of SELF bit = "1"

Figure 9-4 Circuit Example of a Buzzer Driver Mounted Outside

Chapter 10

Capture Circuit (CAPR)

Chapter 10 Capture Circuit (CAPR)

10.1 Overview

The ML64168 has a capture circuit that fetches 32 Hz to 256 Hz output of the time base counter at the falling of Port 0.0 or 0.1 (P0.0 or P0.1) to "L" level when the pull-up resistance input is chosen or at the rising to "H" level when the pull-down resistance input is chosen. The capture circuit is composed of the Capture control register (CAPCON) and the Capture registers (CAPR0, CAPR1) that fetch output from the time base counter.

10.2 Layout of Capture Circuit

Figure 10-1 shows the layout of the capture circuit.

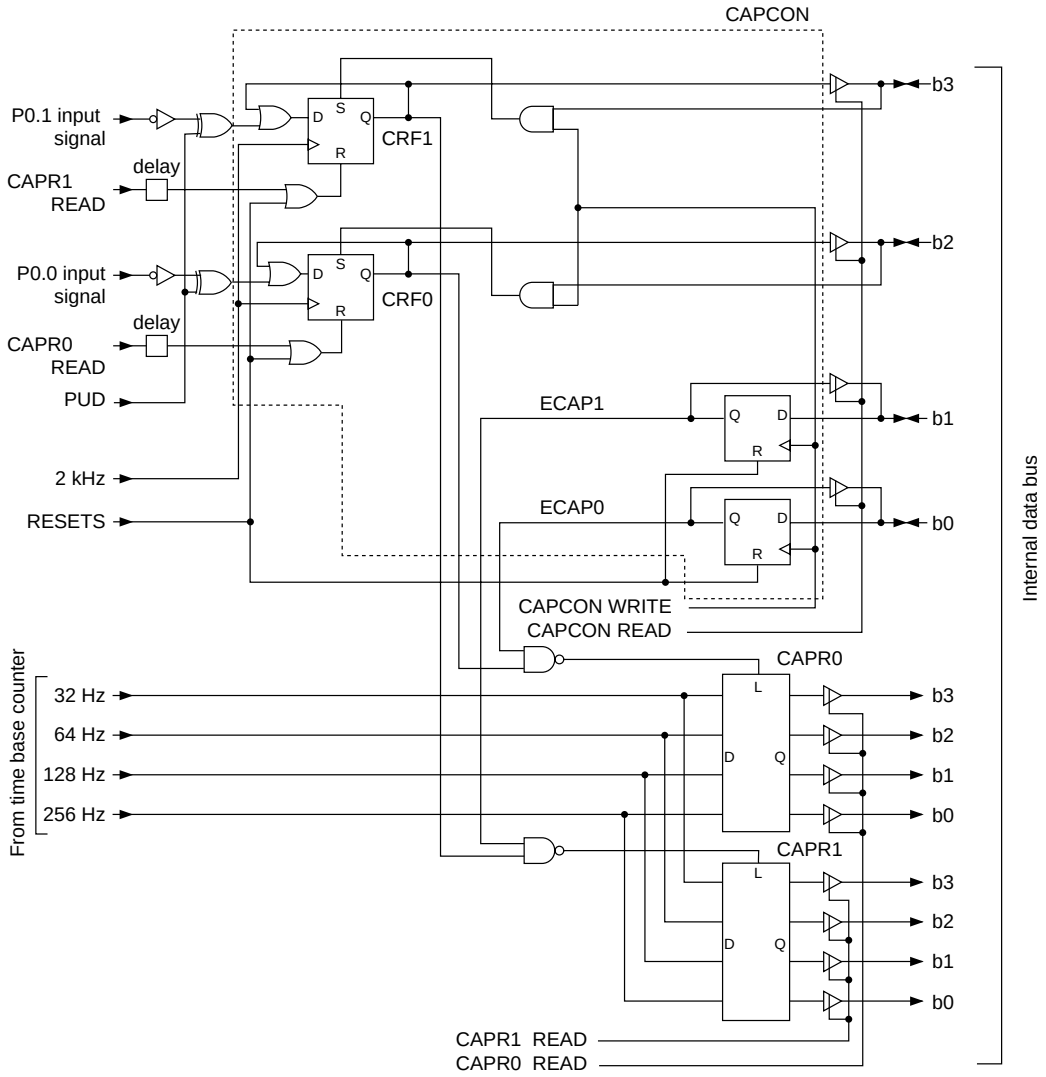


Figure 10-1 Layout of Capture Circuit

10.3 Operation of Capture Circuit

Figure 10-2 shows data latch timing of the Capture data register 0 (CAPR0).

In Figure 10-1, CRF0 is set to "1" at the rising edge of 2 kHz output of the time base counter either when P0.0 input signal becomes "L" level selecting pull-up resistance input or when it becomes "H" level selecting pull-down resistance input while ECAP0 is set to "1" (① in Figure10-2). When CRF0 is set to "1", the latch signal of the Capture data register 0 (CAPR0) becomes "L" level and 32 Hz to 256 Hz of the time base counter is latched to CAPR0 (②). When CAPR0 is read out, CRF0 is reset to "0" (③).

A similar operation is performed when "1" is written to CRF0 even though P0.0 input signal is neither at "L" level nor at "H" level (④).

When ECAP0 is reset to "0" during the latching state, latch operation of CAPR0 is cancelled (⑤).

If the latch signal of CAPR0 is at "H" level (i.e. CRF0 or ECAP0 is reset to "0"), when CAPR0 is read out, 32 Hz to 256 Hz of the time base counter then is read out.

In Figure 10-1, CRF1 is set to "1" at the rising edge of 2 kHz output of the time base counter either when P1.1 of the input port becomes "L" level selecting pull-up resistance input or when it becomes "H" level selecting pull-down resistance input while ECAP1 is set to "1". When CRF1 is set to "1", the latch signal of the Capture data register 1 (CAPR1) becomes "L" level and 32 Hz to 256 Hz of the time base counter is latched to CAPR1. When CAPR1 is read out, CRF1 is reset to "0".

A similar operation is performed when "1" is written to CRF1 even though P0.1 input signal is neither in "L" level nor in "H" level.

If the latch signal of CAPR1 is at "H" level (i.e. CRF1 or ECAP1 is reset to "0"), when CAPR1 is read, 32 Hz to 256 Hz of the time base counter then is read out.

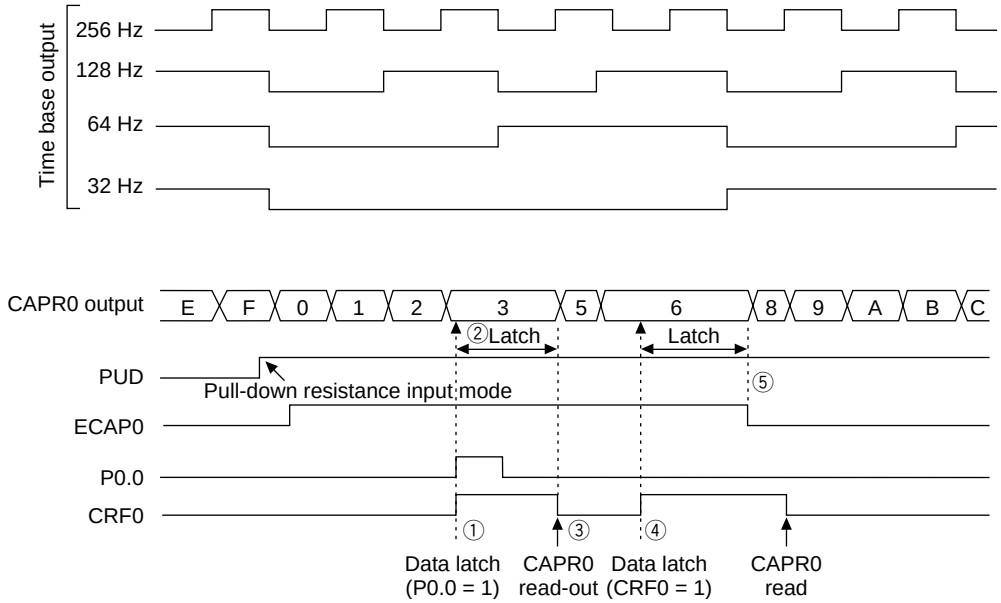
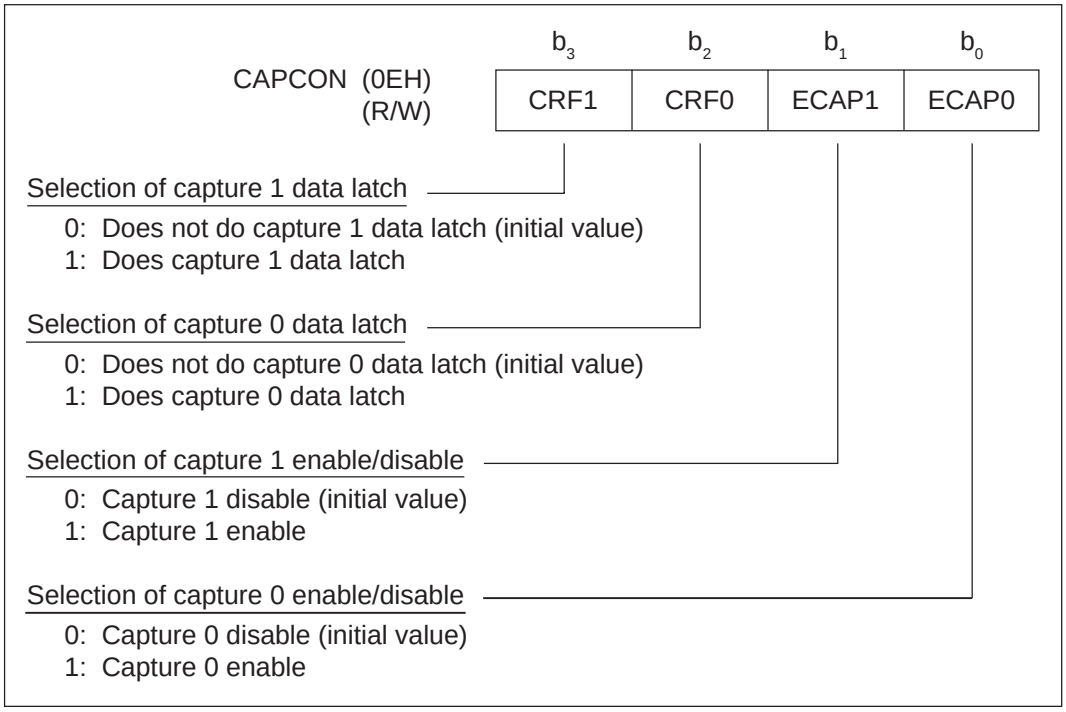


Figure 10-2 Data Latch Timing of Capture Data Register 0 (CAPR0)

10.4 Registers Related to Capture Circuit

(1) Capture control register (CAPCON)

The Capture control register (CAPCON) is a 4-bit special function register (SFR) to control the capture circuit.



Bit 3: CRF1
This bit is the capture flag for the Capture register 1 (CAPR1). CRF1 is set to "1" when P0.1 of the input port detects "L" level selecting pull-up resistance input or when it detects "H" level selecting pull-down resistance input. When CRF1 is set to "1" while ECAP1 is set to "1", 32 Hz to 256 Hz output of the time base counter is latched to CAPR1. When "1" is written to CRF1, a similar operation to the detection of "H" level or "L" level by P0.1 is performed.

CRF1 is reset to "0" when reading out CAPR1. At system reset, CRF1 is reset to "0".

Bit 2: CRF0
This bit is the capture flag for the Capture register 0 (CAPR0). CRF0 is set to "1" when P0.0 of the input port detects "L" level selecting pull-up resistance input or when it detects "H" level selecting pull-down resistance input. When CRF0 is set to "1" while ECAP0 is set to "1", 32 Hz to 256 Hz output of the time base counter is latched to CAPR0. When "1" is written to CRF0, a similar operation to the detection of "H" level or "L" level by P0.0 is performed.

CRF0 is reset to "0" when reading out CAPR0. At system reset, CRF0 is reset to "0".

Bit 1: ECAP1
This bit enables or disables latch of output of the time base counter by the Capture register 1 (CAPR1). When ECAP1 is reset to "0", output of the time base counter is not latched and when CAPR1 is read out, the time base counter value at that time is read out.

When CRF1 is set to "1" while ECAP1 is set to "1", 32 Hz to 256 Hz of the time base counter is latched by CAPR1 and when CAPR1 is read out, the value of latched time base counter is read out.

At system reset, ECAP1 is reset to "0".

Bit 0: ECAP0
This bit enables/disables latch of output of the time base counter by the Capture register 0 (CAPR0). When ECAP0 is reset to "0", output of the time base counter is not latched and when CAPR0 is read out, the time base counter value at that time is read out.

When CRF0 is set to "1" while ECAP0 is set to "1", 32 Hz to 256 Hz of the time base counter is latched by CAPR0 and when CAPR0 is read out, the value of latched time base counter is read out.

At system reset, ECAP0 is reset to "0".

(2) Capture registers (CAPR0, CAPR1)
The capture registers (CAPR0, CAPR1) are 4-bit special function registers (SFRs) to read out latch data of 32 Hz to 256 Hz of the time base counter.

CAPR0 (0CH) (R)

b_3	b_2	b_1	b_0
32Hz	64Hz	128Hz	256Hz

Value of 32 Hz to 256 Hz of time base counter

CAPR1 (0DH) (R)

b_3	b_2	b_1	b_0
32Hz	64Hz	128Hz	256Hz

Value of 32 Hz to 256 Hz of time base counter

Tables 10-1 and 10-2 show the list of capture circuit-related registers and pins.

Table 10-1 List of Capture Circuit-Related Registers

Register name	Symbol	Address	Read/Write	Byte access	Value at system reset
Capture control register	CAPCON	0EH	R/W	No	0H
Capture register 0	CAPR0	0CH	R	Yes	0H
Capture register 1	CAPR1	0DH	R		0H

Table 10-2 Capture Circuit-Related Pins

Pin name	Pin No.		Pad No.	Input/ Output	Note
	GP	GA, TB			
P0.0	77	75	75	Input	Trigger input of CAPR0
P0.1	78	76	76	Input	Trigger input of CAPR1

Chapter 11

Watchdog Timer (WDT)

Chapter 11 Watchdog Timer (WDT)

11.1 Overview

The ML64168 has a built-in watchdog timer to prevent the CPU from crashing. The watchdog timer is composed of a 6-bit watchdog timer (WDT) and a watchdog timer control register (WDTCON) to reset WDT.

11.2 Layout of Watchdog Timer

Figure 11-1 shows the layout of the watchdog timer.

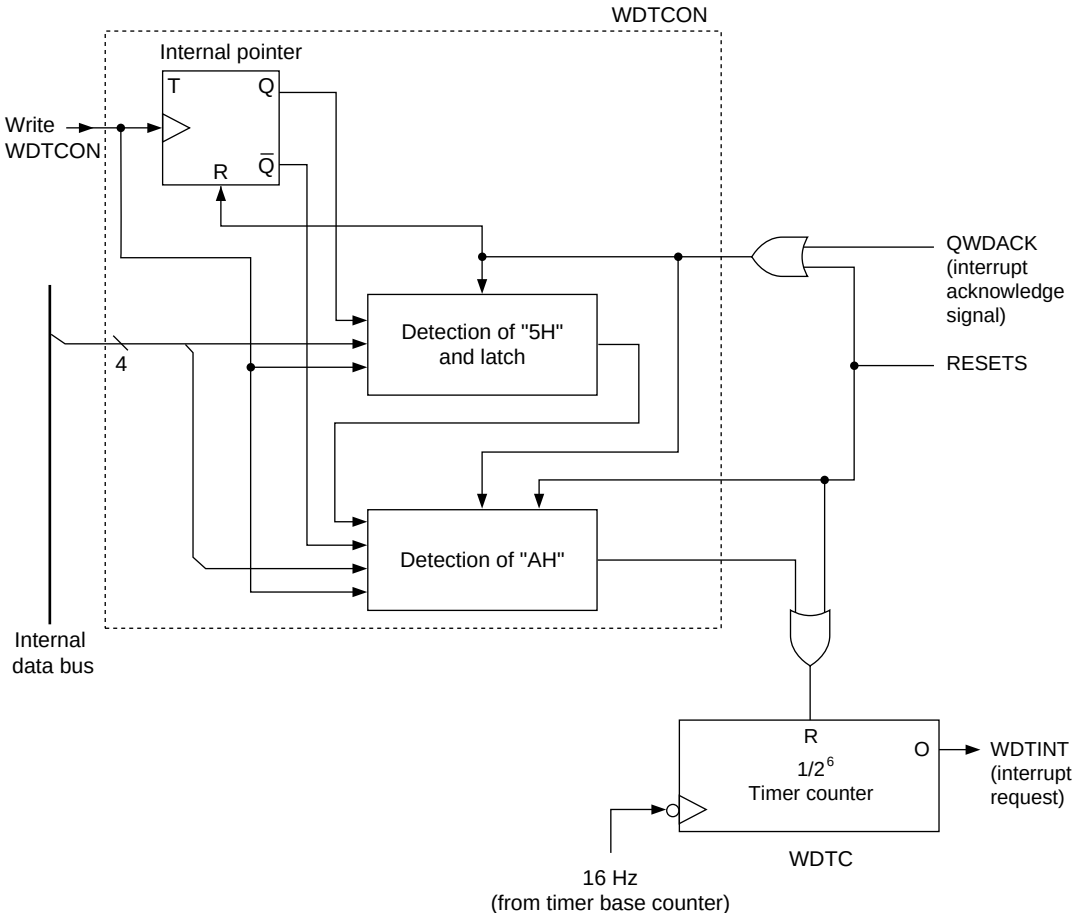


Figure 11-1 Layout of Watchdog Timer

11.3 Operation of Watchdog Timer

When the system reset is released, the Watchdog timer (WDT) is automatically started and the Watchdog timer counter (WDTC) begins count-up. WDTC reset can be performed by writing "5H" and "0AH" alternatively to the Watchdog timer control register (WDTCON).

If WDTC is not reset, WDTC overflows after 1.9 to 2.0 seconds and the Watchdog timer interrupt request (WDTINT) is generated. WDINT is an interrupt that software cannot disable (non-maskable interrupt) and has the highest priority over other interrupts. Normally WDTC is to be programmed to be reset every one second by software. When reset of WDTC is not performed normally by a CPU crash, WDTC overflows and WDTINT is generated. In the watchdog timer interrupt routine, the return operation to a normal routine should be performed from an abnormal state.

Note: The watchdog timer cannot detect all abnormal operations. If WDTC is in reset state, error cannot be detected even if the CPU crashes.

Figure 11-2 shows the reset flowchart of the watchdog timer. As shown in the figure, WDT is reset by writing "5H" when the internal pointer is "0" and writing "0AH" when it is "1" to WDTCON. The internal pointer is reset to "0" at system reset and by WDTC overflow and is reversed each time WDTCON is written.

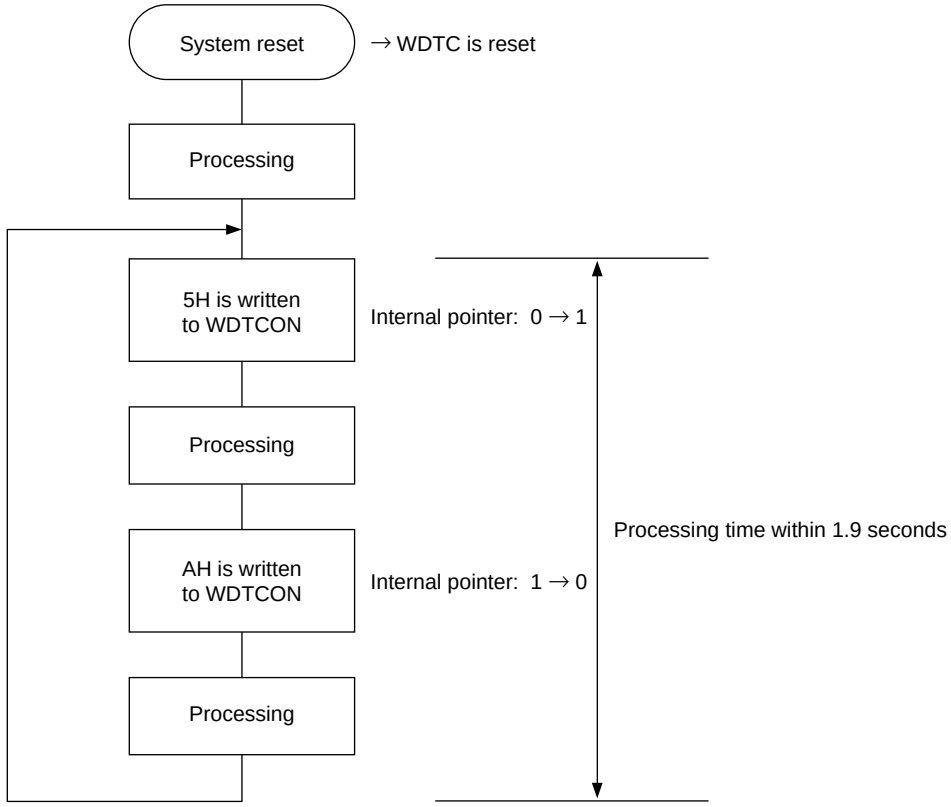


Figure 11-2 Flowchart of Watchdog Timer

Figure 11-3 shows the operation time chart of the watchdog timer.

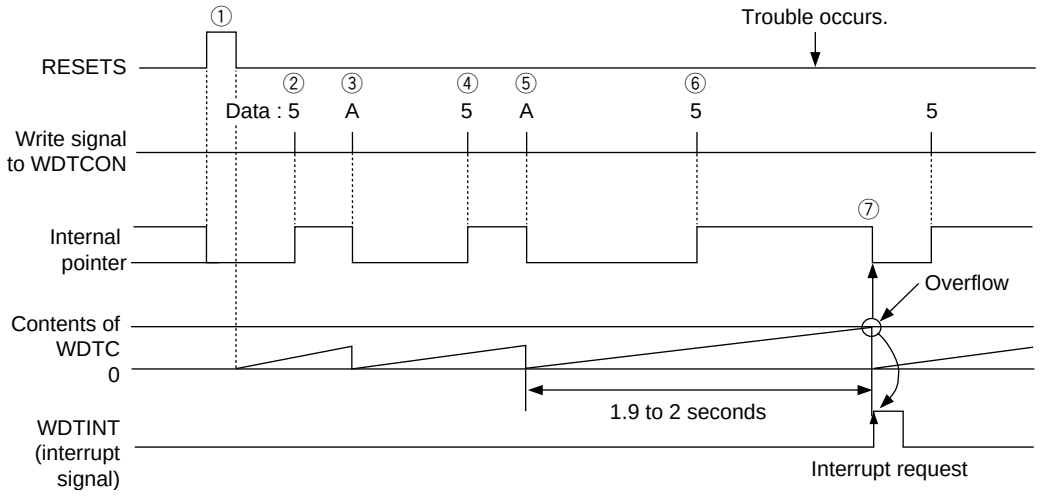


Figure 11-3 Operation Time Chart of the Watchdog Timer

The operation of the watchdog timer is as follows:

① The contents of the internal pointer and the Watchdog timer counter (WDTC) are reset by the system reset (RESETS).

② "5H" is written to WDTCON (internal pointer 0→1).

③ "0AH" is written to WDTCON and the watchdog timer is reset (internal pointer 1→0).

④ "5H" is written to WDTCON (internal pointer 0→1).

⑤ "0AH" is written to WDTCON and the watchdog timer is reset (internal pointer 1→0).

⑥ "5H" is written to WDTCON (internal pointer 0→1).

⑦ When "0AH" is not written to WDTCON while the internal pointer is "1" (i.e. the CPU crashes and the watchdog timer is not reset), the watchdog timer interrupt (WDTINT) is generated by WDTC overflow. The internal pointer becomes "0" then.

11.4 Watchdog Timer Control Register (WDTCON)

The watchdog timer control register (WDTCON) is a 4-bit special function register (SFR) to reset the watchdog timer.

WDTCON (36H) (W)

b_3	b_2	b_1	b_0
d3	d2	d1	d0

Chapter 12

A/D Converter (ADC)

Chapter 12 A/D Converter (ADC)

12.1 Overview

The ML64168 has a built-in 2-channel RC oscillation method A/D converter. The A/D converter is composed of a 2-channel oscillation circuit, Counter A (CNTA0 to 4) which is a 4.8-digit decade counter, Counter B (CNTB0 to 3) which is a 14-bit binary counter and A/D converter control registers 0 and 1 (ADCON0, ADCON1).

By counting oscillation frequencies due to resistance or capacitance connected to the RC oscillation circuit, the A/D converter converts resistance values or capacitance values to corresponding digital values. By using a thermistor or a humidity sensor as a resistance, a thermometer or a hygrometer can be constructed. By applying sensors to the 2-channel RC oscillation circuit, it is also possible to extend measurement ranges or measurement at two places.

12.2 Layout of A/D Converter

Figure 12-1 shows the layout of the A/D converter.

12.3 Operation of A/D Converter

As shown in Figure 12-1, the RC oscillation circuit can be made by connecting resistors and capacitors to each pin.

Counter A (CNTA0 to 4) is a 4.8-digit decade counter ($1/10^4 \times 8$) to count the system clock (CLK) which is the time reference and can count up to a maximum of 79,999.

Counter B (CNTB0 to 3) is a 14-stage binary counter to count the oscillation clock (OSCCLK) of the RC oscillation circuit and can count up to a maximum of 16,383.

Both Counter A and Counter B have the overflow flags (OVFA and OVFB) and overflow output generates the A/D converter interrupt request (ADINT). ADINT due to overflow of either Counter A or Counter B is selected by Bit 1 (SADI) of the A/D converter control register 0 (ADCON0). By resetting SADI to "0", overflow of Counter A is selected and by setting SADI to "1", overflow of Counter B is selected. The vector address of ADINT is at address 02FH.

Bit 0 (EADC) of ADCON0 is a bit to select operation/halt of the A/D conversion. By resetting EADC to "0", the RC oscillation is halted and no counting is performed. By setting EADC to "1", the RC oscillation is begun and counting of the RC oscillation clock and the system clock is started.

Various oscillation mode of the RC oscillation part is performed by the A/D converter control register 1 (ADCON1). The RC oscillation clock can be monitored by outputting to P4.3 in test function. For details of the test functions, refer to Chapter 15 "Test Circuit".

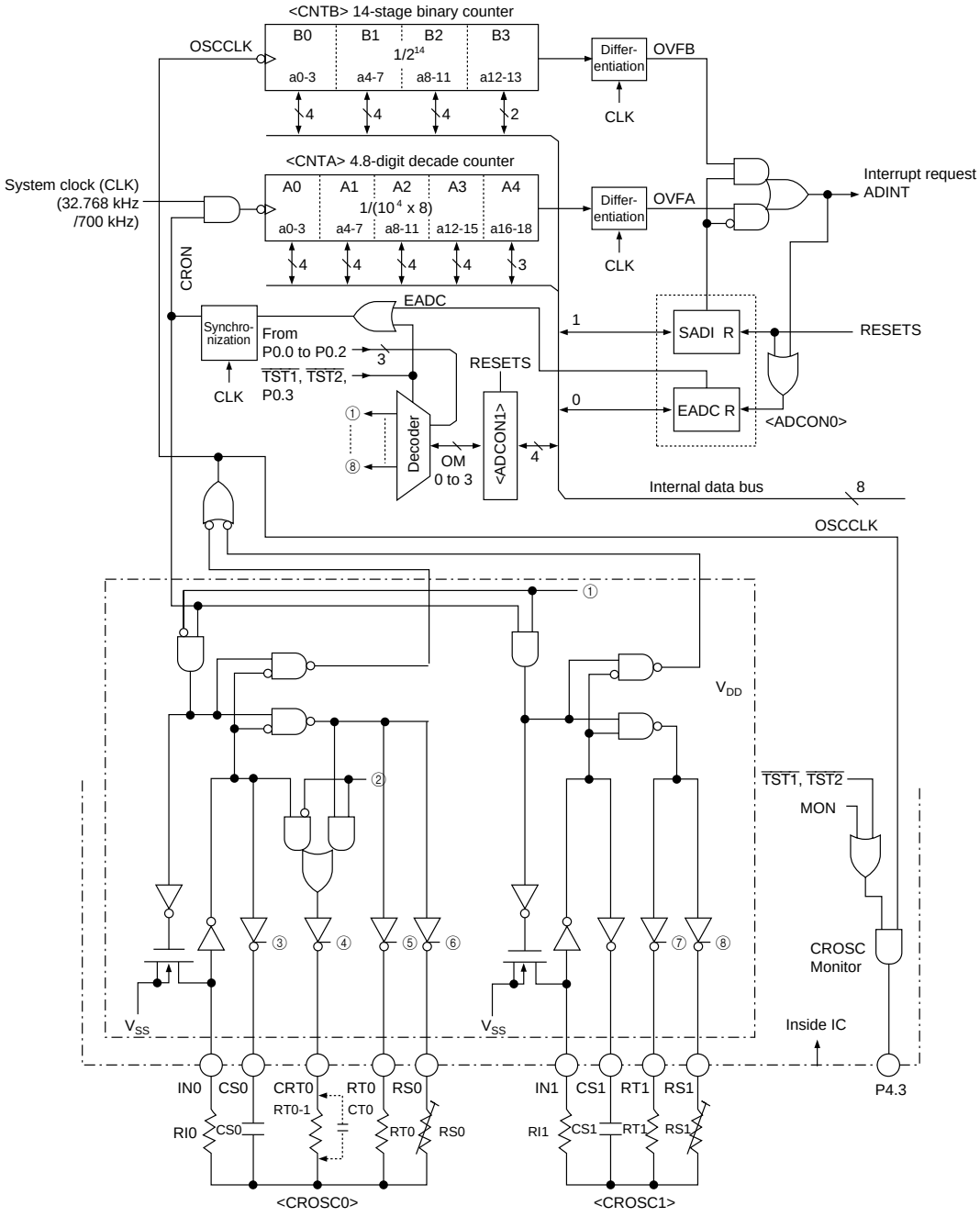


Figure 12-1 Layout of A/D Converter

12.3.1 RC Oscillation Circuit

The A/D converter of the RC oscillation method performs A/D conversion by digitizing the ratio of a reference resistance (or capacitance) to a resistanc sensor, such as thermistor sensor (or capacitance sensor).

By taking the ratio of oscillation frequencies of the reference to the sensor, it is possible to A/D convert the characteristics of a sensor itself by canceling error factors intrinsic to the RC oscillation circuit. Consequently, it is necessary to oscillate the reference side and the sensor side with the same oscillation circuit and a pair of the reference side and the sensor side is usually used.

Table 12-1 shows the oscillation mode by Bits 3 to 0 (OM3 to OM0) of the A/D converter control register (ADCON1). Figures 12-2 to 12-5 show the layout and values of the OM3 to 0 bits.

Table 12-1 Oscillation Mode by OM3 to OM0 Bits

Mode No.	ADCON1				CROSC0 output pins				CROSC1 output pins		Mode	
	OM3	OM2	OM1	OM0	RS0	RT0	CRT0	CS0	RS1	RT1		
0	0	0	0	0	Z	Z	Z	Z	Z	Z	IN0 external clock input mode	
1	0	0	0	1	1/0	Z	Z	0/1	Z	Z	RS0-CS0 oscillation	CROSC0 oscillation mode
2	0	0	1	0	Z	1/0	Z	0/1	Z	Z	RT0-CS0 oscillation	
3	0	0	1	1	Z	Z	1/0	0/1	Z	Z	$RT_{0\text{-}1}$-CS0 oscillation	
4	0	1	0	0	1/0	Z	0/1	Z	Z	Z	RS0-CT0 oscillation	
5	0	1	0	1	Z	Z	Z	Z	1/0	Z	RS1-CS1 oscillation	CROSC1 oscillation mode
6	0	1	1	0	Z	Z	Z	Z	Z	1/0	RT1-CS1 oscillation	
7	0	1	1	1	Z	Z	Z	Z	Z	Z	IN1 external clock input mode	
8	1	—	—	—	Z	Z	Z	Z	Z	Z	—	

Note: Z: High-impedance output

1/0, 0/1: Active output

—: Arbitrary

Modes No.0 and No.7 in Table 12-1 measure the external clock which is input to the IN0 pin or the IN1 pin by halting the operation of the RC oscillation circuit.

As shown in Table 12-1, no two oscillation circuits can operate simultaneously. This prevents interference to the oscillation operation when two are operated simultaneously.

An equation between oscillation frequency (f_{OSCCLK}), capacitance value (C) and resistance value (R).

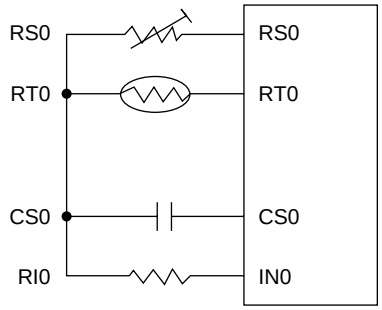
$$\frac{1}{f_{OSCCLK}} = t_{OSCCLK} = k_{OSCCLK} \bullet C \bullet R$$

where t_{OSCCLK} is the period of the oscillation frequency, k_{OSCCLK} is a proportionality constant and C • R is product of C_S or C_T and R_S or R_T. The value of k_{OSCCLK} varies slightly depending on V_{DD} (power supply voltage), RI, C and R and its standard values are listed in Table 12-2.

Table 12-2 Standard Value of k_{OSCCLK} of RC Oscillation Circuit

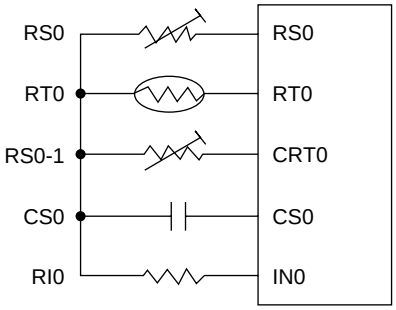
V_{DD} (V)	RIn (kΩ)	CSn, CTn (pF)	RSn, RTn (kΩ)	k_{OSCCLK} (Typ.)
3	10	820	100	2.2
		820	10	2.5
1.5	10	820	100	2.2
		820	10	2.4

Note: n = 0, 1, 0-1



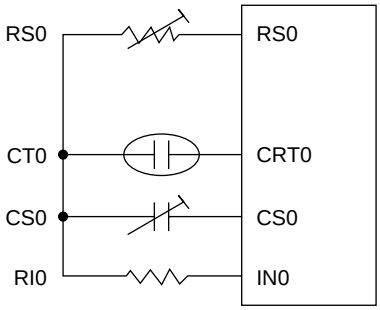
OM3	OM2	OM1	OM0	Oscillation mode
0	0	0	1	Oscillation with reference resistance RS0
0	0	1	0	Oscillation with sensor RT0

Figure 12-2 Measurement of CROSC0 by a Resistance Sensor



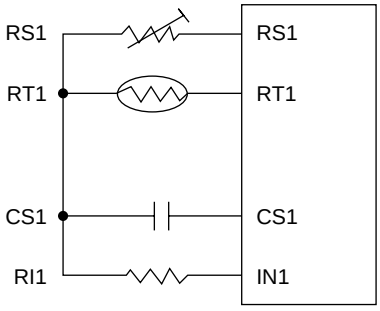
OM3	OM2	OM1	OM0	Oscillation mode
0	0	0	1	Oscillation with reference resistance RS0
0	0	1	0	Oscillation with sensor RT0
0	0	1	1	Oscillation with reference resistance RS_{0-1}

Figure 12-3 Measurement of CROSC0 by a Resistance Sensor (when two-point adjustment with two reference resistances)



OM3	OM2	OM1	OM0	Oscillation mode
0	0	0	1	Oscillation with reference capacitance CS0
0	1	0	0	Oscillation with sensor CT0

Figure 12-4 Measurement of CROSC0 by a Capacitance Sensor



OM3	OM2	OM1	OM0	Oscillation mode
0	1	0	1	Oscillation with reference resistance RS1
0	1	1	0	Oscillation with sensor RT1

Figure 12-5 Measurement of CROSC1 by a Resistance Sensor

Note: Unused pins should be left open.

12.3.2 Counter A/B Reference Mode

The conversion operation of the A/D converter is performed by one of the following two modes.

- Counter A Reference Mode (SADI bit of ADCON0 = 0)
  This is the mode to set gate time by the system clock (CLK) and Counter A, to count the RC oscillation clock (OSCCLK) by Counter B with the gate time and to output contents of Counter B as a digital value.
  The digital value is proportional to the RC oscillation frequency.
- Counter B Reference Mode (SADI bit of ADCON0 = 1)
  This is the mode to set gate time by the RC oscillation clock (OSCCLK) and Counter B, to count the system clock (CLK) by Counter A with the gate time and to output contents of Counter A as a digital value.
  The digital value is inverse proportional to the RC oscillation frequency.

(1) Operation of Counter A Reference Mode

Figure 12-6 shows the operating timing of Counter A reference mode.

Counter A reference mode is performed by the following procedure: (refer to Figure 12-6)

[1] Subtract "nA0" (the count value) from the maximum value + 1 (80,000) and set that value to Counter A (CNTA4 to 0). The count value, "nA0", indicates the gate time.

Counter A ← 80,000 – nA0

[2] Clear Counter B (CNTB3 to 0) to 0000H.

Counter B ← 0000H

[3] Set the OM 3 to 0 bits of ADCON1 to a necessary oscillation mode (refer to Table12-1).

[4] Write "1H" to ADCON0 (SADI = 0, EADC = 1).

Note: The order of [1] to [3] is arbitrary.

By [4], A/D conversion starts.

Counter A starts counting the system clock (CLK) when EADC is set to "1" and the CRON signal that synchronizes with the falling of the system clock is set to "1". When Counter A overflows, [5] the EADC bit is automatically reset and the counting is finished. At the same time, [6] the A/D converter interrupt request signal (ADINT) becomes "1" to generate the A/D converter interrupt request.

When the CRON signal is set to "1", the RC oscillation is started and Counter B starts counting the RC oscillation clock (OSCCLK). When Counter A overflows and the EADC bit is automatically reset, the counting of counter B is finished.

The last count value of "nB0" at Counter B is the count value of OSCCLK during the gate time "nA0 • t_{SYSCLK}" and is expressed by

$$nB0 \doteqdot nA0 \bullet \frac{t_{SYSCLK}}{t_{OSCCLK}} \propto f_{OSCCLK}$$

where t_{SYSCLK} is the period of CLK and t_{OSCCLK} is the period of OSCCLK.

In other words, "nB0" is directly proportional to the RC oscillation frequency (f_{OSCCLK}).

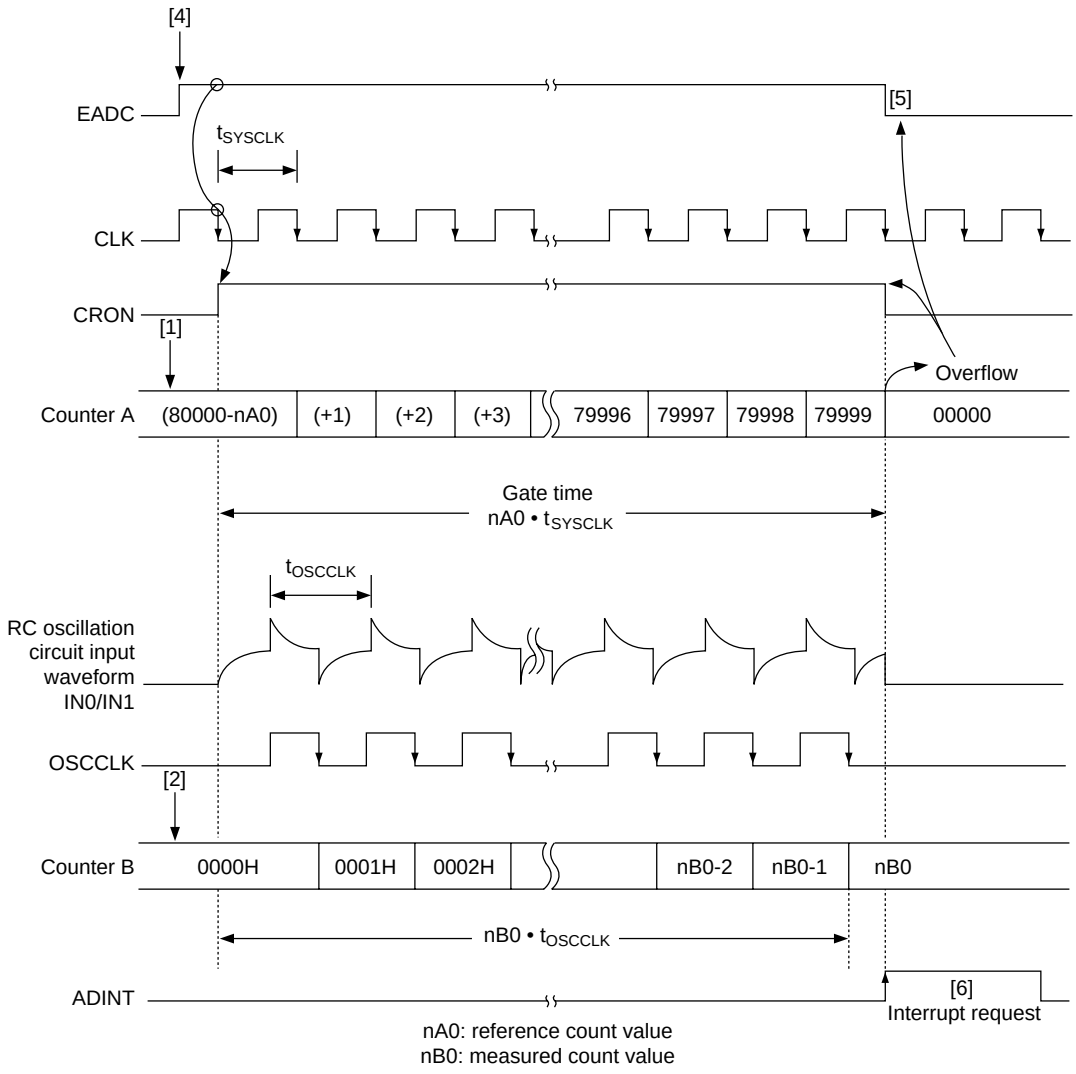


Figure 12-6 Operating Timing of Counter A Reference Mode

(2) Operation of Counter B Reference Mode

Figure 12-7 shows the operating timing of Counter B reference mode.

Counter B reference mode is performed by the following procedure: (refer to Figure 12-7)

[1] Subtract "nB1" (the count value) from the maximum value + 1 (4000H) and set the result to Counter B (CNTB3 to 0). The count value, "nB1", denotes the gate time.

Counter B ← 4000 – nB1

[2] Clear Counter A (CNTA4 to 0) to 0000H.

Counter A ← 0000H

[3] Set the OM 3 to 0 bits of ADCON1 to a necessary oscillation mode (refer to Table 12-1).

[4] Write "3H" to ADCON0 (SADI = 1, EADC = 1).

Note: The order of [1] to [3] is arbitrary.

By [4], A/D conversion starts.

Counter B starts counting the RC oscillation clock (OSCCLK) when the EADC bit is set to "1" and the CRON signal (signal that synchronizes with the falling of the system clock) is set to "1". When Counter B overflows, [5] the EADC bit is automatically reset and the conversion is finished. At the same time, [6] the A/D converter interrupt request signal (ADINT) becomes "1" to generate the A/D converter interrupt request.

When the CRON signal is set to "1", Counter A starts counting the system clock (CLK). When Counter B overflows and the EADC bit is automatically reset, the counting of counter A is finished.

The last count value of "nA1" at Counter A is the count value of SYSCLK during the gate time "nB1• t_{OSCCLK}" and is expressed by

$$nA1 \doteqdot nB1 \bullet \frac{t_{OSCCLK}}{t_{SYSCLK}} \propto \frac{1}{f_{OSCCLK}}$$

In other words, "nA1" is inversely proportional to the RC oscillation frequency (f_{OSC}).

Note: n = 0, 1, 0-1

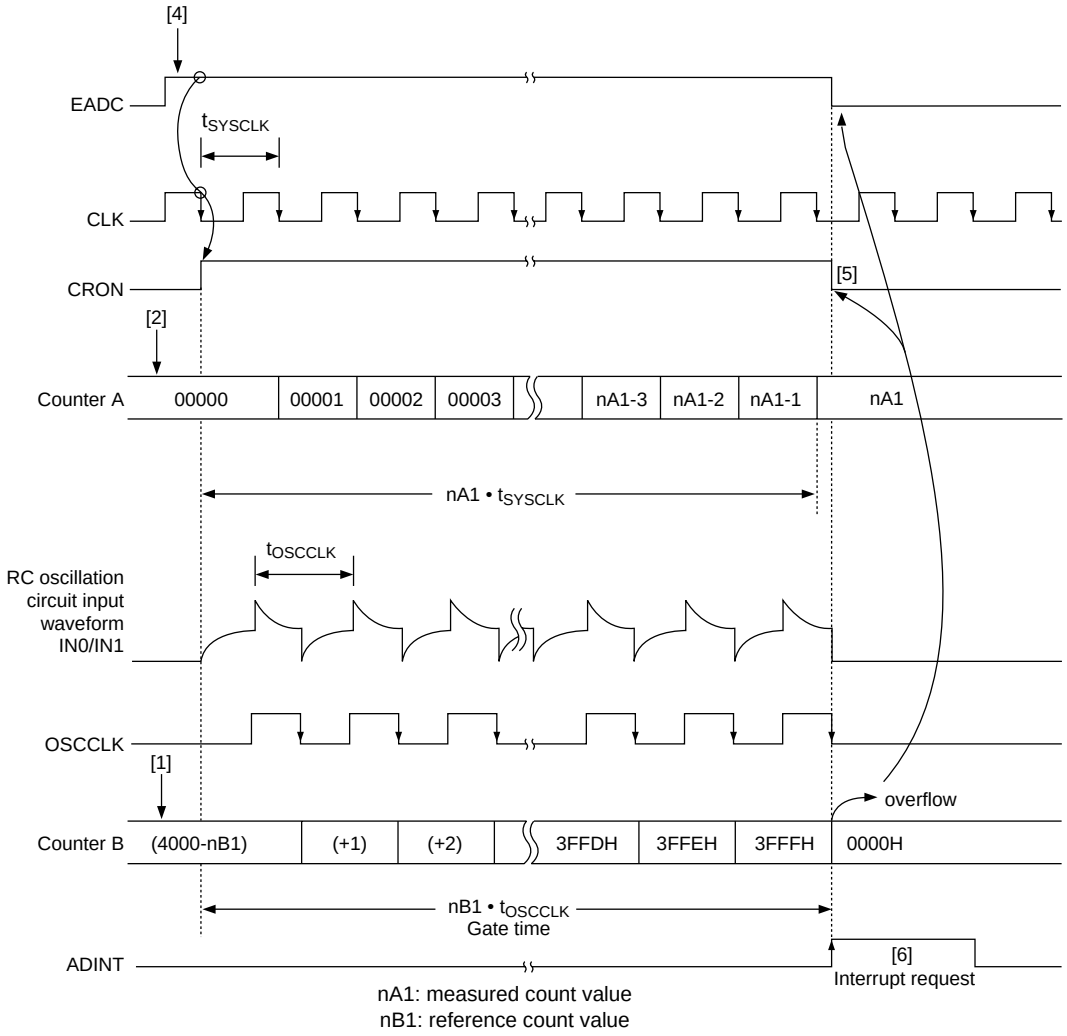


Figure 12-7 Operating Timing of Counter B Reference Mode

12.3.3 Example of Usage of A/D Converter

The method to perform A/D conversion of sensor values by using Counter A reference mode and Counter B reference mode is explained by taking temperature measurement with a thermistor as an example.

Figure 12-8 shows the layout of RC oscillation circuit.

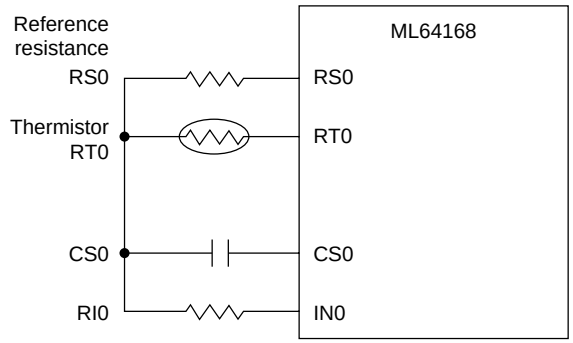


Figure 12-8 Layout of RC Oscillation Circuit of a Thermistor Using CROSC0

Figure 12-9 shows the temperature characteristics of the resistance value, RT0, of the thermistor.

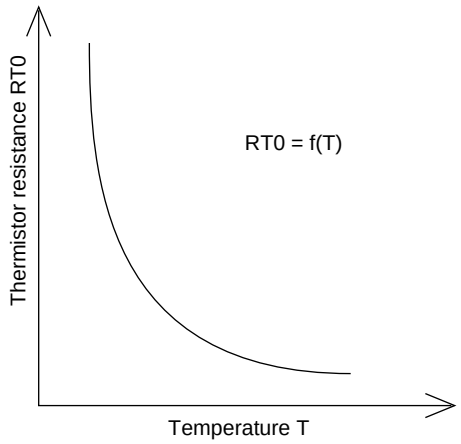


Figure 12-9 Temperature Characteristics of Thermistor

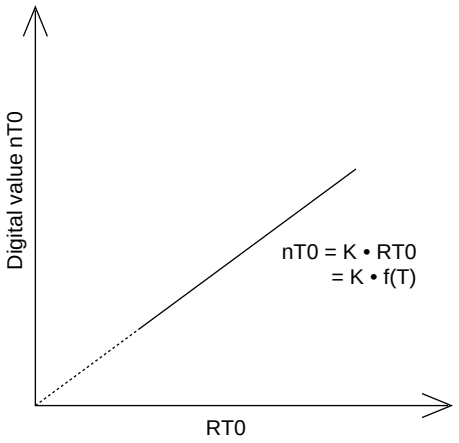


Figure 12-10 A/D Conversion Characteristics

RT0 is expressed as a function of temperature T as

$$RT0 = f(T)$$

Figure 12-10 shows the ideal characteristics of A/D conversion taking RT0 as an analog quantity and the A/D conversion value nT0 is completely proportional to RT0. The value of nT0 is expressed by temperature T and the proportionality factor K as

$$nT0 = K \bullet RT0 = K \bullet f(T) \qquad \text{- - - - - equation (a)}$$

Consequently, by performing conversion processing corresponding to the characteristics shown by Figure 12-9 to nT0, it is possible to express temperatures by digital values.

The conversion method from an analog value of RT0 to a digital value of nT0 is now explained.

To convert RT0 to a digital value, the ratio of oscillation frequencies of RT0 to RS0 (ideal if independent of temperature) is used. This is to cancel the error factors of the oscillation characteristics.

As shown in Figures 12-9 and 12-11, RT0 depends on temperature T and RS0 is always constant regardless of temperature T. The oscillation characteristics, f_{OSC}-T, using these resistances is ideal if the solid lines of Figures 12-12 and 12-13 can be realized. However, in reality, the dotted lines are obtained due to error factors of the temperature characteristics of the IC and others. Since the conditions of f_{OSC}(RT0) and f_{OSC}(RS0) are about the same except the resistance, their error should be similar each other and consequently, if the ratio of one to the other is taken, the error should be canceled.

The ratio of f_{OSC}(RT0) to f_{OSC}(RS0) corresponds to the A/D conversion value of nT0 which, ideally, depends solely on RT0.

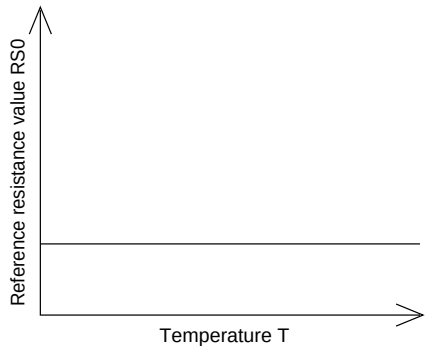


Figure 12-11 Temperature Characteristics of Thermistor

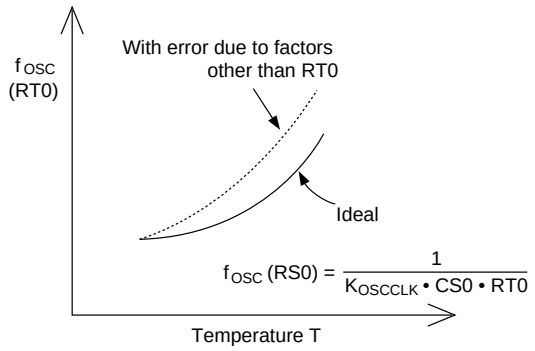


Figure 12-12 Oscillation Characteristics of Thermistor

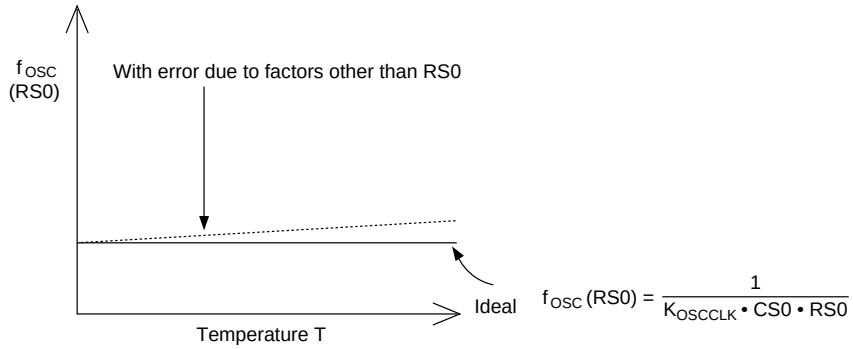


Figure 12-13 Oscillation Characteristics of Reference Resistance

Figure 12-14 shows the conversion to digital values from the RT0 values, i.e. one cycle time chart of temperature measurement.

One cycle of A/D conversion needs to be composed of two steps shown in Figure 12-14 because the reference resistance and the thermistor must be oscillated independently when taking the ratio of them.

In this example, those two steps are taken by the following combination:

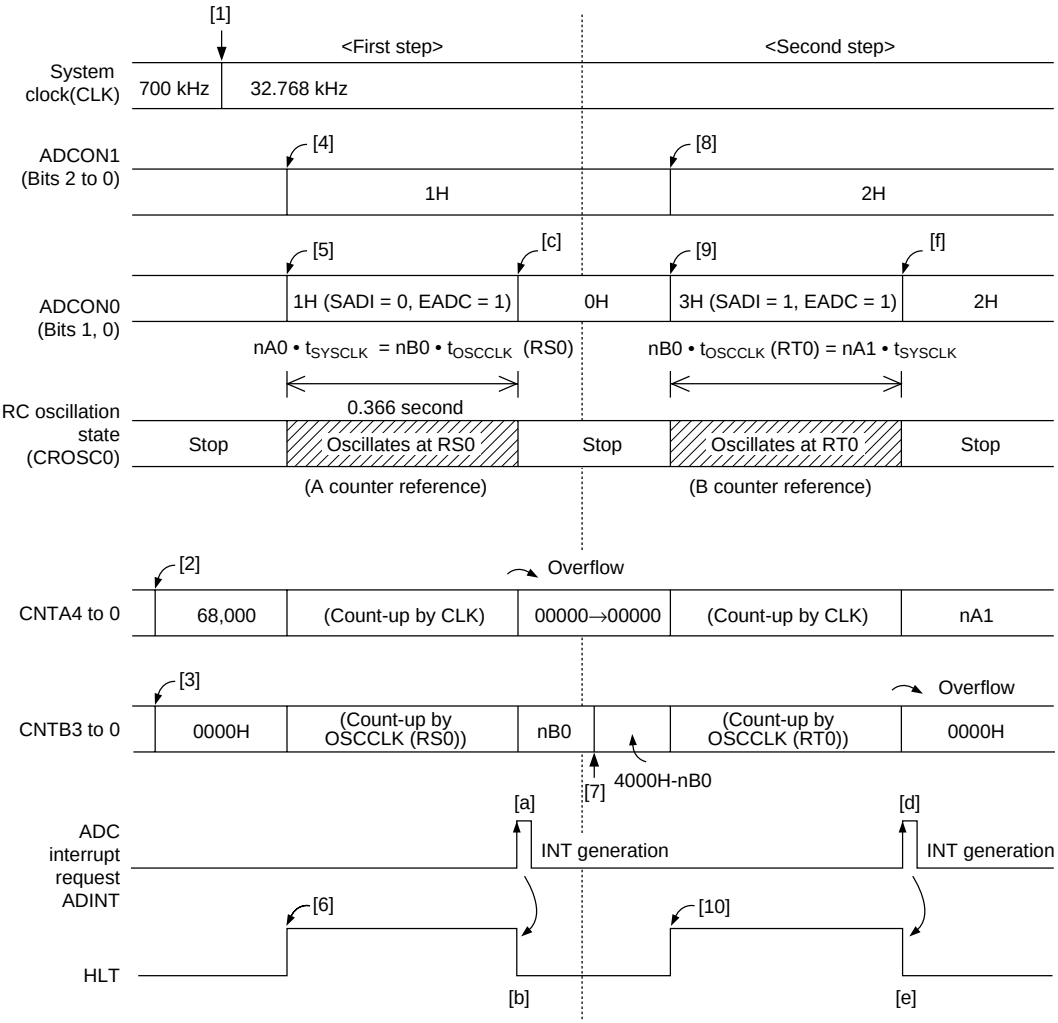
- First step = RC oscillation by RS0 with A counter reference
- Second step = RC oscillation by RT0 with B counter reference

Various other methods are possible besides the one above.

In the above method, the operating time by the second step varies by the value of thermistor RT0. However, if it is necessary to avoid such variation, the following combination is recommended:

- First step = RC oscillation by RS0 with B counter reference
- Second step = RC oscillation by RT0 with A counter reference

In the following, the procedure of A/D conversion will be explained taking Figure 12-14 as an example.



Notes: nA0 = 12,000, t_{SYSCLK} = 1/32768 Hz, [1] to [10]: processing by software, [a] to [f] : processing by hardware

Figure 12-14 Time Chart of One Cycle of Temperature Measurement

<First Step>

[1] Set the system clock to 32.768 kHz (Write 0H to FCON), if using 400 kHz clock as system clock.

[2] Set "80,000-nA0" to Counter A.

Note: nA0 is taken as 12,000 in order to set the gate time nA0 • t_{SYSCLK} of oscillation mode of the reference resistance RS0 as 0.366 second. The value of nA0 depends on the size of quantum error of A/D conversion and the larger nA0, the smaller the error.

[3] Clear Counter B to "0000H".

[4] Write "1H" to ADCON1 and set it to oscillation mode with reference resistance RS0.

Note: The order of [1] to [4] is arbitrary.

[5] Write "1H" to ADCON0 and start A/D conversion in Counter A reference mode.

[6] Set the HLT bit of HALT register to "1" for halt mode.

Note: By selecting halt mode, noise to the RC oscillation circuit may be reduced. In regular usage, halt mode is recommended during RC oscillation operation.

The RC oscillation circuit (CROSC0) continues oscillation with reference resistance RS0 for about 0.366 second at this time and when Counter A overflows, [a] the ADINT signal is set to "1" and the A/D converter interrupt request is generated. By the generation of the interrupt request, [b] halt mode is released and [c] the A/D conversion operation is stopped (the EADC bit = 0). At this moment, Counter A is in 00000 state.

The contents of Counter B are expressed as

$$nB0 = nA0 \cdot \frac{t_{SYSCLK}}{t_{OSCCLK(RS0)}} \qquad \text{- - - - - equation (b)}$$

<Second Step>

[7] Calculate "4000H-nB0" by the contents "nB0" of Counter B and set that value to Counter B.

Note: Although clearing of Counter A is needed, additional processing is not necessary as it is already in "00000" state.

[8] Write "2H" to ADCON1 and start oscillation mode with thermistor RT0.

[9] Write "3H" to ADCON0 and start A/D conversion in Counter B reference mode.

[10] Set the HLT bit of HALT register to "1" to start halt mode.

The RC oscillation circuit (CROSC0) oscillates with thermistor RT0 from this time until overflow of Counter B. This period is equivalent to product of "nB0" from first step and $t_{OSCCLK(RT0)}$ due to RT0.

When Counter B overflows, [d] the ADINT signal is set to "1" and the A/D converter interrupt request is generated. By the generation of the interrupt request, [e] halt mode is released and [f] the A/D conversion operation is stopped (the EADC bit = "0").The contents of Counter A becomes the A/D conversion value of nA1 and is expressed by the following:

$$nA1 = nB0 \cdot \frac{t_{OSCCLK(RT0)}}{t_{SYSCLK}} \qquad \text{- - - - - equation (c)}$$

By equations (b) and (c), nA1 is expressed as

$$nA1 = nA0 \cdot \frac{t_{OSCCLK(RT0)}}{t_{OSCCLK(RS0)}} \qquad \text{- - - - - equation (d)}$$

where $t_{OSCCLK\ (RS0)}$ is the period of the oscillation clock by reference resistance RS0 and $t_{OSCCLK\ (RT0)}$ is the period of the oscillation clock by thermistor RT0.

The oscillation period is expressed ideally as

$$t_{OSCCLK\ (RS0)} = k_{OSCCLK} \cdot CS0 \cdot RS0$$
$$t_{OSCCLK\ (RT0)} = k_{OSCCLK} \cdot CS0 \cdot RT0 \qquad \text{- - - - - equation (e)}$$

By substituting equation (e) to equation (d), nA1 is expressed as

$$nA1 = nA0 \cdot \frac{RT0}{RS0}$$

As "nA0" (12,000 in this example) and RS0 are fixed constants, "nA1" becomes a digital value proportional to RT0. This "nA1" is equivalent to "nT0" in equation (a).

The obtained "nA1" must be further converted to a temperature display value depending on the temperature-resistance characteristics of the thermistor in a program.

12.3.4 RC Oscillation Monitor

By setting Bit 2 (MON) of the Port 43 control register (P43CON) to "1", the RC oscillation clock (OSCCLK) can be output to P4.3.

By using the test functions, the RC oscillation clock can be output at P4.3 without using software. For details of the test functions, refer to Chapter 15 "Test Circuit".

The RC oscillation monitor is useful when checking the characteristics of the RC oscillation circuit. For instance, it is possible to measure the relationship between sensors such as a thermistor and an oscillation frequency. For example, by examining the relationship between ambient temperature of a thermistor built-in RC oscillation circuit and oscillation frequencies of the thermistor RT0 and the reference resistance RS0, it is possible to obtain the conversion coefficient from the value of nA1 to the temperature display values.

12.4 Registers Related to A/D Converter

(1) A/D converter control register 0 (ADCON0)

The A/D converter control register 0 (ADCON0) is a 4-bit special function register (SFR) that selects start/stop of RC oscillation of the A/D converter and the A/D converter interrupt by Counter A or Counter B.

ADCON0 (2AH) (R/W)

b_3	b_2	b_1	b_0
-----*	-----*	SADI	EADC

Selection of A/D interrupt
- 0: Interrupt request by Counter A overflow (initial value)
- 1: Interrupt request by Counter B overflow

Selection of A/D conversion start/stop
- 0: Stop of RC oscillation (initial value)
- 1: RC oscillation start

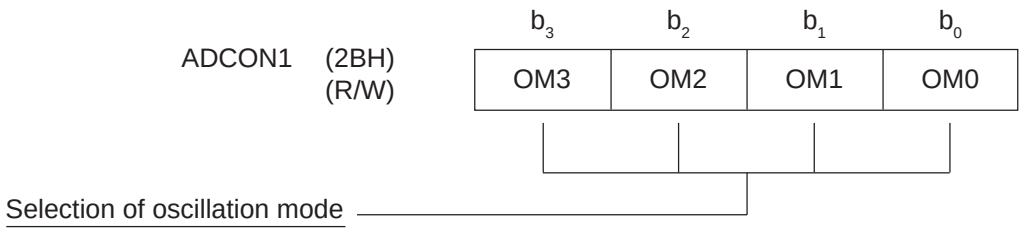
*Reserved bit: "1" is always read. Not valid for write.

Bit 1: SADI
This bit selects the A/D converter interrupt request (ADINT) by overflow of either Counter A or Counter B. By resetting SADI to "0", the interrupt request by overflow of Counter A is selected and by setting SADI to "1", the interrupt request by overflow of Counter B is selected. At system reset, SADI is reset to "0".

Bit 0: EADC
This bit selects start/stop of conversion of the A/D converter. When set to "1", A/D conversion is started and when reset to "0", A/D conversion is stopped. When either Counter A or Counter B overflows while EADC is set to "1" to start counting, the EADC bit is set to "0" automaticaly. Consequently, EADC indicates that the measurement is in progress. At system reset, the EADC bit is reset to "0" and the system is in stop state.

(2) A/D converter control register 1 (ADCON1)

The A/D converter control register 1 (ADCON1) is a 4-bit special function register (SFR) to select oscillation mode of the RC oscillation circuit.



OM0	OM1	OM2	OM3	
0	0	0	0	0 : IN0 pin external clock input mode (initial value)
0	0	0	1	1 : RS0-CS0 oscillation mode
0	0	1	0	0 : RT0-CS0 oscillation mode
0	0	1	1	1 : RT(0-1)-CS0 oscillation mode
0	1	0	0	0 : RS0-CT0 oscillation mode
0	1	0	1	1 : RS1-CS1 oscillation mode
0	1	1	0	0 : RT1-CS1 oscillation mode
0	1	1	1	1 : IN1 pin external clock input mode
1	-	-	-	- : Unavailable

(3) A/D converter counter A registers (CNTA0 to 4)

The A/D converter counter A registers (CNTA0 to 4) are 4-bit special function registers (SFRs) to read/write the Counter A.

Note: CNTA0 to CNTA3 are decimal counters and can handle only data from 0H to 9H.

CNTA0 (20H) (R/W)

b_3	b_2	b_1	b_0
a3	a2	a1	a0

Bits 0 to 3 of Counter A

CNTA1 (21H) (R/W)

b_3	b_2	b_1	b_0
a7	s6	a5	a4

Bits 4 to 7 of Counter A

CNTA2 (22H) (R/W)

b_3	b_2	b_1	b_0
a11	a10	a9	a8

Bits 8 to 11 of Counter A

CNTA3 (23H) (R/W)

b_3	b_2	b_1	b_0
a15	a14	a13	a12

Bits 12 to 15 of Counter A

CNTA4 (24H) (R/W)

b_3	b_2	b_1	b_0
-----*	a18	a17	a16

Bits 16 to 18 of Counter A

*Reserved bit: "1" is always read. Not valid for write.

(4) A/D converter counter B registers (CNTB0 to 3)

The A/D converter counter B registers (CNTB0 to 3) are 4-bit special function registers (SFRs) to read/write the Counter B.

CNTB0 (26H) (R/W)

b_3	b_2	b_1	b_0
b3	b2	b1	b0

Bits 0 to 3 of Counter B

CNTB1 (27H) (R/W)

b_3	b_2	b_1	b_0
b7	b6	b5	b4

Bits 4 to 7 of Counter B

CNTB2 (28H) (R/W)

b_3	b_2	b_1	b_0
b11	b10	b9	b8

Bits 8 to 11 of Counter B

CNTB3 (29H) (R/W)

b_3	b_2	b_1	b_0
-----*	-----*	b13	b12

Bits 12 and 13 of Counter B

*Reserved bit: "1" is always read. Not valid for write.

Tables 12-3 and 12-4 list A/D converter-related registers and pins.

Table 12-3 List of A/D Converter-Related Registers

Register name	Symbol	Address	Read/Write	Byte access	Value at system reset
A/D converter control register 0	ADCON0	2AH	R/W	Yes	0CH
A/D converter control register 1	ADCON1	2BH	R/W		0H
A/D converter counter A register 0	CNTA0	20H	R/W	Yes	0H
A/D converter counter A register 1	CNTA1	21H	R/W		0H
A/D converter counter A register 2	CNTA2	22H	R/W	Yes	0H
A/D converter counter A register 3	CNTA3	23H	R/W		0H
A/D converter counter A register 4	CNTA4	24H	R/W	No	8H
A/D converter counter B register 0	CNTB0	26H	R/W	Yes	0H
A/D converter counter B register 1	CNTB1	27H	R/W		0H
A/D converter counter B register 2	CNTB2	28H	R/W	Yes	0H
A/D converter counter B register 3	CNTB3	29H	R/W		0CH

Table 12-4 List of A/D Converter-Related Pins

Pin name	Pin No.		Pad No.	Input/Output	Note
	GP	GA, TB			
RT0	33	31	31	Output	Resistance sensor connection pin to measure Channel 0
CRT0	34	32	32	Output	Resistance/capacitance sensor connection pin to measure Channel 0
RS0	35	33	33	Output	Reference resistance connection pin for Channel 0
CS0	36	34	34	Output	Reference capacitance connection pin for Channel 0
IN0	37	35	35	Input	Oscillation input pin for Channel 0
RT1	41	39	39	Output	Resistance sensor connection pin to measure Channel 1
RS1	40	38	38	Output	Reference resistance connection pin for Channel 1
CS1	39	37	37	Output	Reference capacitance connection pin for Channel 1
IN1	38	36	36	Input	Oscillation input pin for Channel 1

Chapter 13

LCD Driver (LCD)

Chapter 13 LCD Driver (LCD)

13.1 Overview

The ML64168 has a built-in LCD driver.

There are three types of driving methods, i.e. 1/4 duty, 1/3 duty and 1/2 duty. Maximum of 120 segments can be driven for 1/4 duty, 93 segments for 1/3 duty and 64 segments for 1/2 duty, respectively.

The mask option can select either a common driver or a segment driver for each LCD driver. The mask option can also specify assignment of each bit of the display register to each segment.
On the one hand, all the display resisters to be used must be selected by the mask option. If not, note that the display registers can not be used.
Refer to Appendix F on the mask options.

L26 to L33 of the LCD driver can become output ports by the mask option.

The following is the relation among the duty, the bias method and the maximum segment number.

1/4 duty 1/3 bias method - 120 segments
1/3 duty 1/3 bias method - 93 segments
1/2 duty 1/2 bias method - 64 segments

13.2 Layout of LCD Driver

The layout of the LCD driver is shown in Figure 13-1. Figures 13-2 and 13-3 show the LCD driver and its peripheral circuits.

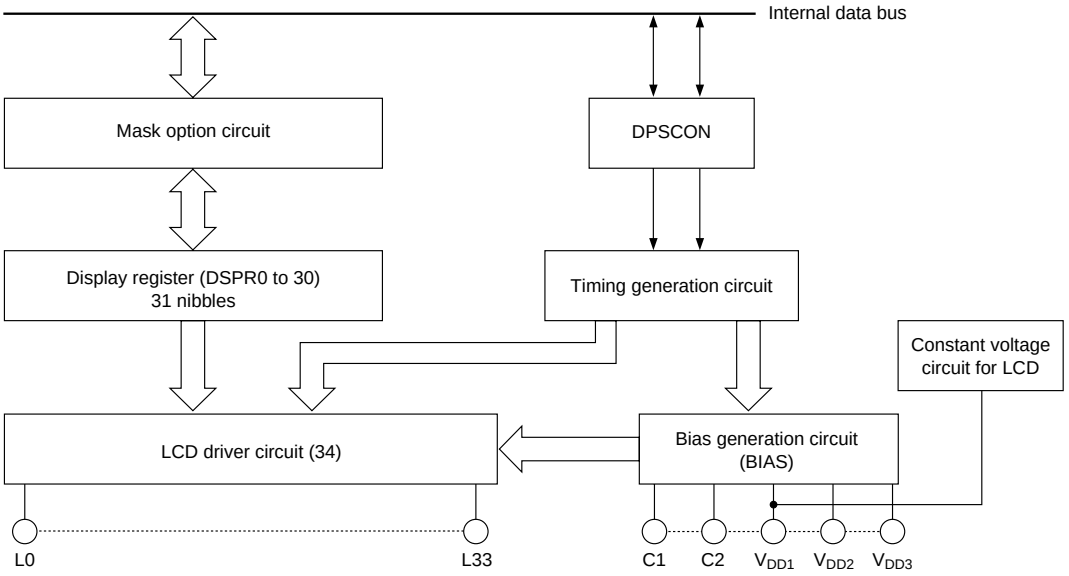


Figure 13-1 Layout of LCD Driver

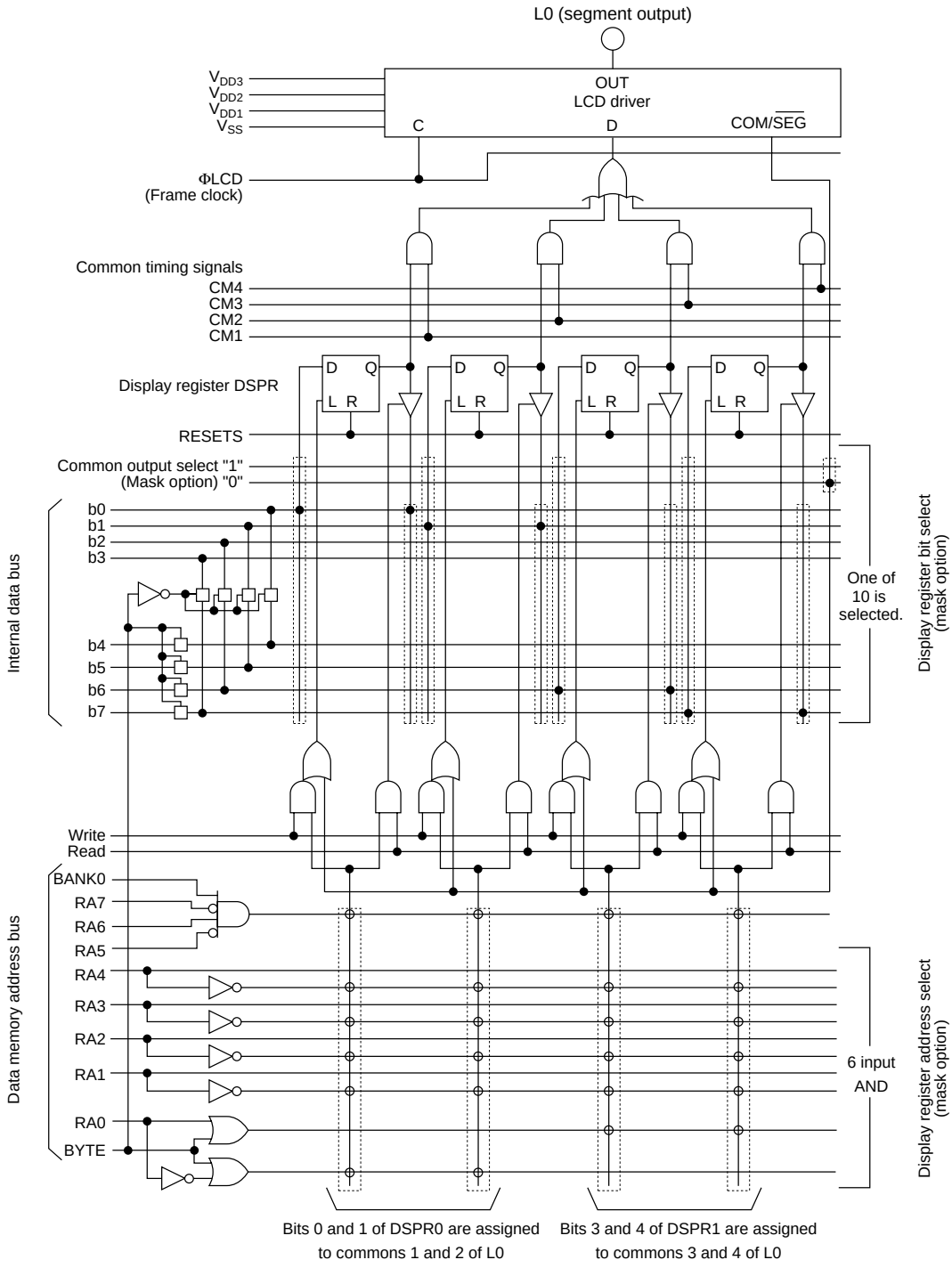


Figure 13-2 LCD Driver and Display Register (Circuit layout of L0 to L25: One output)

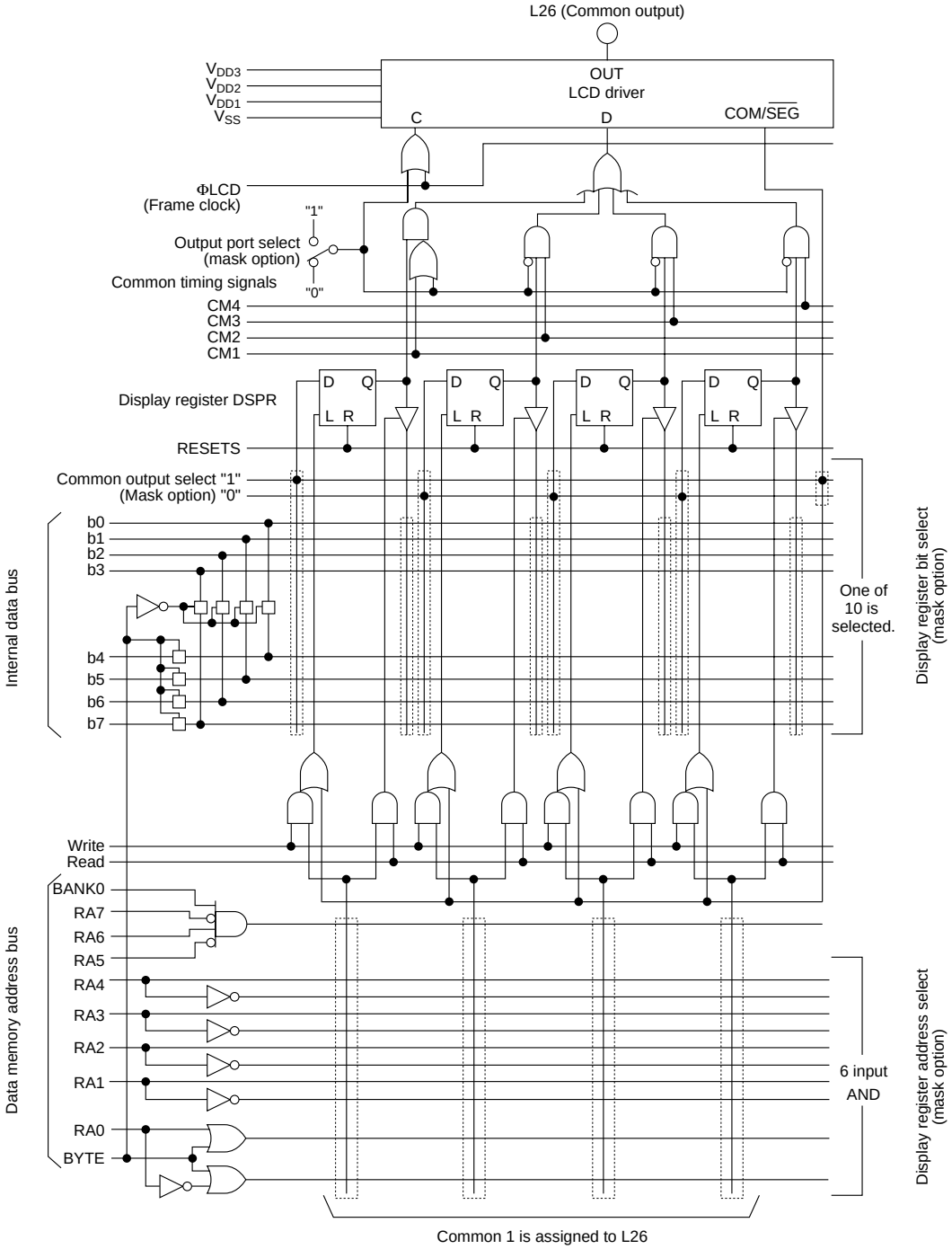


Figure 13-3 LCD Driver and Display Register (Circuit layout of L26 to L33: One output)

13.3 Operation of LCD Driver

The LCD driver outputs LCD square waveforms based on data written to the display registers.

The mask option can select the address of the display register, bit assignment and a segment driver/a common driver.

4 segment display registers per one segment driver are assigned. All the 4 segments are used for 1/4 duty, 3 segments for 1/3 duty and 2 segments for 1/2 duty, respectively.

In Figure 13-2, the L0 output is the segment driver. Bits 0 and 1 of DSPR0 are assigned to the segment corresponding to Commons 1 and 2 and Bits 2 and 3 of DSPR1 are assigned to the segment corresponding to Commons 3 and 4. In Figure 13-3, the L26 output is the common 1 driver. Thus, it is possible to assign arbitrary display registers and bits to arbitrary segment by the mask option.

Duty of the LCD driver is selected by the display control register (DSPCON).

13.4 Display Control Register (DSPCON)

The display control register (DSPCON) is a 4-bit special function register (SFR) to control the duty ratio of the LCD driver.

DSPCON (1EH) (R/W)

b_3	b_2	b_1	b_0
-----*	-----*	DUTY1	DUTY0

Duty selection

DUTY1 DUTY0
- 0 0 : 1/4 duty (initial value)
- 0 1 : 1/3 duty
- 1 0 : 1/2 duty
- 1 1 : disabled

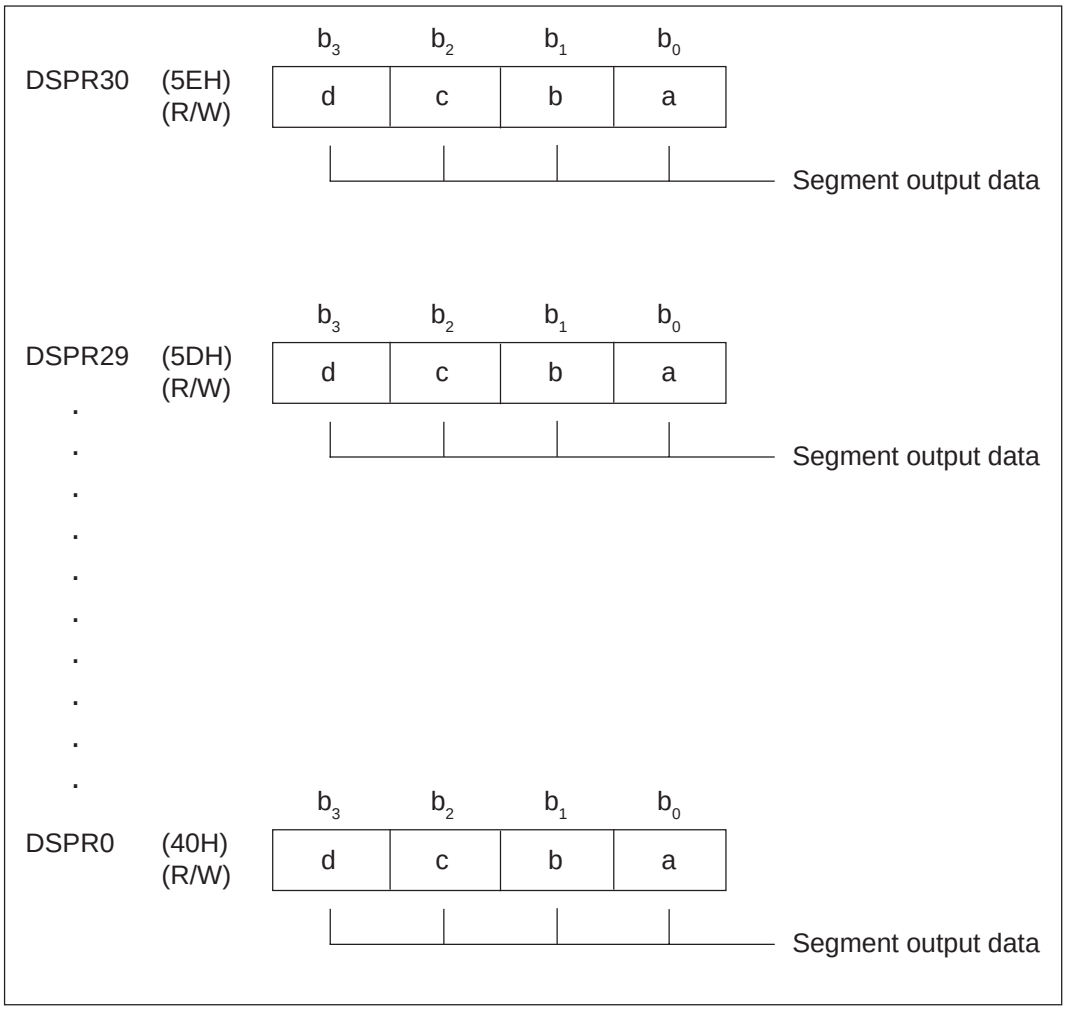
*Reserved bit: "1" is always read out. Not valid for write.

Bits 1 and 0: DUTY1, DUTY0

DUTY1 and DUTY0 are bits to select the duty ratio of the LCD driver. They are reset to "0" at system reset and 1/4 duty is selected. Setting both DUTY1 and DUTY0 to "1" is disabled.

13.5 Display Registers 0 to 30 (DSPR0 to 30)

The display registers 0 to 30 (DSPR0 to 30) are data registers for segment output of the LCD driver. They are assigned to addresses 40H to 5EH of Bank 0.



It is possible to assign an arbitrary bit of the display register to an arbitrary segment driver by the mask option. At system reset, all the display registers are reset to "0" and LCD segments are all off. Those bits set to "1" in the display register are in on state on the LCD segment while those bits reset to "0" are in off state.

For details of assignment of each bit of the display register for the display segment, refer to "List of LCD Driver Mask Option" in "Appendix F: Mask Options".

13.6 Output Port Selection by Mask Option

Each of the 8 pins of L26 to L33 of the LCD driver can be selected as an output port by the mask option. When these pins are selected as output ports, one port pin is assigned to one bit of the display register. Figure 13-4 shows an example of assigning DSPR0 to L26 to L29 as an output port using an equivalent circuit. The output voltage level at this time is at the V_{DD} level at "H" output and is at the V_{SS} level when outputting "L".

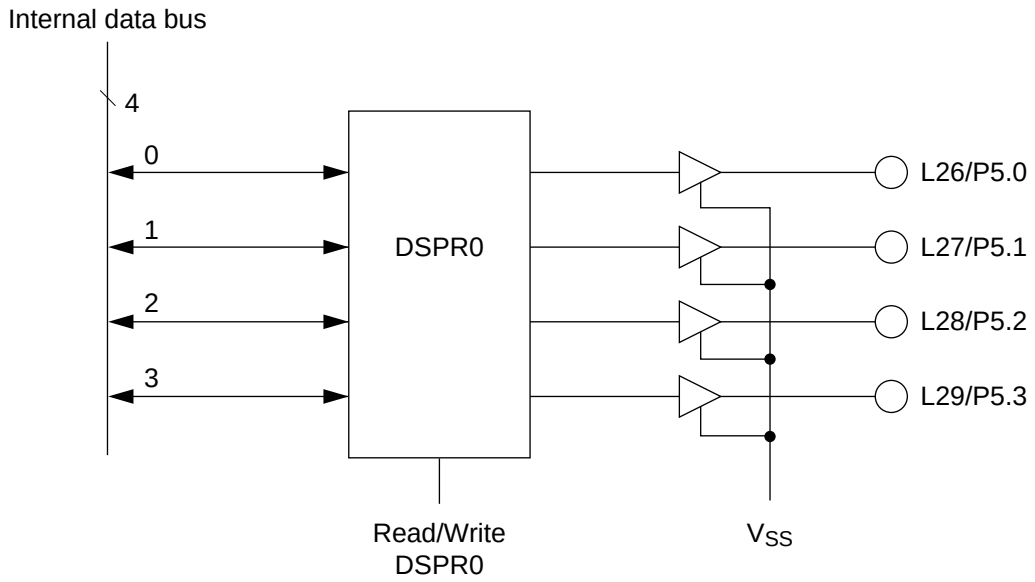


Figure 13-4 Equivalent Circuit when DSPR0 is Assigned to L26 to L29 as an Output Port

Only DSPR0 and DSPR1 can be used as output ports. Other registers cannot be used as output ports.

For bit assignment of the display register for output pins and selection of output ports, refer to "List of LCD Driver Mask Options" in "Appendix F: Mask Options".

13.7 Bias Generation Circuit for LCD Driver (BIAS)

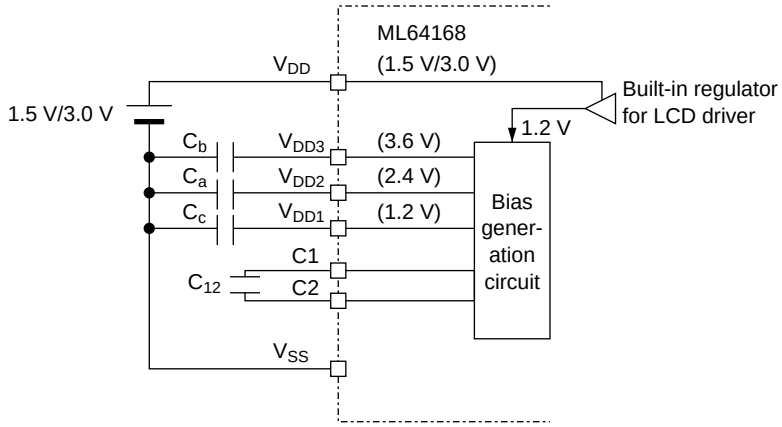
The bias generation circuit for LCD driver (BIAS) generates bias voltages.

Either power supply voltage or built-in regulator output voltage can be selected by mask option as the bias reference voltage for LCD driver.

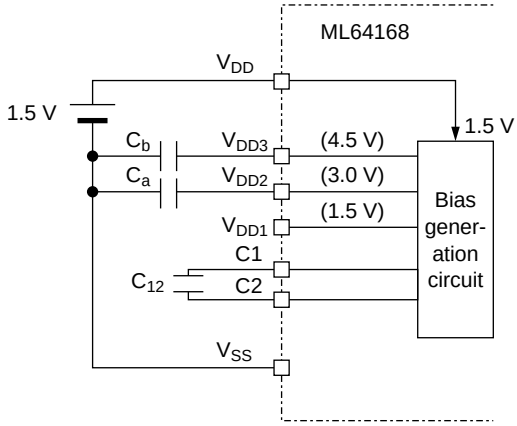
Table 13-1 lists the bias output voltages according to LCD reference voltages.

Table 13-1 Bias Output Voltages

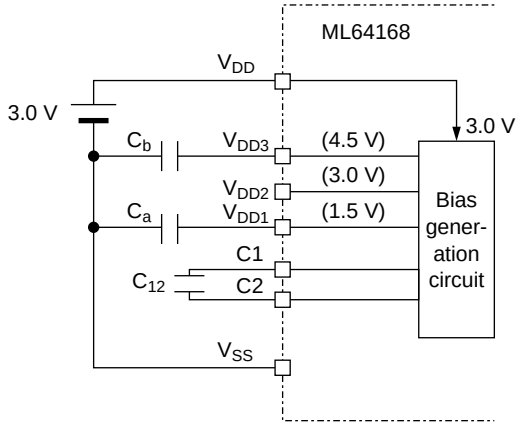
Power supply voltage (V_{DD})	1.5 V		3.0 V	
Mask option	Built-in regulator output	Power supply voltage	Built-in regulator output	Power supply voltage
LCD reference voltage	1.2 V	1.5 V	1.2 V	3.0 V
V_{DD3}	3.6 V	4.5 V	3.6 V	4.5 V
V_{DD2}	2.4 V	3.0 V	2.4 V	3.0 V (LCD reference voltage)
V_{DD1}	1.2 V (LCD reference voltage)	1.5 V (LCD reference voltage)	1.2 V (LCD reference voltage)	1.5 V



(a) When built-in regulator output is selected (common to the 1.5 V and 3.0 V power supply voltages)



(b) When power supply voltage (1.5 V) is selected (built-in regulator not used)



(c) When power supply voltage (3.0 V) is selected (built-in regulator not used)

Figure 13.5 Bias Generation Circuit Configuration (C_a, C_b, C_c, C_{12} = 0.1 μF)

Notes: Capacitors C_a, C_b, C_c, and C_{12} are not required unless the LCD driver is used. If the LCD driver is not used, leave the C1, C2, V_{DD1}, V_{DD2}, and V_{DD3} pins open.

When the LCD driver is used with 1/2 duty, a capacitor C_b is not required. Leave the V_{DD3} pin open then.

13.8 LCD Driver Output Waveforms

Figures 13-6 (a) to (c) show 1/4 duty of output waveforms of the LCD driver and Figures 13-7 (a) and (b) show 1/3 duty and Figures 13-8 (a) and (b) show 1/2 duty.

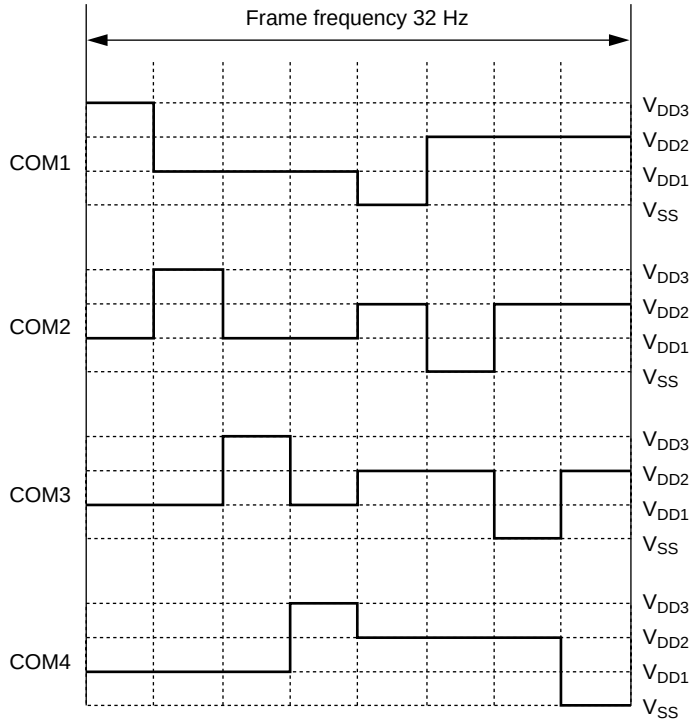


Figure 13-6 (a) 1/4 Duty Common Driving Waveforms (1/3 bias)

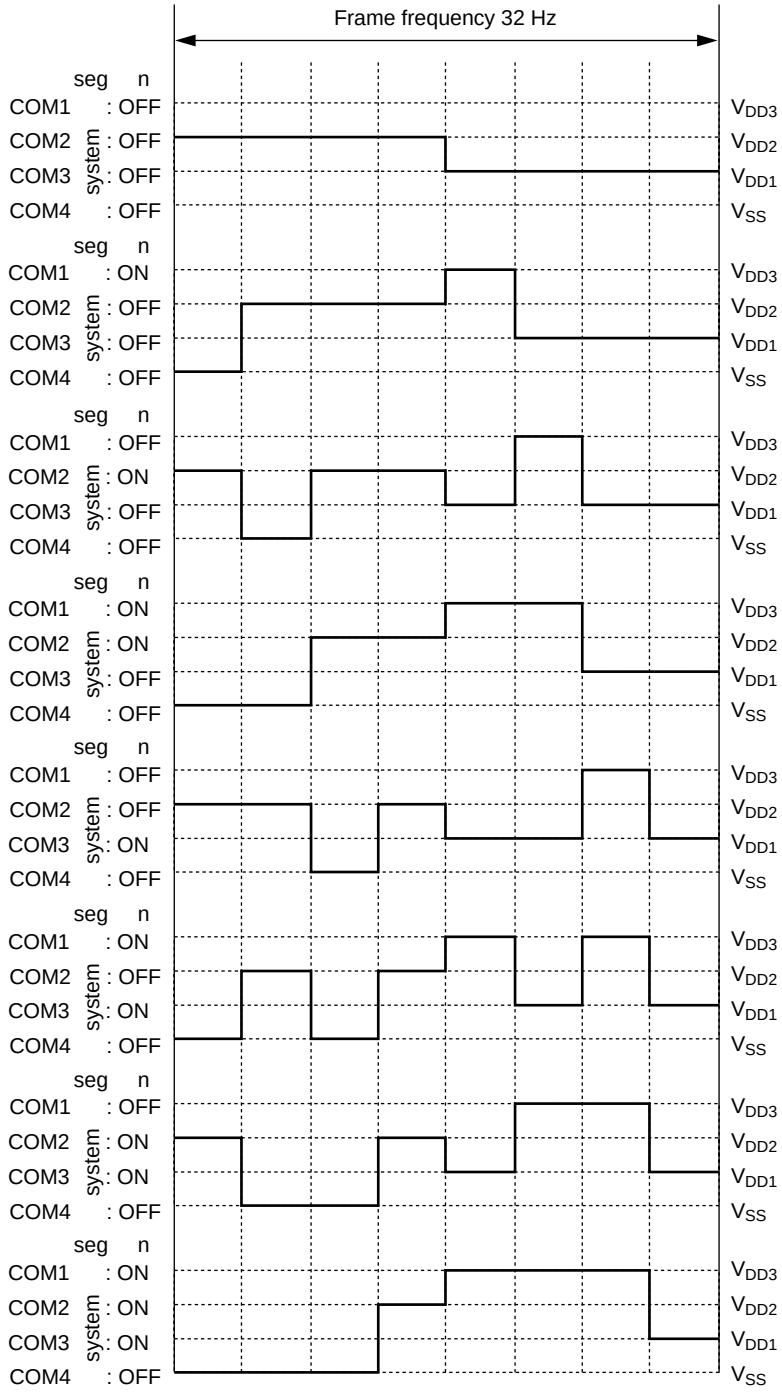


Figure 13-6 (b) 1/4 Duty Common Driving Waveforms (1/3 bias)

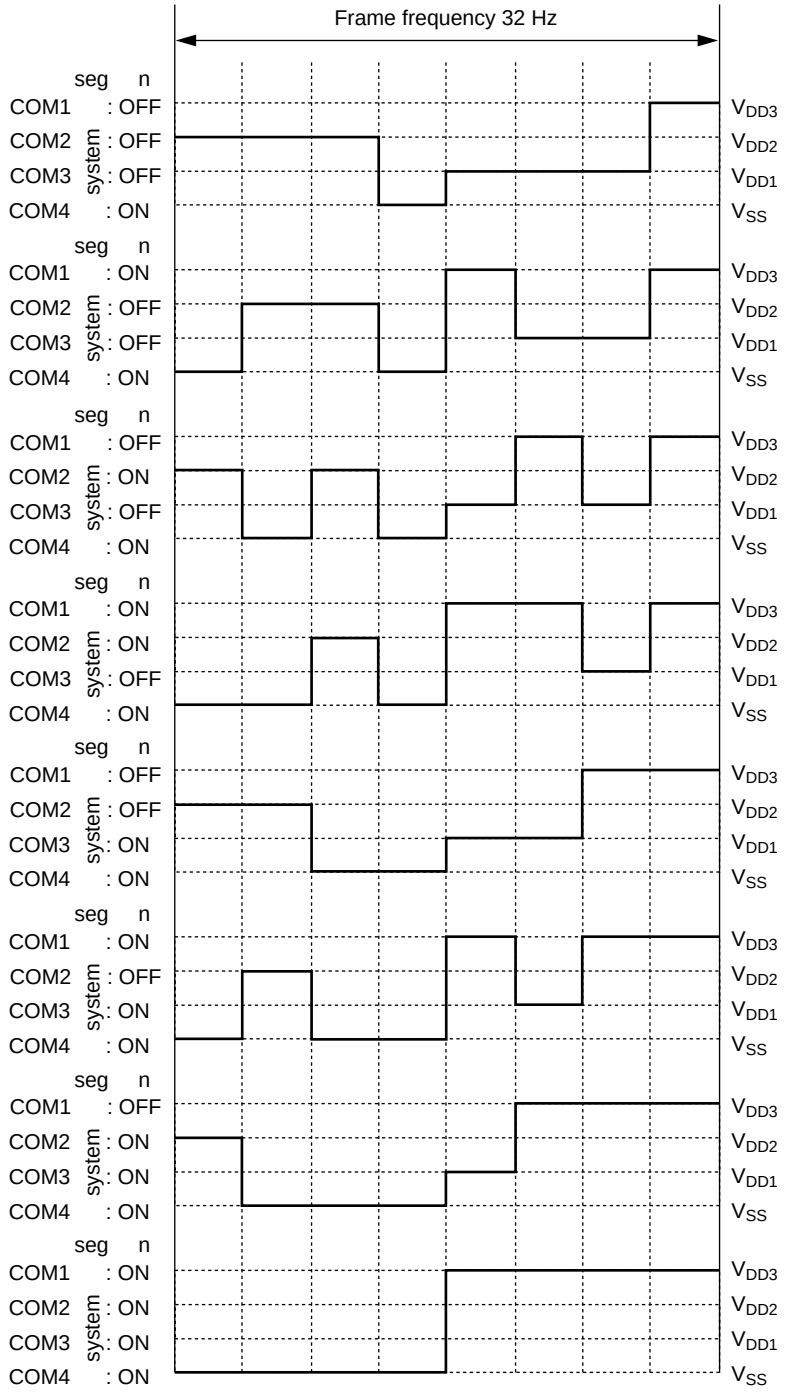


Figure 13-6 (c) 1/4 Duty Common Driving Waveforms (1/3 bias)

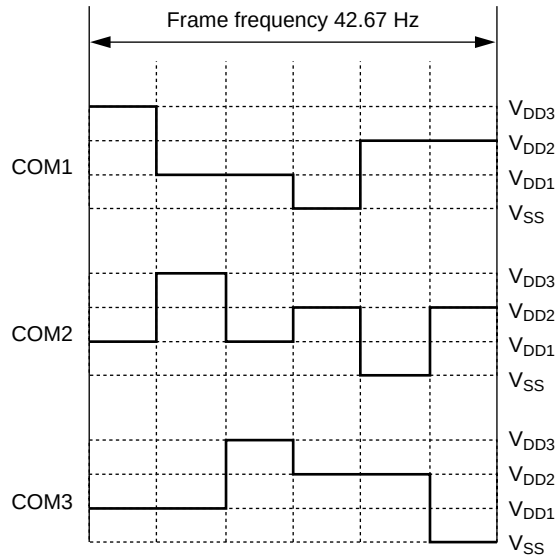


Figure 13-7 (a) 1/3 Duty Common Driving Waveforms (1/3 bias)

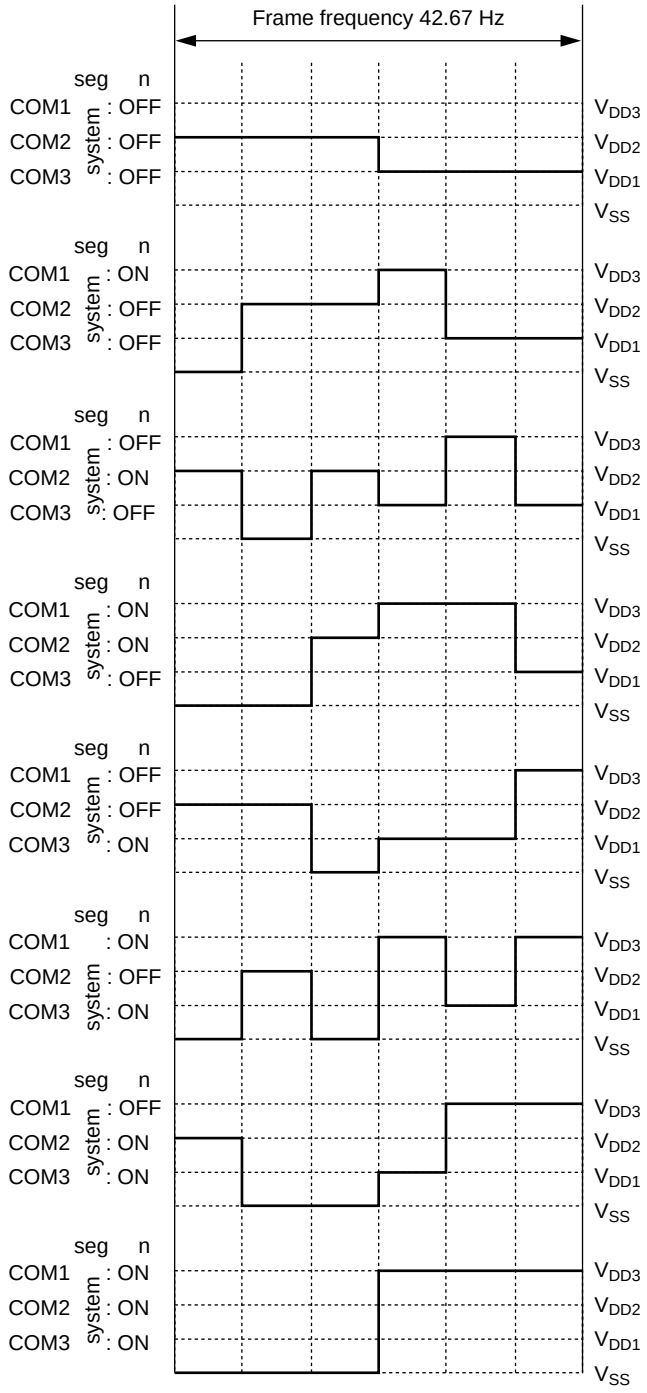


Figure 13-7 (b) 1/3 Duty Common Driving Waveforms (1/3 bias)

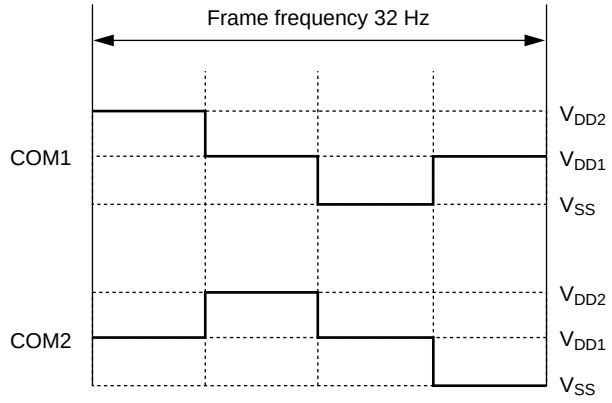


Figure 13-8 (a) 1/2 Duty Common Driving Waveforms (1/2 bias)

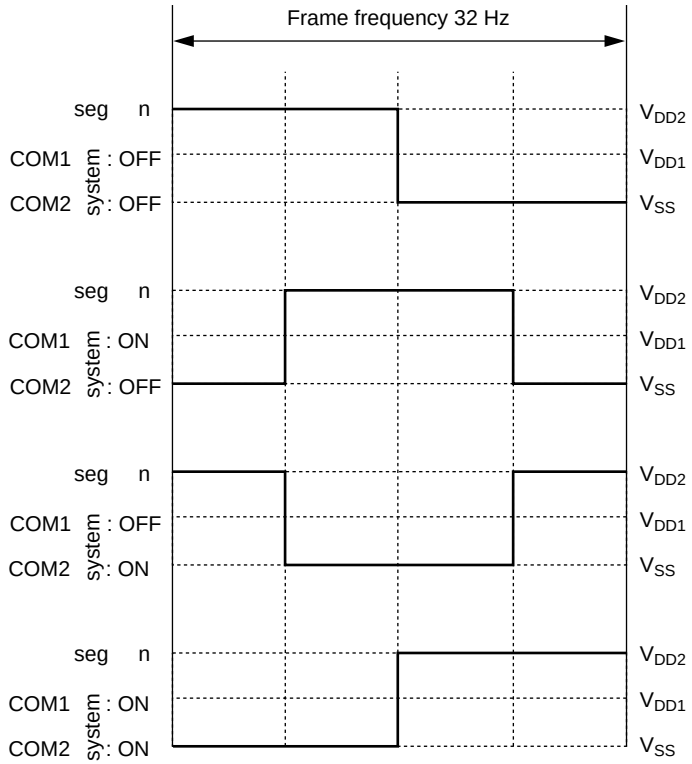


Figure 13-8 (b) 1/2 Duty Common Driving Waveforms (1/2 bias)

Tables 13-1 and 13-2 show the list of LCD driver-related registers and pins.

Table 13-1 (a) List of LCD Driver-Related Registers

Register name	Symbol	Address	Read/Write	Byte access	Value at system reset
Display control register	DSPCON	1EH	R/W	No	0CH
Display register 0	DSPR0	40H	R/W	Yes	0H
Display register 1	DSPR1	41H	R/W		0H
Display register 2	DSPR2	42H	R/W	Yes	0H
Display register 3	DSPR3	43H	R/W		0H
Display register 4	DSPR4	44H	R/W	Yes	0H
Display register 5	DSPR5	45H	R/W		0H
Display register 6	DSPR6	46H	R/W	Yes	0H
Display register 7	DSPR7	47H	R/W		0H
Display register 8	DSPR8	48H	R/W	Yes	0H
Display register 9	DSPR9	49H	R/W		0H
Display register 10	DSPR10	4AH	R/W	Yes	0H
Display register 11	DSPR11	4BH	R/W		0H
Display register 12	DSPR12	4CH	R/W	Yes	0H
Display register 13	DSPR13	4DH	R/W		0H
Display register 14	DSPR14	4EH	R/W	Yes	0H
Display register 15	DSPR15	4FH	R/W		0H
Display register 16	DSPR16	50H	R/W	Yes	0H
Display register 17	DSPR17	51H	R/W		0H
Display register 18	DSPR18	52H	R/W	Yes	0H
Display register 19	DSPR19	53H	R/W		0H
Display register 20	DSPR20	54H	R/W	Yes	0H
Display register 21	DSPR21	55H	R/W		0H
Display register 22	DSPR22	56H	R/W	Yes	0H
Display register 23	DSPR23	57H	R/W		0H
Display register 24	DSPR24	58H	R/W	Yes	0H
Display register 25	DSPR25	59H	R/W		0H

Table 13-1 (b) List of LCD Driver-Related Registers

Register name	Symbol	Address	Read/Write	Byte access	Value at system reset
Display register 26	DSPR26	5AH	R/W	Yes	0H
Display register 27	DSPR27	5BH	R/W		0H
Display register 28	DSPR28	5CH	R/W	Yes	0H
Display register 29	DSPR29	5DH	R/W		0H
Display register 30	DSPR30	5EH	R/W	No	0H

Note : The display registers 0 through 30 are registers that can not be used without selection by the mask option.
All the display registers to be used must be allocated on the LCD driver mask option table per bit. (Refer to Appendix F on the mask options.)

Table 13-2 (a) List of LCD Driver-Related Pins

Pin name	Pin No.		Pad No.	Input/Output	Function
	GP	GA, TB			
V_{DD1}	42	40	40	——	Bias output for driving LCD (1.2 V/1.5 V)
V_{DD2}	44	42	42	——	Bias output for driving LCD (2.4 V/3.0 V)
V_{DD3}	45	43	43	——	Bias output for driving LCD (3.6 V/4.5 V)
C1	46	44	44	——	Capacitor connection pin for LCD driving bias generation
C2	47	45	45	——	
L0	1	79	79	Output	LCD segment/common signal output pins
L1	2	80	80	Output	
L2	3	1	1	Output	
L3	4	2	2	Output	
L4	5	3	3	Output	
L5	6	4	4	Output	
L6	7	5	5	Output	
L7	8	6	6	Output	
L8	9	7	7	Output	
L9	10	8	8	Output	
L10	11	9	9	Output	
L11	12	10	10	Output	
L12	13	11	11	Output	
L13	14	12	12	Output	
L14	15	13	13	Output	
L15	16	14	14	Output	
L16	17	15	15	Output	
L17	48	46	46	Output	
L18	49	47	47	Output	
L19	50	48	48	Output	
L20	51	49	49	Output	
L21	52	50	50	Output	
L22	53	51	51	Output	
L23	54	52	52	Output	
L24	55	53	53	Output	
L25	56	54	54	Output	

Table 13-2 (b) List of LCD Driver-Related Pins

Pin name	Pin No.		Pad No.	Input/Output	Function
	GP	GA, TB			
L26/P5.0	57	55	55	Output	LCD driver output pins.
L27/P5.1	58	56	56	Output	Can become output ports by the mask option.
L28/P5.2	59	57	57	Output	
L29/P5.3	60	58	58	Output	
L30/P6.0	61	59	59	Output	
L31/P6.1	62	60	60	Output	
L32/P6.2	63	61	61	Output	
L33/P6.3	64	62	62	Output	

Chapter 14

Constant Voltage Circuit for Logic Power Supply (VR)

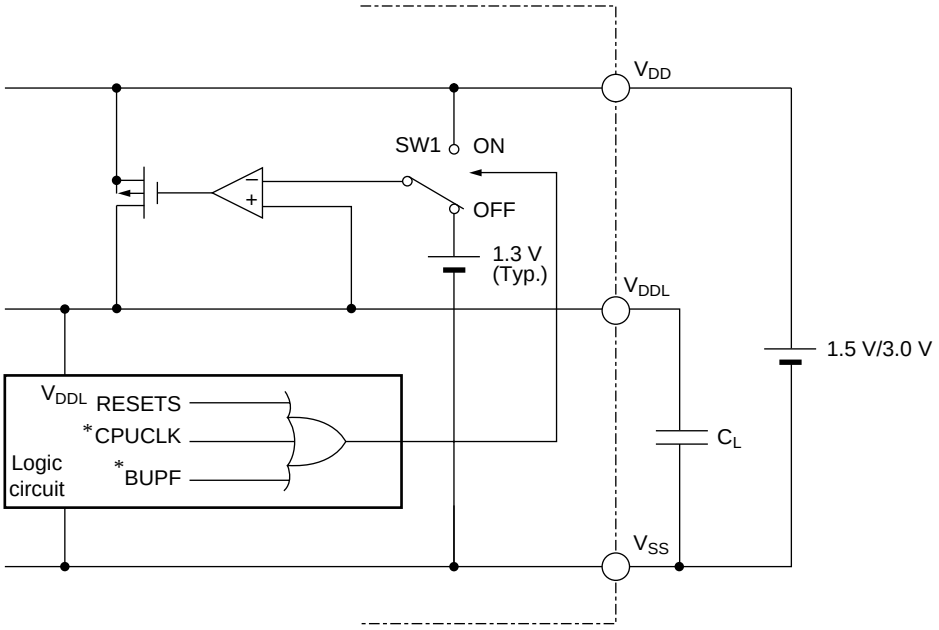
Chapter 14 Constant Voltage Circuit for Logic Power Supply (VR)

14.1 Overview

The ML64168 has a built-in constant voltage circuit for the logic power supply (VR).

14.2 Layout of Constant Voltage Circuit for Logic Power Supply

Figure 14-1 shows the layout of the constant voltage circuit for the logic power supply.



* BUPF indicates output of the backup flag.
CPUCLK indicates output of the system clock selection bit.

Figure 14-1 Constant Voltage Circuit for Logic Power Supply

In Figure 14-1, the "C_L" capacitor is a noise smoothening condenser on the V_{DDL} line of the logic circuit and it is necessary to install the capacitor of 0.05 µF to 0.2 µF for C_L. SW1 in the Figure becomes ON state when (1) the system clock selection bit (CPUCLK) is set to "1", (2) in system reset mode or (3) the backup flag (BUPF) is set to "1".

When developing an application in which CPUCLK or BUPF is set to "1" in the 3.0 V specifications, install the capacitor of 0.47 µF ±30% for C_L. In other cases, install the capacitor of 0.05 µF to 0.2 µF for C_L.

14.3 Operation of Constant Voltage Circuit for Logic Power Supply

The constant voltage for the logic power supply (VR) outputs a constant voltage of 1.3 V (Typ.) to the V_{DDL} pin and supplies V_{DDL} level as the power supply of the logic circuit.

At system reset or when selecting 700 kHz RC oscillation output as the system clock, the V_{DDL} output is forced to be switched to V_{DD}.

In normal operation mode, the V_{DDL} output is switched to V_{DD} when Bit 0 (BUPF) of the backup control register (BUPCON) is set to "1" while the crystal oscillation output is the system clock. When resetting BUPF to "0", the V_{DDL} output becomes approximately 1.3 V.

In system reset mode, BUPF is reset to "0" but as shown in Figure 14-2, the V_{DDL} output becomes either V_{DD} level for 0.5 second after crystal oscillation started.

Table 14-1 shows output state of V_{DDL} by the CPUCLK bit, BUPF flag and system reset mode and Figure 14-2 shows output status of V_{DDL} in system reset mode.

Table 14-1 Output State of V_{SSL}

System reset mode	CPUCLK flag	BUPF flag	V_{DDL} output level
0.5 sec duration	——	——	V_{DD}
——	0	0	about 1.3 V
——	0	1	V_{DD}
——	1	——	V_{DD}

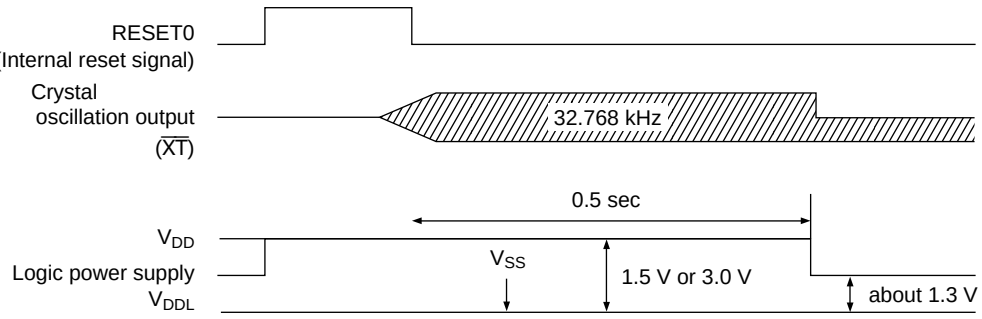


Figure 14-2 V_{SSL} Output State in System Reset Mode

14.4 Backup Control Register (BUPCON)

The backup control register (BUPCON) is a 4-bit special function register (SFR) to control the output voltage level of V_{DDL} which is output of the constant voltage circuit for logic.

BUPCON (37H) (R/W)

b_3	b_2	b_1	b_0
-----*	CMPF	ECMP	BUPF

Battery check flag
- 0: Input voltage level of P0.3 is higher than reference voltage (initial value)
- 1: Input voltage level of P0.3 is lower than reference voltage

Battery check enable
- 0: Battery check disabled (initial value)
- 1: Battery check abled

V_{DDL} level
- 0: 1.3 V level (initial value)
- 1: V_{DD} level

*Reserved bit: "1" is always read. Not valid for write.

Bit 0: BUPF

This bit is a flag to select output voltage level of V_{DDL} which is output of the constant voltage circuit for logic (VR). By resetting BUPF to "0", the V_{DDL} output becomes 1.3 V and by setting BUPF to "1", the V_{DDL} output becomes V_{DD} level. At system reset, it is reset to "0". For 0.5 second after the system reset, the V_{DDL} output is forced to be switched to V_{DD} level.

Table 14-2 shows those pins related to the constant voltage circuit for logic.

Table 14-2 Pins Related to Constant Voltage Circuit for Logic

Pin name	Pin No.		Pad No.	Input/Output	Note
	GP	GA, TB			
V_{DD}	67	65	65	——	Positive side power supply pin
V_{DDL}	31	29	29	——	Positive side power supply pin for internal logic (internally generated voltage)

Chapter 15

Test Circuit (TST)

Chapter 15 Test Circuit (TST)

15.1 Overview

The ML64168 can output RC oscillation clock of the A/D converter or 700 kHz RC oscillation clock of the system clock to Port 4.3 using $\overline{TST1}$ and $\overline{TST2}$, which are test pins.

By monitoring each RC oscillation clock, it is possible to measure the conversion characteristics of the A/D converter and the frequency of the RC oscillation side system clock.

15.2 Operation of Test Circuit

When releasing system reset mode by inputting "H" to the $\overline{RESET}$ pin after selecting system reset mode by inputting "L" to the $\overline{RESET}$ pin while both $\overline{TST1}$ and $\overline{TST2}$ are in "L" level, the test mode is selected.

To return from test mode to normal mode, both $\overline{TST1}$ and $\overline{TST2}$ must be left open or in a state where "H" level is input and the system reset must be input after that. When both $\overline{TST1}$ and $\overline{TST2}$ are open, test mode is released. However, normal operation mode is not restored until the system reset is input.

Figure 15-1 shows the relation among the $\overline{TST1}$, $\overline{TST2}$ pins and the $\overline{RESET}$ pin.

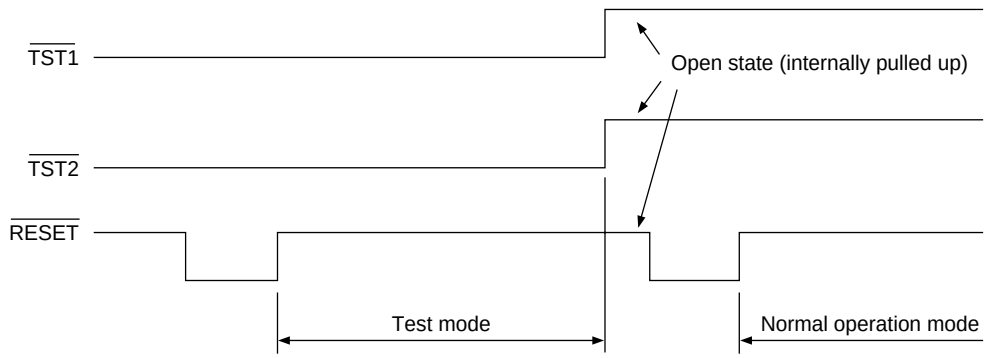


Figure 15-1 Relation among the $\overline{TST1}$, $\overline{TST2}$ pins and the $\overline{RESET}$ pin

Depending the state of Ports 0.0 to 0.3, various RC oscillation signals are output to Port 4.3 after moving to test mode.

Tables 15-1 and 15-2 show the list of test modes and test circuit related pins. Figure 15-2 shows an example of connection in test mode.

Notes:

Please note that there is no guarantee of normal operation if both $\overline{TST1}$ and $\overline{TST2}$ are not simultaneously open or at "H" level or "L" level.

Table 15-1 List of Test Modes

$\overline{TST1}$	$\overline{TST2}$	P0.3	P0.2	P0.1	P0.0	P4.3 output mode	
0	0	1	0	0	0	CROSC0 oscillation stop (P4.3 = IN0 input)	CROSC0 oscillation mode
0	0	1	0	0	1	RS0-CS0 oscillation clock	
0	0	1	0	1	0	RT0-CS0 oscillation clock	
0	0	1	0	1	1	RT0-1-CS0 oscillation clock	
0	0	1	1	0	0	CT0-1-RS0 oscillation clock	
0	0	1	1	0	1	RS1-CS1 oscillation clock	CROSC1 oscillation mode
0	0	1	1	1	0	RT1-CS1 oscillation clock	
0	0	1	1	1	1	CROSC1 oscillation stop (P4.3 = IN1 input)	
0	0	0	—	—	—	700 kHz RC oscillation clock output	

Notes: 0: "L" level input
1: "H" level input
—: Arbitrary

Table 15-2 Test Circuit-Related Pins

Pin name	Pin No.		Pad No.	Input/Output	Notes
	GP	GA, TB			
$\overline{TST1}$	71	69	69	Input	Test input
$\overline{TST2}$	72	70	70	Input	Test input
$\overline{RESET}$	70	68	68	Input	Reset input
P0.0	77	75	75	Input	Test mode selection
P0.1	78	76	76	Input	Test mode selection
P0.2	79	77	77	Input	Test mode selection
P0.3	80	78	78	Input	Test mode selection
P4.3	29	27	27	Output	RC oscillation clock monitor output

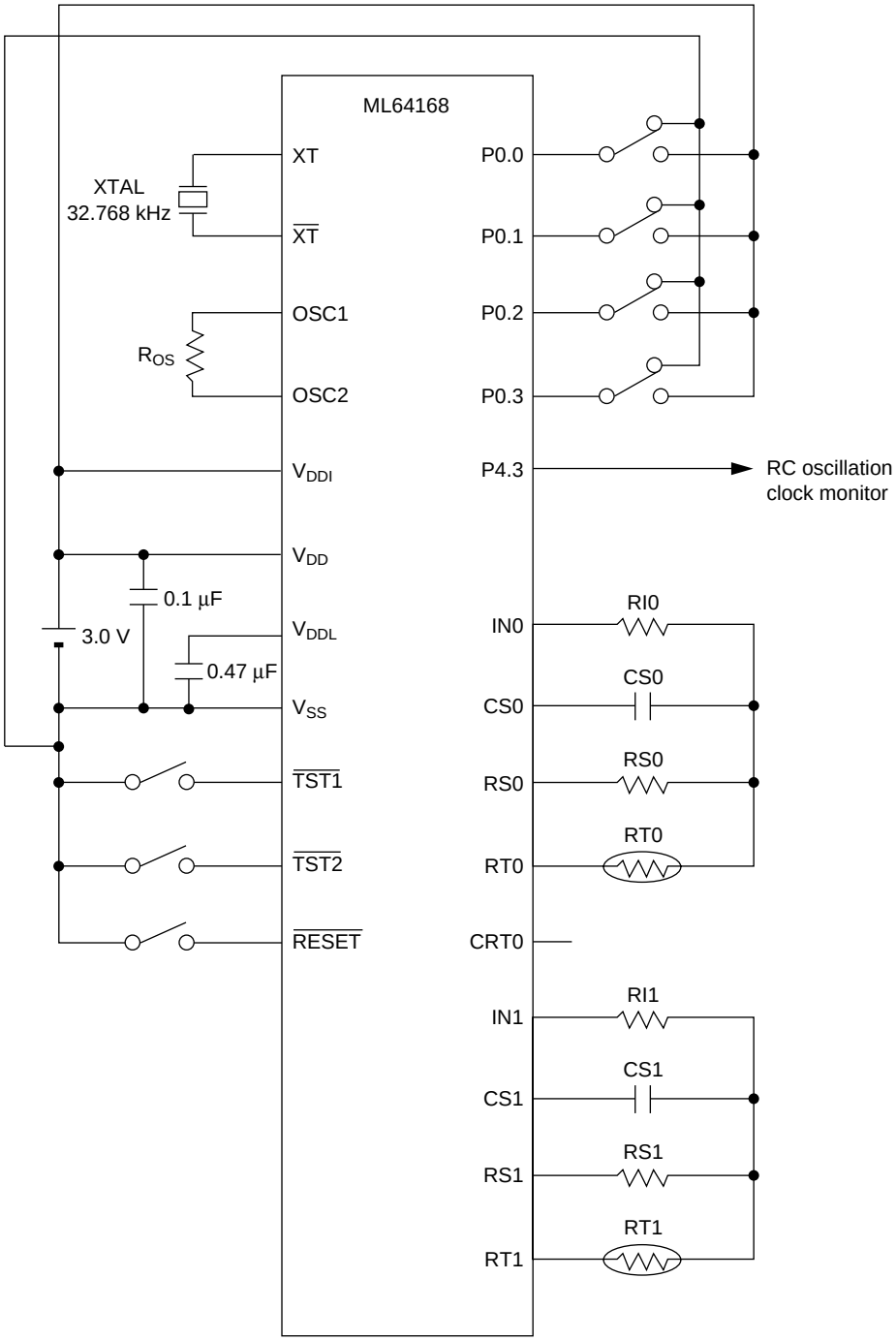


Figure 15-2 Connection Example of Test Mode (3.0 V operation mode)

Chapter 16

Battery Check Circuit (BC)

Chapter 16 Battery Check Circuit (BC)

16.1 Overview

The battery check circuit applies current to the external IC load equalizing resistor (R_{BLD}) and detects the level down of current voltage by comparing the voltage with the internal reference voltage (Vrb).

16.2 Layout of Battery Check Circuit

The battery check circuit is composed of a comparator and reference voltage generation circuit. The comparator input is assigned P0.3 port (also used as input port).

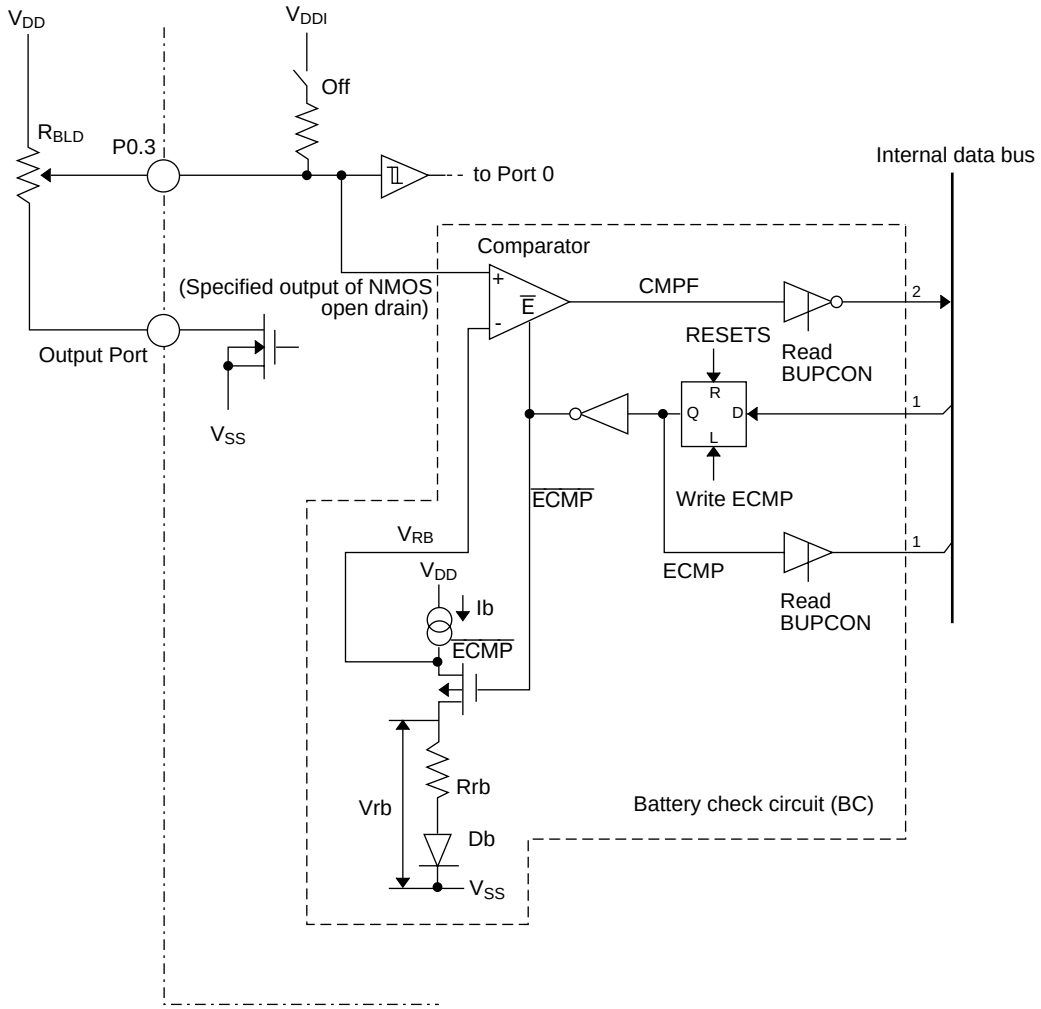


Figure 16-1 Layout of Battery Check Circuit

Figure 16-1 shows the layout of the battery check circuit.

Since the P0.3 is also used as the input port as shown in Figure 16-1, cut off the pull-up or pull-down resistor for the battery check. By controlling ON/OFF of the external resistor (R_{BLD}) with the NMOS open drain of output port, a simple battery check circuit is available. The reference voltage Vrb is approx. 0.6 V.

16.3 Operation of Battery Check Circuit

The battery check circuit is controlled and checked by the ECMP and CMPF assigned to the Back-up control register BUPCON (refer to chapter 14).

The ECMP is an enable bit of comparator. When ECMP is set to "1", the reference voltage is generated and comparator is started and when it is set to "0", the comparator is halted.

The CMPF is an output of comparator. When CMPF is "1", the input voltage level is lower than the reference voltage level, and when it is "0", the input voltage is higher than the reference voltage. The value of CMPF is not valid when the ECMP is "0".

Figure 16-2 shows operation timing of the battery check operation.

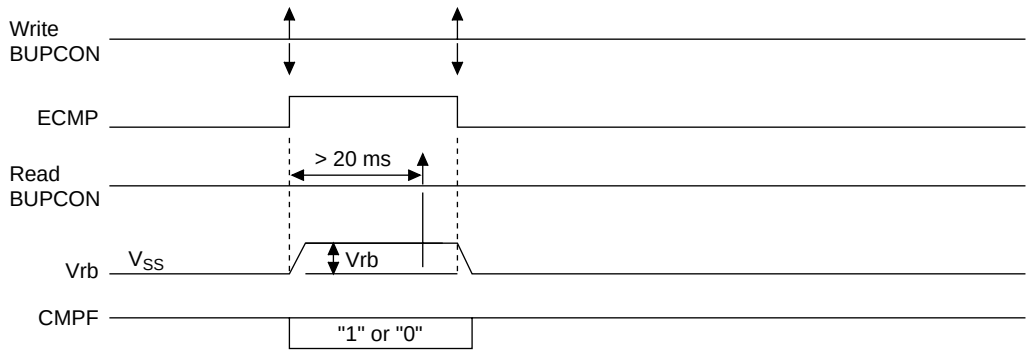


Figure 16-2 Battery Check Timing

16.4 Registers Related to Battery Check Circuit

The battery check circuit is controlled by the ECMP and CMPF assigned to the Back-up control register (BUPCON).

BUPCON (37H) (R/W)

b_3	b_2	b_1	b_0
-----*	CMPF	ECMP	BUPF

Battery check flag

0: Input voltage level of P0.3 is higher than reference voltage (initial value)
1: Input voltage level of P0.3 is lower than reference voltage (battery low being detected)

Battery check enable

0: Battery check disabled (initial value)
1: Battery check enabled

V_{DDL} level

0: 1.3 V level (initial value)
1: V_{DD} level

* Reserved bit: "1" is always read out. Not valid for write.

For details of BUPF at bit 0, refer to Chapter 14 "Constant Voltage Circuit for Logic Power Supply (VR)".

Chapter 17

ML64P168 (OTP Version)

Chapter 17 ML64P168 (OTP Version)

17.1 Overview

The ML64P168 is a program memory (ROM) chip built into the ML64168(mask ROM chip) which is converted to a one time PROM (OTP) chip.

In addition, this chip that differs from the mask ROM chip has no supply.

For these reasons, this OTP version of the ML64P168 should be used mainly for verification of application program functions.

The ML64P168 has two operating modes of a microcontroller operating mode and PROM mode. The microcontroller operating mode is a mode to make the same operation as a mask ROM chip and the PROM mode is a mode to write/read PROM.

This chapter explains different specifications from the mask ROM chip.

17.2 Features

Following shows the features of the ML64P168 that are different from the ML64168.

1) Built-In Program Memory: 8160 bytes (PROM)
2) LCD Driver: 34 drivers
   - 1/4 duty, during 1/3 bias: 120 segments (30 × 4)
   - 1/3 duty, during 1/3 bias: 93 segments (31 × 3)
   - 1/2 duty, during 1/2 bias: 64 segments (32 × 2)
   - Output ports selectable by mask options on 8 drivers
   - Externally supplied (from power supply voltage)/internally supplied (from built-in ragulator) reference voltage selectable by mask option
   - Preparation for several kinds of standard mask option products
3) External Appearance
   - 80-pin flat package (QFP) only

   * Other features are the same as the ML64168.

17.3 Block Diagram

Figure 17-1 shows the block diagram of the ML64P168.

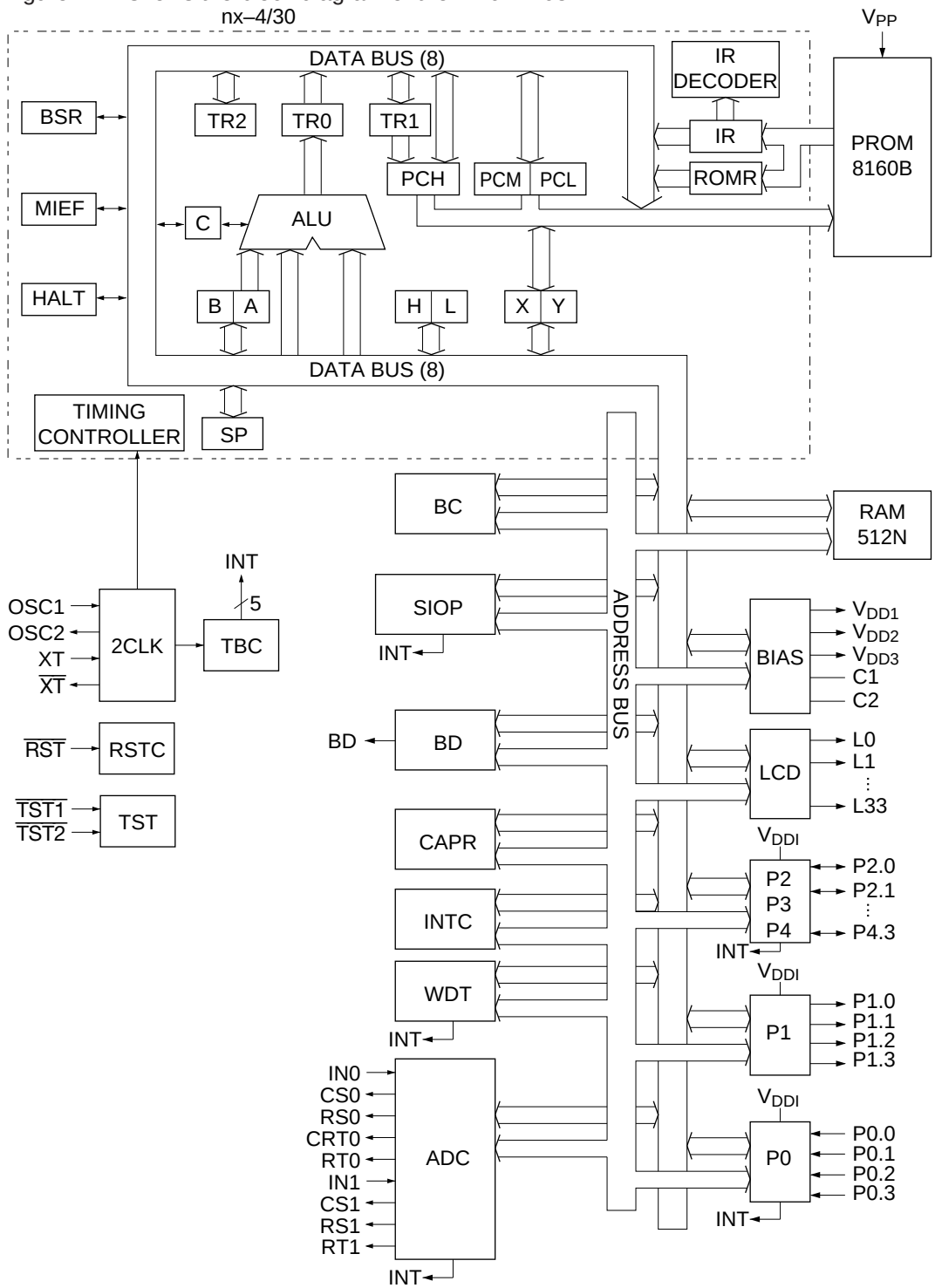


Figure 17-1 ML64P168 Block Diagram

17.4 Pin Configuration

Figures 17-2 and 17-3 show the layout of package pins of the ML64P168.

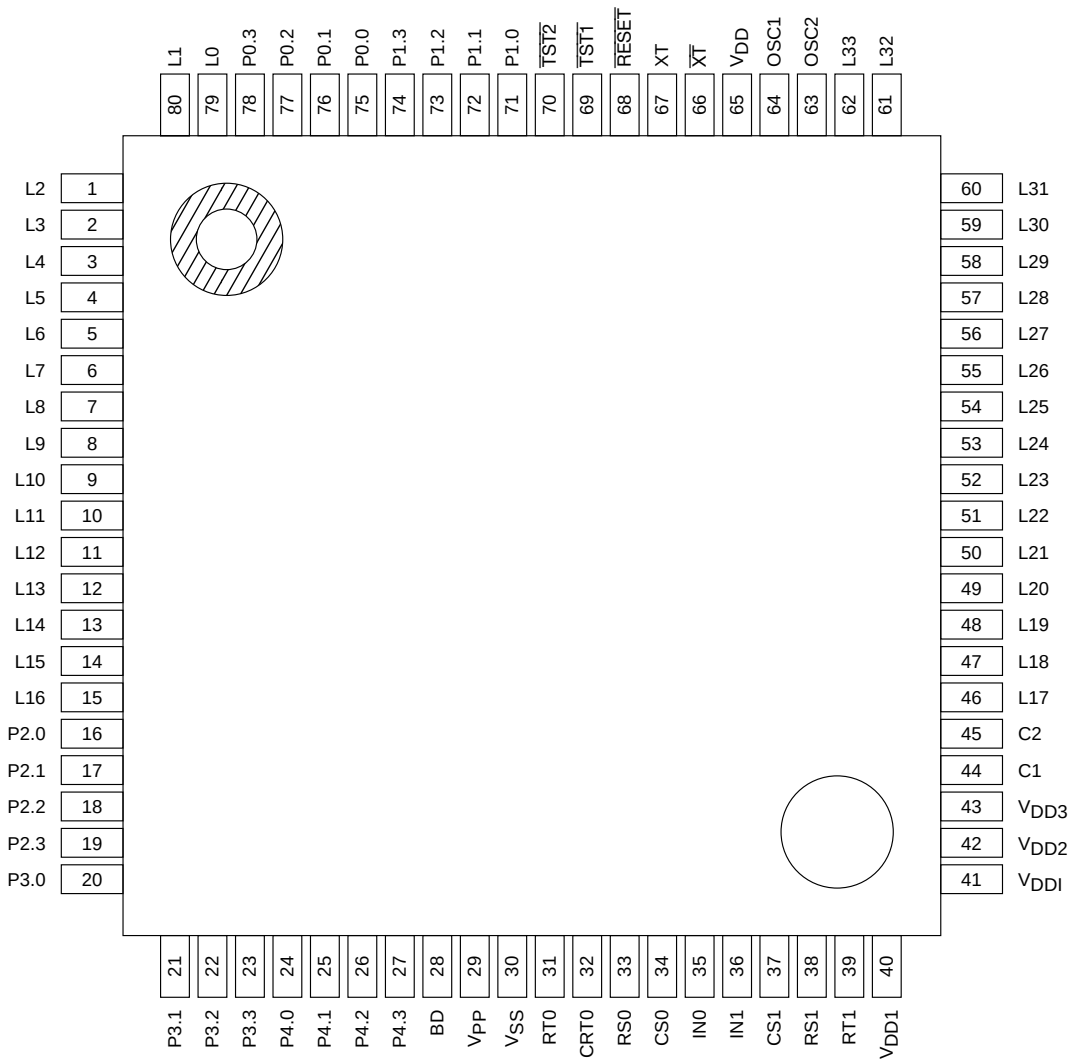


Figure 17-2 ML64P168 (GA) Pin Configuration

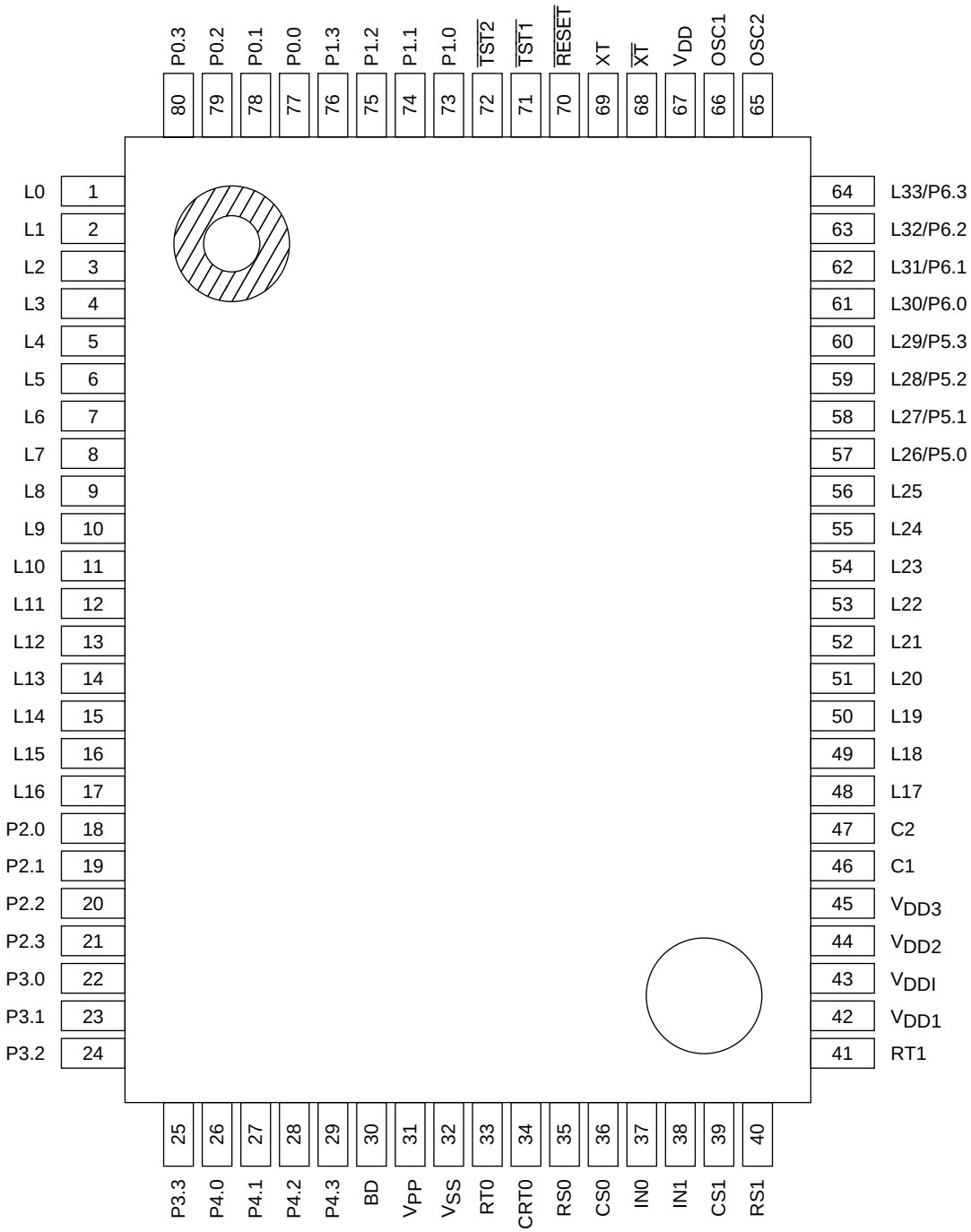


Figure 17-3 ML64P168 (GP) Pin Configuration

17.5 Pin Description

17.5.1 Changes in the OTP Version

Table 17-1 lists the pin changes that have been made in the OTP version.

Table 17-1 Pin Changes in the OTP Version

Classification	Pin name	Pin No.		Input/Output	Function
		GP	GA		
Power supply	V_{PP}	31	29	—	Positive power supply for writing to PROM (+12.5 V)
	V_{DDI}	43	41	—	Positive power supply for I/O port interface. When 1.5 V power supply is used, a voltage of 2.7 V or more needs to be supplied to this pin. (Power supply for PROM)

Note: The OTP version (ML64P168) has the V_{PP} pin (positive power supply for writing to PROM : +12.5 V) instead of the V_{DDL} pin.

When using a 1.5 V power supply, be sure to apply a voltage of 2.7 V or more to the V_{DDI} pin. (Not required when using a 3.0 V power supply.)

17.5.2 PROM Related Pins

Table 17-2 shows pins used to write program data to the ML64P168.

Table 17-2 Explanation of Pins (PROM Functions)

Classification	Pin name	Pin No.		Input/ Output	Function
		GP	GA		
LCD Driver	V_{SS}	32	30	—	0 V power supply
	V_{DD}*	67	65	—	Positive power supply pin (+5 V supplied)
	V_{DDI}*	43	41	—	Positive power supply pin (+5 V supplied)
	V_{PP}	31	29	—	PROM write power supply (+12.5 V supplied)
	$\overline{RESET}$	70	68	Input	PROM write setting pin PROM mode is set by "L" level input
	$\overline{TST1}$	71	69	Input	
	$\overline{TST2}$	72	70	Input	
	D0 (L0)	1	79	I/O	Pin for writing and reading of program data
	D1 (L1)	2	80	I/O	
	D2 (L2)	3	1	I/O	
	D3 (L3)	4	2	I/O	
	D4 (L4)	5	3	I/O	
	D5 (L5)	6	4	I/O	
	D6 (L6)	7	5	I/O	
	D7 (L7)	8	6	I/O	
	$\overline{CE}$ (L8)	9	7	I/O	PROM chip enable pin
	$\overline{OE}$ (L9)	10	8	I/O	PROM output enable signal
	A0 (L10)	11	9	Input	Program address input pin
	A1 (L11)	12	10	Input	
	A2 (L12)	13	11	Input	
	A3 (L13)	14	12	Input	
	A4 (L14)	15	13	Input	
	A5 (L15)	16	14	Input	
	A6 (L16)	17	15	Input	
	A7 (L17)	48	46	Input	
	A8 (L18)	49	47	Input	
	A9 (L19)	50	48	Input	
	A10 (L20)	51	49	Input	
	A11 (L21)	52	50	Input	
	A12 (L22)	53	51	Input	
	L23	54	52	Input	Input "H" level

* PROM mode should be supplied with 5 V both to V_{DD} and V_{DDI}.

17.6 Logic Power Supply

The ML64P168 is not equipped with the Constant Voltage Circuit for Logic Power Supply (VR). The ML64P168 logic circuit is therefore driven by the power supply voltage.

For this reason, the LSB (b0) of the backup control register (BUPCON) is disabled in the ML64P168.

BUPCON (37H) (R/W)

b_3	b_2	b_1	b_0
-----*	CMPF	ECMP	-----*

Battery check flag

0: Input voltage level of P0.3 is higher than reference voltage (initial value)
1: Input voltage level of P0.3 is lower than reference voltage (battery low being detected)

Battery check enable

0: Battery check disabled (initial value)
1: Battery check enabled

*Reserved bit: Always reads "1". Write is disabled.

17.7 Power Supply Circuit Configuration for IC

Figures 17-4 and 17-5 show the circuit configuration of the power supply for IC including the differences between the ML64P168 and the mask ROM chip ML64168.

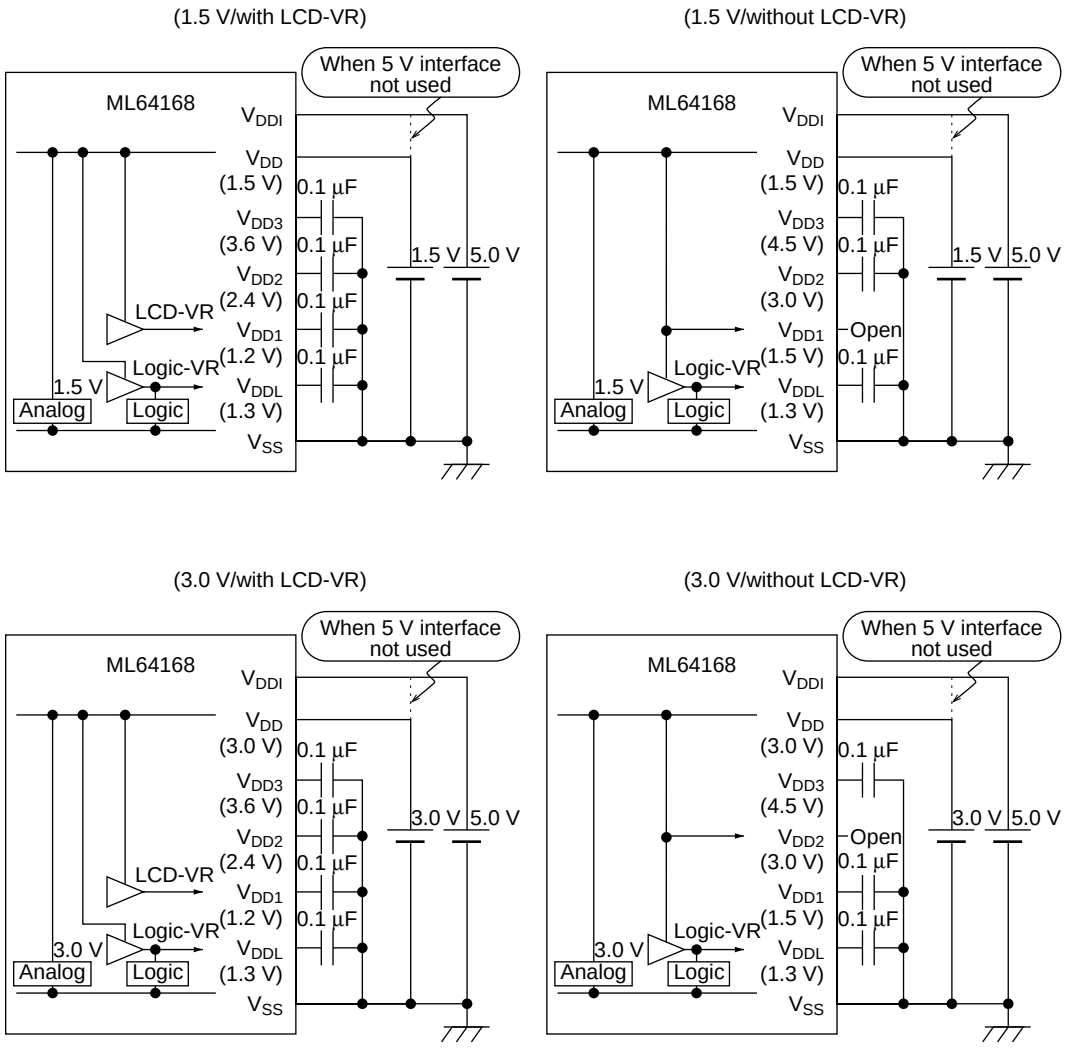


Figure 17-4 Configuration of Power Supply System (Mask ROM Version)

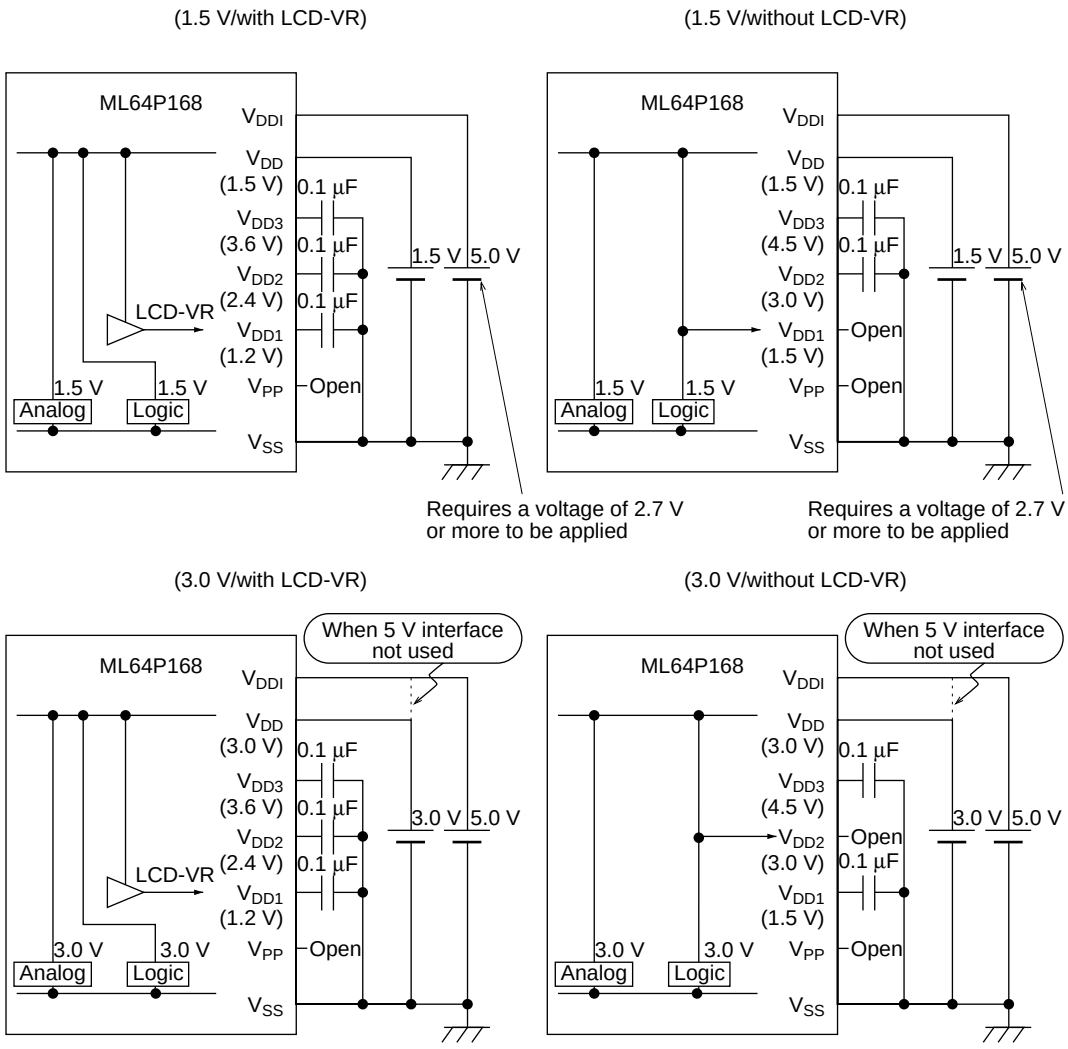


Figure 17-5 Configuration of Power Supply System (OTP Version)

17.8 PROM

The ML64P168 uses built-in PROM as program memory. The capacity of this PROM is 8160 bytes, and the capacity that omitted 32 bytes from the 1FE0H address to the 1FFFH address, forming the test data area of the mask ROM chip.

In order to write the program data to this PROM, the ML64P168 uses a special adapter (OTP 64168 BOARD) which is connected to the general EPROM writer for writing. See also the manual of this special adapter for further reference.

17.8.1 Explanation of Pins

Table 17-3 shows PROM related pins of the ML64P168.

Table 17-3 (a) List of PROM Related Pins

Pin name	Pin No.		Input/ Output	Remarks
	GP	GA		
V_{SS}	32	30	—	0 V power supply
V_{DD}	67	65	—	Positive power supply pin (+5 V supplied)
V_{DDI}	43	41	—	Positive power supply pin (+5 V supplied)
V_{PP}	31	29	—	Power supply for PROM writing (+12.5 V supplied)
$\overline{RESET}$	70	68	Input	PROM mode setting pin PROM mode is activated when the "L" level is input for 3 common pins
$\overline{TST1}$	71	69	Input	
$\overline{TST2}$	72	70	Input	

Table 17-3 (b) List of PROM Related Pins

Pin name	Pin No.		Input/ Output	Function
	GP	GA		
D0 (L0)	1	79	I/O	Program data write and read pins
D1 (L1)	2	80	I/O	
D2 (L2)	3	1	I/O	
D3 (L3)	4	2	I/O	
D4 (L4)	5	3	I/O	
D5 (L5)	6	4	I/O	
D6 (L6)	7	5	I/O	
D7 (L7)	8	6	I/O	
$\overline{CE}$ (L8)	9	7	Input	PROM chip enable pin
$\overline{OE}$ (L9)	10	8	Input	PROM output enable signal
A0 (L10)	11	9	Input	Program address input pins
A1 (L11)	12	10	Input	
A2 (L12)	13	11	Input	
A3 (L13)	14	12	Input	
A4 (L14)	15	13	Input	
A5 (L15)	16	14	Input	
A6 (L16)	17	15	Input	
A7 (L17)	48	46	Input	
A8 (L18)	49	47	Input	
A9 (L19)	50	48	Input	
A10 (L20)	51	49	Input	
A11 (L21)	52	50	Input	
A12 (L22)	53	51	Input	
L23	54	52	Input	Input "H" level

17.8.2 PROM Mode

The ML64P168 is capable of two separate modes, a PROM mode, which is used to write to PROM and read from PROM, and a computer operating mode, which is used to execute programs written to PROM. When ML64P168 is in the PROM mode, it simply operates as PROM. These operations are explained under PROM mode.

17.8.3 Setting the PROM Mode

Setting of the PROM mode is done with $\overline{\text{RESET}}$, $\overline{\text{TST1}}$, and $\overline{\text{TST2}}$, listed in Table 17-4. When the PROM mode is set, LCD pins become PROM related pins.

Table 17-4 PROM Mode Setting

$\overline{\text{RESET}}$	$\overline{\text{TST1}}$	$\overline{\text{TST2}}$	Mode
L	L	L	PROM Mode

17.8.4 PROM Mode Functions

PROM Mode functions are shown in Table 17-5.

Table 17-5 List of PROM Mode Functions

Mode	$\overline{\text{CE}}$ (L8)	$\overline{\text{OE}}$ (L9)	V_{PP}	V_{DD} V_{DDI}	D7 to D0 (L7 to L0)
Read	L	L	5 V	5 V	Program data output
Program	L	H	12.5 V	5 V	Program data input
Program verify	L	L	12.5 V	5 V	Program data output

17.8.5 Connection to the EPROM Writer

Figure 17-6 shows how to connect the EPROM writer to the ML64P168.

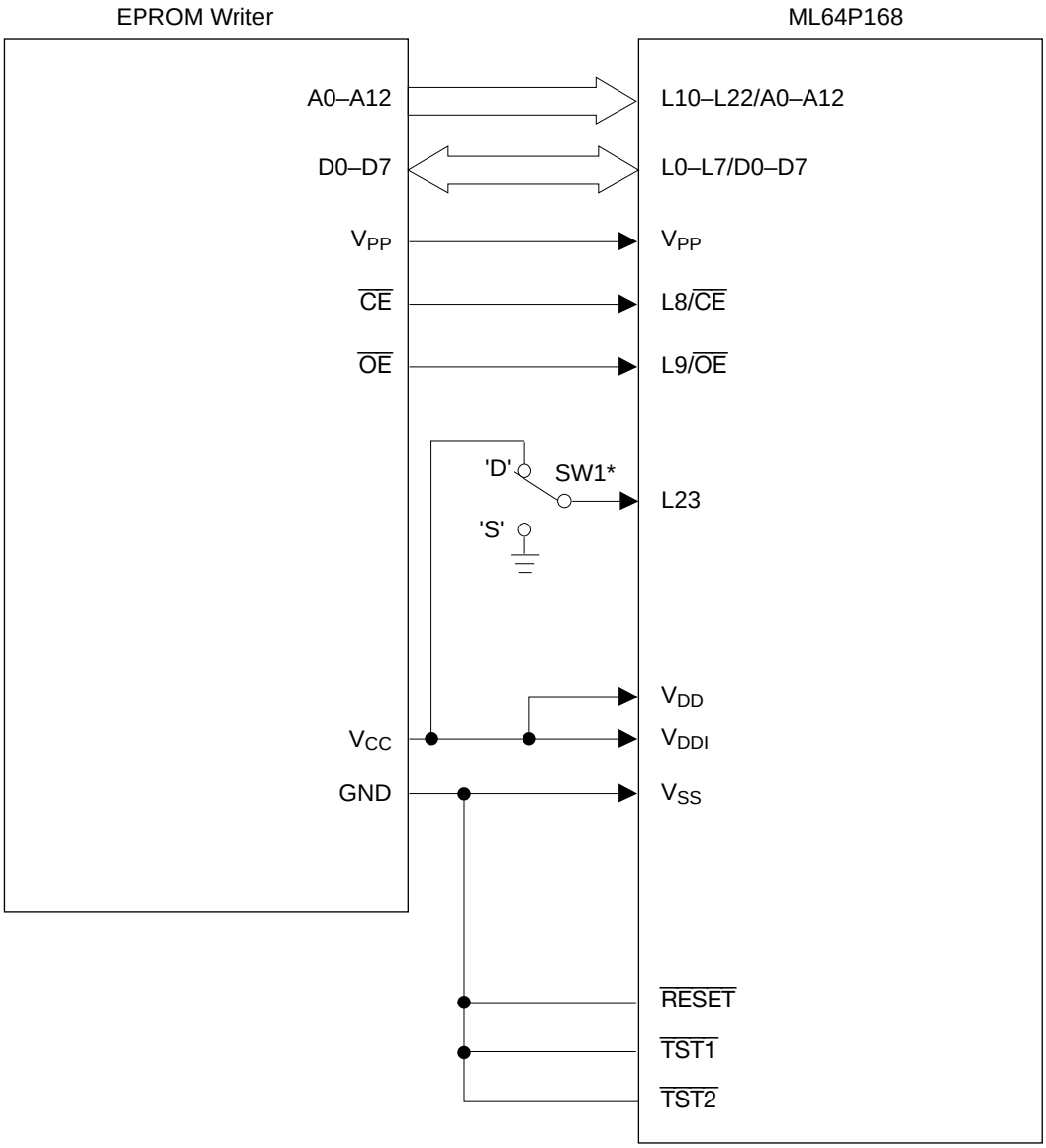


Figure 17-6 Connection to the EPROM Writer

* : In SW1, 'D' is a normally closed contact.

Chapter 18

Instruction Set

Chapter 18 Instruction Set

18.1 Overview

All instructions are configured in byte (8-bit) units. By instruction word length, instructions are classified into three types: 1-byte length, 2-byte length, and 3-byte length.

There are 148 types of instructions, however if HL indirect addressing and XY indirect addressing instruction pairs in data memory addressing mode are regarded as 1 type, then there are 121 types of basic instructions.

These 148 types of instructions are classified by instruction word length as follows:

- 1-byte instruction 81types
- 2-byte instruction ..... 64types (of these, 26 types are XY indirect addressing instructions)
- 3-byte instruction ..... 3 types (of these, 1 type is an XY indirect addressing instruction)

Total 148 types

Instruction features are explained below. In this document, "Data Memory" refers to RAM and various special function registers (SFRs) laid out in data memory space.

(1) Instructions frequently used are allocated to a 1-byte instruction.

(2) The HL and XY register pairs allow two indirect addressing modes to be used for data memory.

(3) Byte transfer, byte addition/subtraction, and byte comparison are possible for the entire data memory area. However, a byte instruction cannot be used for some of the SFRs.

(4) Bit operation is possible for the entire data memory area.

(5) A conditional branch is performed by a skip and jump instruction combination.

(6) The ROM table reference instruction (LMTB a_4) allows a data table to be created in program memory (ROM).

(7) The vertical stack instructions (LAI n_4, LLI n_4) allow efficient programming such as multientry of subroutines.

Because of the above features, instruction sets are easy to program and very efficient to use.

Since all SFRs are laid out in the data memory address space, SFRs can be operated and referred to just like data memory. Some SFRs, however, have limited functions, such as write only, or read only.

The instruction execution time is from 1 to 5 machine cycles (3 times the CPU clock cycle is one machine cycle.)

By machine cycle, instructions are classified as follows:

- 1 machine cycle ..... 55 types
- 2 machine cycles .... 75 types (of these, 18 types are XY indirect addressing instructions)
- 3 machine cycles .... 13 types (of these, 9 types are XY indirect addressing instructions)
- 4 machine cycles .... 2 types
- 5 machine cycles .... 3 types

By function, instructions are classified as follows:

(1) 4-Bit Transfer Instruction

This type of instruction transfers data in the accumulator (A), working registers (B, H, L, X, Y), and in data memory. It loads immediate data to working registers, data memory, bank select registers (BSR0, BSR1), etc. in 4-bit units.

(2) 8-Bit Transfer Instruction

This type of instruction transfers data in the accumulator (A), B register pair (BA) and other working register pairs, and in HL and XY working register pairs. It loads immediate data to each register pair and data memory in 8-bit units.

(3) Exchange Instruction

This type of instruction exchanges data in the accumulator (A), B register, and data memory in 4-bit units. It also exchanges data in the accumulator (A), B register pair, and data memory in 8-bit units.

(4) 4-Bit Operation Instruction

This type of instruction performs addition, subtraction, AND, OR and exclusive OR operations on data memory content and on immediate data for the accumulator (A), and performs rotation and inversion (complementary operation of 1).

(5) 8-Bit Operation Instruction

This type of instruction performs addition and subtraction on data memory content for the accumulator (A) and B register pair in 8-bit units.

(6) Bit Operation Instruction

This type of instruction sets, resets and tests any bit of the carry flag (C), bank common flag (BCF), bank enable flag (BEF), and data memory.

(7) Increment-Decrement Instruction

This type of instruction increments and decrements the accumulator (A), each of H, L, X and Y registers, and data memory.

(8) Comparison Instruction

This type of instruction compares the accumulator (A), L register, data memory and immediate data, and compares the accumulator (A), B register, and data memory in 4-bit units. It also compares the accumulator (A), B register pair (BA), and data memory in 8-bit units.

(9) Stack Instruction

This type instruction pushes (adds) and pops (removes) information from the accumulator (A), each of B, H, and L registers, and the bank select registers.

(10) Branch Instruction
This is a jump instruction.

(11) Subroutine Instruction
This is a call/return instruction.

(12) NOP Instruction.

The HLT flag, master interrupt enable flag MI, and the stack pointer SP are allocated in data memory space as follows.

BANK0 $7C_H$ address bit 0	:	MI flag
BANK0 $7D_H$ address bit 0	:	HLT flag
BANK0 $7F_H$, $7E_H$ addresses bits 1 to 7	:	SP

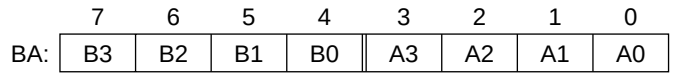
These flags and registers can be read and written by the same control instructions as used for data memory.

To convert to halt mode, for example, write "1" to BANK0 $7D_H$ address bit 0 (HLT).

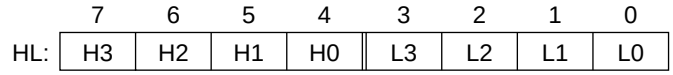
[Explanation of Symbols]

The meanings of the symbols used in the following sections are explained below.

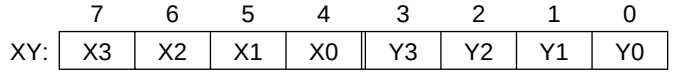
- A ..... Accumulator
- C ..... Carry flag
- B, H, L, X, Y ..... Working registers
- BA ..... Indicates 8-bit data of the content of B registers (B3 to B0), and accumulators (A3 to A0), with B register at the MSB side.



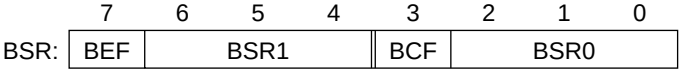
- HL ..... Indicates 8-bit data of the content of H, L registers, with H register at the MSB side.



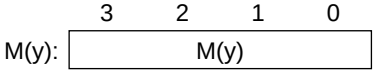
- XY ..... Indicates 8-bit data of the content of X, Y registers, with X register at the MSB side.



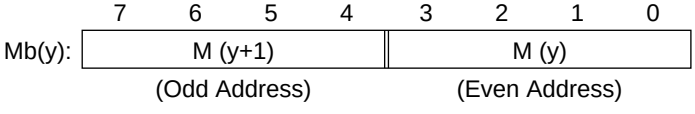
- BSR ..... Indicates bank select registers (BSR1, BSR0), bank common flag (BCF) and bank enable flag (BEF).



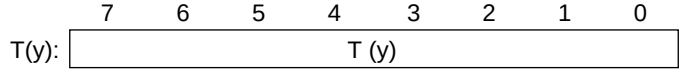
- M (y) ..... Indicates 4-bit data memory content in address indicated by y.



- Mb (y) ..... Indicates 8-bit data memory content in address indicated by y. The data configuration is shown below. The LSB side is always an even address.



- T (y) ..... Indicates 8-bit program memory (ROM) content in address indicated by y (for ROM table data).



- PC ..... Indicates content of program counter (max. 12 bits). The PC value is the program memory address.

- SP ..... Indicates content of stack pointer (8-bit). SP value is the stack address in data memory. SP is allocated to $7F_H$, $7E_H$ addresses of data memory bank0.

SP:

7	6	5	4	3	2	1	0
1	SP6	SP5	SP4	SP3	SP2	SP1	1
($07F_H$ Address)				($07E_H$ Address)			

- ST ..... Indicates 8-bit stack content. This is 8-bit data indicated by SP in data memory. The configuration is shown below.

ST:

7	6	5	4	3	2	1	0
(SP)				(SP–1)			
(Odd Address)				(Even Address)			

- MI ..... Indicates the master interrupt enable flag. MI is allocated to $7C_H$ address, bit 0 of data memory bank0.

- @XY ..... Indicates XY indirect addressing mode instruction. An indirect address mode instruction without this symbol is HL indirect addressing.

- n_x ..... Indicates x bits of immediate data.

- In ..... Indicates immediate data at bit n. (n = 0, 1, 2 • • •)

- a_x ..... Indicates immediate data to be loaded to PC as an x-bit program memory (ROM) address. x-bit is usually from bit 0, but in the table address it is from bit 8.

- m_8 ..... Indicates immediate data to be the low order 8-bit address for direct addressing to data memory.

- r [n_2] ..... Indicates value of bit shown as n_2 (see figure below) in content of r (data memory, working registers, accumulators, etc.).

n_2: 11/ 10/ 01/ 00 ↓ ↓ ↓ ↓

r:	r3	r2	r1	r0

- $\vee$ ..... Indicates OR.
- $\wedge$ ..... Indicates AND.
- $\forall$ ..... Indicates exclusive-OR (EOR).
- X_H ..... "H" indicates that "X" is a hexadecimal value.

- Skip if ..... The next instruction is skipped if the condition is met, that is, the machine cycle time of the next instruction is spent and the next instruction is not executed.
- Carry ..... Indicates the carry of an operation result.
- Borrow ..... Indicates the borrow after an operation result.

18.2 Instruction List

"B" indicates the byte length of an instruction.
"C" indicates the number of execution machine cycles of an instruction.

Mnemonic	Op-code	B	C	Operation
ADC		1	1	A, C ← A + M (HL) + C
ADC	@XY	2	2	A, C ← A + M (XY) + C
ADCB		1	2	BA, C ← BA + M_b (HL) + C
ADCB	@XY	2	3	BA, C ← BA + M_b (XY) + C
ADCS		1	1	A, C ← A + M (HL) + C, Skip if Carry = 1
ADCS	@XY	2	2	A, C ← A + M (XY) + C, Skip if Carry = 1
ADS		1	1	A ← A + M (HL), Skip if Carry = 1
ADS	@XY	2	2	A ← A + M (XY), Skip if Carry = 1
ADSB		1	2	BA ← BA + M_b (HL), Skip if Carry = 1
ADSB	@XY	2	3	BA ← BA + M_b (XY), Skip if Carry = 1
AIS	n_4	1	1	A ← A + n_4, Skip if Carry = 1
AND		1	1	A ← A ∧ M (HL)
AND	@XY	2	2	A ← A ∧ M (XY)
ANDI	n_4	2	2	A ← A ∧ n_4
CAB		1	1	Skip if A = B
CAI	n_4	2	2	Skip if A = n_4
CAL	a_{11}	2	4	ST ← PC + 2, $PC_{10\ to\ 0}$ ← a_{11}, SP ← SP – 2
CAM		1	1	Skip if A = M (HL)
CAM	@XY	2	2	Skip if A = M (XY)
CAMB		1	2	Skip if BA = M_b (HL)
CAMB	@XY	2	3	Skip if BA = M_b (XY)
CAMD	m_8	2	2	Skip if A = M (m_8)
CLI	n_4	2	2	Skip if L = n_4
CMA		2	2	A ← $\overline{A}$
CMI	n_4	2	2	Skip if M (HL) = n_4
CZP	a_5	1	4	ST ← PC + 1, $PC_{4\ to\ 0}$ ← a_5, $PC_{11\ to\ 5}$ ← 0 SP ← SP – 2 (a_5 indicates the even number between 10_H and $1E_H$.)

Mnemonic	Op-code	B	C	Operation
DCA		1	1	A ← A – 1, Skip if A = $0F_H$
DCH		1	1	H ← H – 1, Skip if H = $0F_H$
DCL		1	1	L ← L – 1, Skip if L = $0F_H$
DCM		1	1	M (HL) ← M (HL) – 1, Skip if M (HL) = $0F_H$
DCM	@XY	2	2	M (XY) ← M (XY) – 1, Skip if M (XY) = $0F_H$
DCMD	m_8	2	2	M (m_8) ← M (m_8) – 1, Skip if M (m8) = $0F_H$
DCX		1	1	X ← X – 1, Skip if X = $0F_H$
DCY		1	1	Y ← Y – 1, Skip if Y = $0F_H$
EOR		1	1	A ← A ∀ M (HL)
EOR	@XY	2	2	A ← A ∀ M (XY)
EORI	n_4	2	2	A ← A ∀ n_4
INA		1	1	A ← A + 1, Skip if A = 0
INH		1	1	H ← H + 1, Skip if H = 0
INL		1	1	L ← L + 1, Skip if L = 0
INM		1	1	M (HL) ← M (HL) + 1, Skip if M (HL) = 0
INM	@XY	2	2	M (XY) ← M (XY) + 1, Skip if M (XY) = 0
INMD	m_8	2	2	M (m_8) ← M (m_8) + 1, Skip if M (m_8) = 0
INX		1	1	X ← X + 1, Skip if X = 0
INY		1	1	Y ← Y + 1, Skip if Y = 0
JA		1	1	$PC_{5\ to\ 0}$ ← BA (bit 0 to bit 5)
JCP	a_6	1	1	$PC_{5\ to\ 0}$ ← a_6
JM		1	3	$PC_{11\ to\ 0}$ ← M_b (HL), BA
JP	a_{11}	2	2	$PC_{10\ to\ 0}$ ← a_{11}
LAB		2	2	A ← B
LAH		1	1	A ← H
LAI	n_4	1	1	A ← n_4 (Vertical Stack Instruction)
LAL		1	1	A ← L
LALB		2	2	BA ← HL
LAM		1	1	A ← M (HL)
LAM	@XY	2	2	A ← M (XY)

Mnemonic	Op-code	B	C	Operation
LAMB		1	2	BA ← M_b (HL)
LAMB	@XY	2	3	BA ← M_b (XY)
LAMD	m_8	2	2	A ← M (m_8)
LAMDB	m_8	2	2	BA ← M_b (m_8)
LAMM	n_2	1	1	A ← M (HL), H ← H ∀ n_2
LAM+		1	2	A ← M (HL), L ← L + 1, Skip if L = 0
LAM–		1	2	A ← M (HL), L ← L – 1, Skip if L = $0F_H$
LAX		1	1	A ← X
LAY		1	1	A ← Y
LAYB		2	2	BA ← XY
LBA		2	2	B ← A
LBAI	n_8	2	2	BA ← n_8
LBS0I	n_3	2	2	BSR0 ← n_3
LBS1I	n_3	2	2	BSR1 ← n_3
LCAL	a_{12}	3	5	ST ← PC + 3, PC ← a_{12}, SP ← SP – 2
LHA		1	1	H ← A
LHI	n_4	2	2	H ← n_4
LHLI	n_8	2	2	HL ← n_8
LJP	a_{12}	3	5	$PC_{11\ to\ 0}$ ← a_{12}
LLA		1	1	L ← A
LLAB		2	2	HL ← BA
LLI	n_4	1	1	L ← n_4 (Vertical Stack Instruction)
LMA		1	1	M (HL) ← A
LMA	@XY	2	2	M (XY) ← A
LMAB		1	2	M_b (HL) ← BA
LMAB	@XY	2	3	M_b (XY) ← BA
LMAD	m_8	2	2	M (m_8) ← A
LMADB	m_8	2	2	M_b (m_8) ← BA
LMA+		1	2	M (HL) ← A, L ← L + 1, Skip if L = 0
LMA–		1	2	M (HL) ← A, L ← L – 1, Skip if L = $0F_H$

Mnemonic	Op-code	B	C	Operation
LMBI	n_8	2	2	M_b (HL) ← n_8
LMBI	@XY, n_8	3	3	M_b (XY) ← n_8
LMI	n_4	2	2	M (HL) ← n_4
LMTB	a_4	2	3	M_b (HL) ← T (a_4, XY)
LXA		1	1	X ← A
LXI	n_4	2	2	X ← n_4
LXYI	n_8	2	2	XY ← n_8
LYA		1	1	Y ← A
LYAB		2	2	XY ← BA
LYI	n_4	2	2	Y ← n_4
NOP		1	1	No operation
OR		1	1	A ← A ∨ M (HL)
OR	@XY	2	2	A ← A ∨ M (XY)
ORI	n_4	2	2	A ← A ∨ n_4
POP	BA	1	2	SP ← SP + 1, BA ← ST
POP	HL	1	2	SP ← SP + 1, HL ← ST
POP	BSR	1	2	SP ← SP + 1, BSR ← ST
PUSH	BA	1	2	ST ← BA, SP ← SP – 1
PUSH	HL	1	2	ST ← HL, SP ← SP – 1
PUSH	BSR	1	2	ST ← BSR, SP ← SP – 1
RAL		1	1	C ← A_3, A_3 ← A_2, A_2 ← A_1, A_1 ← A_0, A_0 ← C
RAR		1	1	C ← A_0, A_0 ← A_1, A_1 ← A_2, A_2 ← A_3, A_3 ← C
RBC		1	1	BCF ← 0
RBE		1	1	BEF ← 0
RC		1	1	C ← 0
RMB	n_2	1	1	M (HL) [n_2] ← 0
RMB	@XY, n_2	2	2	M (XY) [n_2] ← 0
RMBD	m_8, n_2	2	2	M (m_8) [n_2] ← 0
RT		1	3	$PC_{11\ to\ 0}$ ← ST, SP ← SP + 2
RTI		1	5	$PC_{11\ to\ 0}$ • C • HL • BA ← ST, SP ← SP + 4, MI ← 1
RTS		1	3	$PC_{11\ to\ 0}$ ← ST, SP ← SP + 2, Then skip

Mnemonic	Op-code	B	C	Operation
SBC		1	1	BCF ← 1
SBE		1	1	BEF ← 1
SC		1	1	C ← 1
SMB	n_2	1	1	M (HL) [n_2] ← 1
SMB	@XY, n_2	2	2	M (XY) [n_2] ← 1
SMBD	m_8, n_2	2	2	M (m_8) [n_2] ← 1
SUBC		1	1	A, C ← A – M (HL) – C
SUBC	@XY	2	2	A, C ← A – M (XY) – C
SUBCB		1	2	BA, C ← BA – M_b (HL) – C
SUBCB	@XY	2	3	BA, C ← BA – M_b (XY) – C
SUBCS		1	1	A, C ← A – M (HL) – C, Skip if Borrow = 0
SUBCS	@XY	2	2	A, C ← A – M (XY) – C, Skip if Borrow = 0
SUBS		1	1	A ← A – M (HL), Skip if Borrow = 1
SUBS	@XY	2	2	A ← A – M (XY), Skip if Borrow = 1
SUBSB		1	2	BA ← BA – M_b (HL), Skip if Borrow = 1
SUBSB	@XY	2	3	BA ← BA – M_b (XY), Skip if Borrow = 1
TAB	n_2	1	1	Skip if A [n_2] = 1
TC		1	1	Skip if C = 1
TMB	n_2	1	1	Skip if M (HL) [n_2] = 1
TMB	@XY, n_2	2	2	Skip if M (XY) [n_2] = 1
TMBD	m_8, n_2	2	2	Skip if M (m_8) [n_2] = 1
XAB		1	2	A ↔ B
XAM		1	1	A ↔ M (HL)
XAM	@XY	2	2	A ↔ M (XY)
XAMB		1	2	BA ↔ M_b (HL)
XAMB	@XY	2	3	BA ↔ M_b (XY)
XAMD	m_8	2	2	A ↔ M (m_8)
XAMDB	m_8	2	2	BA ↔ M_b (m_8)
XAMM	n_2	1	1	A ↔ M (HL), H ← H ∀ n_2
XAM+		1	2	A ↔ M (HL), L ← L + 1, Skip if L = 0
XAM–		1	2	A ↔ M (HL), L ← L – 1, Skip if L = $0F_H$

18.3 Instruction Code Table

(1) 1st Byte

H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	INA	AIS													
1	CZP	RBC	CZP	SBC	CZP	RBE	CZP	SBE	CZP	RC	CZP	SC	CZP	TC	CZP	DCA
2	TMBD				RMBD				SMBD				LAMD	LMAD	LAM DB	LMA DB
3	TAB				LAM+	LAM–	LMA+	LMA–	XAM+	XAM–	LBAI	CAMD	XAMD	XAM DB	INMD	DCMD
4	LAL	LAH	LAY	LAX	LLA	LHA	LYA	LXA	INL	INH	INY	INX	DCL	DCH	DCY	DCX
5	LHLI	LXYI	XAB	CAB	RAR	RAL	XAMB	LMBI	ADCB	ADSB	SUB CB	SUB SB	CAM	CAMB	LAMB	LMAB
6	TMB				RMB				SMB				AND	OR	EOR	LMA
7	LAM	LAMM			XAM	XAMM			ADC	ADS	SUBC	SUBS	ADCS	SUB CS	INM	DCM
8	LLI															
9	LAI															
A	CAL								JP							
B	PUSH BA	PUSH HL	PUSH BSR	JA	POP BA	POP HL	POP BSR	LMTB	RT	RTS	JM	RTI	LIP	LCAL		
C	JCP															
D																
E																
F																

(2) 2nd Byte (other than @XY [XY indirect addressing] instruction)

H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	LHI															
1	LYI															
2	LXI															
3	LMI															
4	CAI															
5	CLI															
6	CMI															
7	ANDI															
8	ORI															
9	EORI															CMA
A	LBS0I								LBS1I							
B	LAB	LBA			LALB	LAYB	LLAB	LYAB								
C																
D																
E																
F																

(3) 2nd Byte (for @XY [XY indirect addressing] instruction)

H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0																
1																
2																
3																
4																
5							XAMB	LMBI	ADCB	ADSB	SUB CB	SUB SB	CAM	CAMB	LAMB	LMAB
6	TMB				RMB				SMB				AND	OR	EOR	LMA
7	LAM				XAM				ADC	ADS	SUBC	SUBS	ADCS	SUB CS	INM	DCM
8																
9																
A																
B																
C																
D																
E																
F																

Appendixes

[ML64168]
Appendix A:

List of Special Function Registers

Register name	Symbol	Address	b3	b2	b1	b0	R/W	Byte access	Value at system reset
Port 2 register	P2	00H	P23	P22	P21	P20	R/W	yes	0H
Port 3 register	P3	01H	P33	P32	P31	P30	R/W		0H
Port 4 register	P4	02H	P43	P42	P41	P40	R/W	yes	0H
Port 0 register	P0	03H	P03	P02	P01	P00	R		Depends on input value
Port 1 register	P1	04H	P13	P12	P11	P10	R/W	no	0H
Serial port buffer lower register	SBUFL	06H	SD3	SD2	SD1	SD0	R/W	yes	0H
Serial port buffer upper register	SBUFH	07H	SD7	SD6	SD5	SD4	R/W		0H
Serial port control register	SCON	08H	SDIR	EXSC	SEND	ENTR	R/W	no	0H
Frequency control register	FCON	09H	*—	*—	*—	CPUCLK	R/W	no	0EH
Buzzer driver control register	BDCON	0AH	SELF	EBD	BM1	BM0	R/W	yes	0H
Buzzer frequency control register	BFCON	0BH	BF3	BF2	BF1	BF0	R/W		0H
Capture register 0	CAPR0	0CH	32Hz	64Hz	128Hz	256Hz	R	yes	0H
Capture register 1	CAPR1	0DH	32Hz	64Hz	128Hz	256Hz	R		0H
Capture control register	CAPCON	0EH	CRF1	CRF0	ECAP1	ECAP0	R/W	no	0H
Time base counter register	TBCR	0FH	1Hz	2Hz	4Hz	8Hz	R/W	no	0H
Port 20 control register	P20CON	10H	P20IE	P20F	P20DIR	P20MOD	W	yes	0H
Port 21 control register	P21CON	11H	P21IE	P21F	P21DIR	P21MOD	W		0H
Port 22 control register	P22CON	12H	P22IE	P22F	P22DIR	P21MOD	W	yes	0H
Port 23 control register	P23CON	13H	P23IE	P23F	P23DIR	P23MOD	W		0H

Register name	Symbol	Address	b3	b2	b1	b0	R/W	Byte access	Value at system reset
Port 30 control register	P30CON	14H	P30IE	P30F	P30DIR	P30MOD	W	yes	0H
Port 31 control register	P31CON	15H	P31IE	P31F	P31DIR	P31MOD	W		0H
Port 32 control register	P32CON	16H	P32IE	P32F	P32DIR	P32MOD	W	yes	0H
Port 33 control register	P33CON	17H	P33IE	SIN	P33DIR	P33MOD	W		0H
Port 40 control register	P40CON	18H	P40IE	SOUT	P40DIR	P40MOD	W	yes	0H
Port 41 control register	P41CON	19H	P41IE	SPR	P41DIR	P41MOD	W		0H
Port 42 control register	P42CON	1AH	P42IE	SCLK	P42DIR	P42MOD	W	yes	0H
Port 43 control register	P43CON	1BH	P43IE	MON	P43DIR	P43MOD	W		0H
Port 01 control register	P01CON	1CH	*—	PUD	P1MOD	P0MOD	W	no	8H
Display control register	DSPCON	1EH	*—	*—	DUTY1	DUTY0	R/W	no	0CH
A/D converter counter A register 0	CNTA0	20H	a3	a2	a1	a0	R/W	yes	0H
A/D converter counter A register 1	CNTA1	21H	a7	a6	a5	a4	R/W		0H
A/D converter counter A register 2	CNTA2	22H	a11	a10	a9	a8	R/W	yes	0H
A/D converter counter A register 3	CNTA3	23H	a15	a14	a13	a12	R/W		0H
A/D converter counter A register 4	CNTA4	24H	*—	a18	a17	a16	R/W	no	8H
A/D converter counter B register 0	CNTB0	26H	b3	b2	b1	b0	R/W	yes	0H
A/D converter counter B register 1	CNTB1	27H	b7	b6	b5	b4	R/W		0H
A/D converter counter B register 2	CNTB2	28H	b11	b10	b9	b8	R/W	yes	0H

Register name	Symbol	Address	b3	b2	b1	b0	R/W	Byte access	Value at system reset
A/D converter counter B register 3	CNTB3	29H	*—	*—	b13	b12	R/W	yes	0CH
A/D converter control register 0	ADCON0	2AH	*—	*—	SADI	EADC	R/W	yes	0CH
A/D converter control register 1	ADCON1	2BH	OM3	OM2	OM1	OM0	R/W		0H
Interrupt enable register 0	IE0	30H	EAD	EXI1	ESIO	EXI0	R/W	yes	0H
Interrupt enable register 1	IE1	31H	E1Hz	E16Hz	E32Hz	E256Hz	R/W		0H
Interrupt enable register 2	IE2	32H	*—	*—	*—	E01Hz	R/W	yes	0EH
Interrupt request register 2	IRQ2	33H	*—	*—	QWDT	Q01Hz	R/W		0CH
Interrupt request register 0	IRQ0	34H	QAD	QXI1	QSIO	QXI0	R/W	yes	0H
Interrupt request register 1	IRQ1	35H	Q1Hz	Q16Hz	Q32Hz	Q256Hz	R/W		0H
Watchdog timer control register	WDTCON	36H	d3	d2	d1	d0	W	no	0H
Backup control register	BUPCON	37H	*—	CMPF	ECMP	*1BUPF	R/W	no	08H
Display register 0	DSPR0	40H	d	c	b	a	R/W	yes	0H
Display register 1	DSPR1	41H	d	c	b	a	R/W		0H
Display register 2	DSPR2	42H	d	c	b	a	R/W	yes	0H
Display register 3	DSPR3	43H	d	c	b	a	R/W		0H
Display register 4	DSPR4	44H	d	c	b	a	R/W	yes	0H
Display register 5	DSPR5	45H	d	c	b	a	R/W		0H
Display register 6	DSPR6	46H	d	c	b	a	R/W	yes	0H
Display register 7	DSPR7	47H	d	c	b	a	R/W		0H
Display register 8	DSPR8	48H	d	c	b	a	R/W	yes	0H
Display register 9	DSPR9	49H	d	c	b	a	R/W		0H
Display register 10	DSPR10	4AH	d	c	b	a	R/W	yes	0H

*1: The OTP version has different specifications. See page 17-7.

Register name	Symbol	Address	b3	b2	b1	b0	R/W	Byte access	Value at system reset
Display register 11	DSPR11	4BH	d	c	b	a	R/W	yes	0H
Display register 12	DSPR12	4CH	d	c	b	a	R/W	yes	0H
Display register 13	DSPR13	4DH	d	c	b	a	R/W		0H
Display register 14	DSPR14	4EH	d	c	b	a	R/W	yes	0H
Display register 15	DSPR15	4FH	d	c	b	a	R/W		0H
Display register 16	DSPR16	50H	d	c	b	a	R/W	yes	0H
Display register 17	DSPR17	51H	d	c	b	a	R/W		0H
Display register 18	DSPR18	52H	d	c	b	a	R/W	yes	0H
Display register 19	DSPR19	53H	d	c	b	a	R/W		0H
Display register 20	DSPR20	54H	d	c	b	a	R/W	yes	0H
Display register 21	DSPR21	55H	d	c	b	a	R/W		0H
Display register 22	DSPR22	56H	d	c	b	a	R/W	yes	0H
Display register 23	DSPR23	57H	d	c	b	a	R/W		0H
Display register 24	DSPR24	58H	d	c	b	a	R/W	yes	0H
Display register 25	DSPR25	59H	d	c	b	a	R/W		0H
Display register 26	DSPR26	5AH	d	c	b	a	R/W	yes	0H
Display register 27	DSPR27	5BH	d	c	b	a	R/W		0H
Display register 28	DSPR28	5CH	d	c	b	a	R/W	yes	0H
Display register 29	DSPR29	5DH	d	c	b	a	R/W		0H
Display register 30	DSPR30	5EH	d	c	b	a	R/W	no	0H
Master interrupt enable register	MIEF	7CH	*—	*—	*—	MI	R/W	no	0EH
Halt mode register	HALT	7DH	*—	*—	*—	HLT	R/W	no	0EH
Stack pointer	SP	7EH	SP3	SP2	SP1	*—	R/W	yes	0FFH
		7FH	*—	SP6	SP5	SP4			

Notes:

(1) Only byte access is possible for the Stack pointer.

(2) "*—" in the table is a reserved bit. "1" is always read out. Not valid for write.

(3) The display registers 0 through 30 are registers that cannot be used without selection by the mask option.
All the display registers to be used must be allocated on the LCD driver mask option table per bit. (Refer to Appendix F on the mask options.)

Appendix B:

Description of Special Function Registers

Register name	Symbol	Address	Read/Write	Value at system reset
Port 2 register	P2	00H	R/W	0H
Port 20 control register	P20CON	10H	W	0H
Port 21 control register	P21CON	11H	W	0H
Port 22 control register	P22CON	12H	W	0H
Port 23 control register	P23CON	13H	W	0H

P2 (00H) (R/W)

b_3	b_2	b_1	b_0
P23	P22	P21	P20

P20CON (10H) (W)

b_3	b_2	b_1	b_0
P20IE	P20F	P20DIR	P20MOD

P2.0 Selection of external interrupt disable/enable
- 0: Interrupt disable (initial value)
- 1: Interrupt enable

P2.0 Selection of external interrupt sampling clock
- 0: 64 Hz (initial value)
- 1: System clock

P2.0 Selection of input/output mode
- 0: Input mode (initial value)
- 1: Output mode

P2.0 Selection of pull-down/pull-up resistance input or high impedance input (in input mode)
- 0: Pull-down/pull-up resistance input (initial value)
- 1: High impedance input

P2.0 Selection of CMOS output/NMOS open drain output (in output mode)
- 0: CMOS output (initial value)
- 1: NMOS open drain output

P21 (11H) (W)

b_3	b_2	b_1	b_0
P21IE	P21F	P21DIR	P21MOD

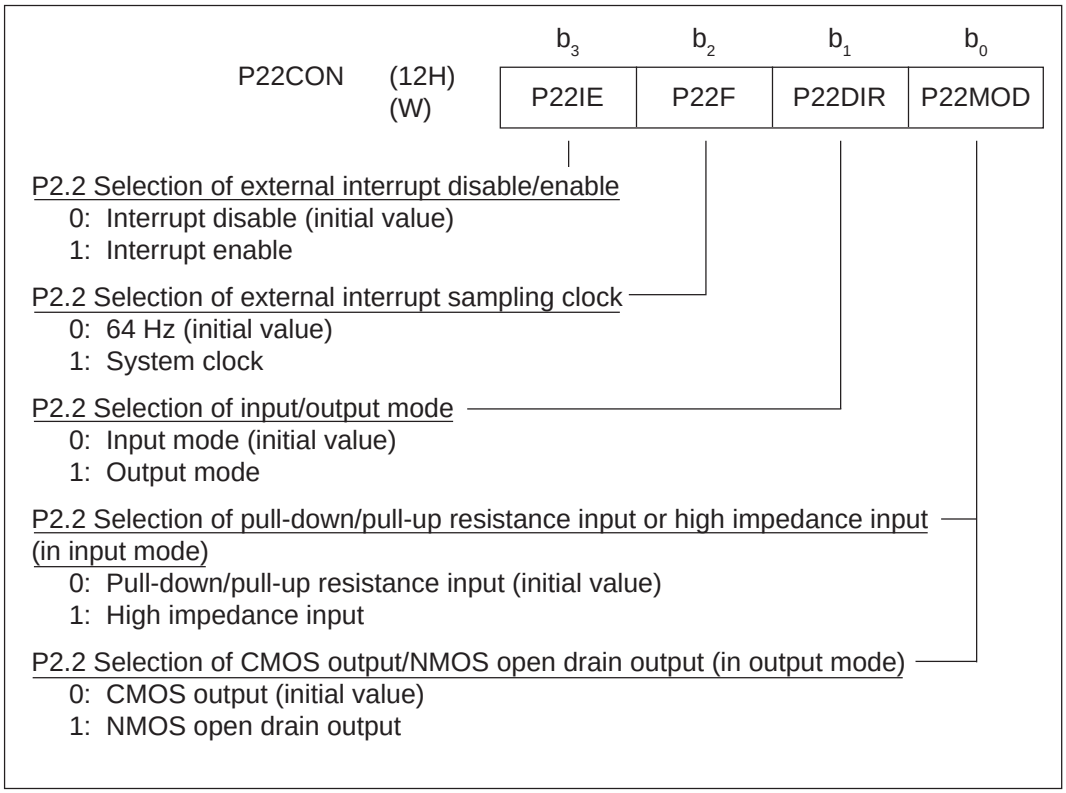
P2.1 Selection of external interrupt disable (initial value)
- 0: Interrupt disable (initial value)
- 1: Interrupt enable

P2.1 Selection of external interrupt sampling clock
- 0: 64 Hz (initial value)
- 1: System clock

P2.1 Selection of input/output mode
- 0: Input mode (initial value)
- 1: Output mode

P2.1 Selection of pull-down/pull-up resistance input or high impedance input (in input mode)
- 0: Pull-down/pull-up resistance input (initial value)
- 1: High impedance input

P2.1 Selection of CMOS output/NMOS open drain output (in output mode)
- 0: CMOS output (initial value)
- 1: NMOS open drain output



P2.2 Selection of external interrupt disable/enable
- 0: Interrupt disable (initial value)
- 1: Interrupt enable

P2.2 Selection of external interrupt sampling clock
- 0: 64 Hz (initial value)
- 1: System clock

P2.2 Selection of input/output mode
- 0: Input mode (initial value)
- 1: Output mode

P2.2 Selection of pull-down/pull-up resistance input or high impedance input (in input mode)
- 0: Pull-down/pull-up resistance input (initial value)
- 1: High impedance input

P2.2 Selection of CMOS output/NMOS open drain output (in output mode)
- 0: CMOS output (initial value)
- 1: NMOS open drain output

P23CON (13H) (W)

b_3	b_2	b_1	b_0
P23IE	P23F	P23DIR	P23MOD

P2.3 Selection of external interrupt disable/enable
- 0: Interrupt disable (initial value)
- 1: Interrupt enable

P2.3 Selection of external interrupt sampling clock
- 0: 64 Hz (initial value)
- 1: System clock

P2.3 Selection of input/output mode
- 0: Input mode (initial value)
- 1: Output mode

P2.3 Selection of pull-down/pull-up resistance input or high impedance input (in input mode)
- 0: Pull-down/pull-up resistance input (initial value)
- 1: High impedance input

P2.3 Selection of CMOS output/NMOS open drain output (in output mode)
- 0: CMOS output (initial value)
- 1: NMOS open drain output

Description

The Port 2 register (P2) is a data register to output to Port 2. When P2 is read out while Bit 1 (each DIR bit) of P20CON to P23CON is reset to "0" in input mode, the pin level of each bit is read out for those bits where input mode is selected.

The Port 20 to 23 control registers (P20CON, P21CON, P22CON and P23CON) perform selection of input/output mode, selection of pull-down/pull-up resistance input/ high-impedance input in input mode, selection of CMOS/NMOS open drain output in output mode, selection of sampling clocks when used as external interrupt input and selection of external interrupt enable/disable for Port 2. Selection of pull-down/pull-up resistance input is performed by Bit 2 (PUD) of the Port 01 control register (P01CON).

Register name	Symbol	Address	Read/Write	Value at system reset
Port 3 register	P3	01H	R/W	0H
Port 30 control register	P30CON	14H	W	0H
Port 31 control register	P31CON	15H	W	0H
Port 32 control register	P32CON	16H	W	0H
Port 33 control register	P33CON	17H	W	0H

P3 (01H) (R/W)

b_3	b_2	b_1	b_0
P33	P32	P31	P30

P30CON (14H) (W)

b_3	b_2	b_1	b_0
P30IE	P30F	P30DIR	P30MOD

P3.0 Selection of external interrupt disable/enable
- 0: Interrupt disable (initial value)
- 1: Interrupt enable

P3.0 Selection of external interrupt sampling clock
- 0: 64 Hz (initial value)
- 1: System clock

P3.0 Selection of input/output mode
- 0: Input mode (initial value)
- 1: Output mode

P3.0 Selection of pull-down/pull-up resistance input or high impedance input (in input mode)
- 0: Pull-down/pull-up resistance input (initial value)
- 1: High impedance input

P3.0 Selection of CMOS output/NMOS open drain output (in output mode)
- 0: CMOS output (initial value)
- 1: NMOS open drain output

P31CON (15H) (W)

b_3	b_2	b_1	b_0
P31IE	P31F	P31DIR	P31MOD

P3.1 Selection of external interrupt disable/enable

0: Interrupt disable (initial value)
1: Interrupt enable

P3.1 Selection of external interrupt sampling clock

0: 64 Hz (initial value)
1: System clock

P3.1 Selection of input/output mode

0: Input mode (initial value)
1: Output mode

P3.1 Selection of pull-down/pull-up resistance input or high impedance input (in input mode)

0: Pull-down/pull-up resistance input (initial value)
1: High impedance input

P3.1 Selection of CMOS output/NMOS open drain output (in output mode)

0: CMOS output (initial value)
1: NMOS open drain output

P32CON (16H) (W)

b_3	b_2	b_1	b_0
P32IE	P32F	P32DIR	P32MOD

P3.2 Selection of external interrupt disable/enable
- 0: Interrupt disable (initial value)
- 1: Interrupt enable

P3.2 Selection of external interrupt sampling clock
- 0: 64 Hz (initial value)
- 1: System clock

P3.2 Selection of input/output mode
- 0: Input mode (initial value)
- 1: Output mode

P3.2 Selection of pull-down/pull-up resistance input or high impedance input (in input mode)
- 0: Pull-down/pull-up resistance input (initial value)
- 1: High impedance input

P3.2 Selection of CMOS output/NMOS open drain output (in output mode)
- 0: CMOS output (initial value)
- 1: NMOS open drain output

P33CON (17H) (W)

b_3	b_2	b_1	b_0
P33IE	SIN	P33DIR	P33MOD

P3.3 Selection of external interrupt disable/enable

0: Interrupt disable (initial value)
1: Interrupt enable

P3.3 Switching of SIN pin function

0: Input/output port function (initial value)
1: Serial port data input function

P3.3 Selection of input/output mode

0: Input mode (initial value)
1: Output mode

P3.3 Selection of pull-down/pull-up resistance input or high impedance input (in input mode)

0: Pull-down/pull-up resistance input (initial value)
1: High impedance input

P3.3 Selection of CMOS output/NMOS open drain output (in output mode)

0: CMOS output (initial value)
1: NMOS open drain output

Description

The Port 3 register (P3) is a data register to output to Port 3. When P3 is read out while Bit 1 (each DIR bit) of P30CON to P33CON is reset to "0" in input mode, the pin level of each bit is read out for those bits where input mode is selected.

The Port 30 to 33 control registers (P30CON, P31CON, P32CON and P33CON) perform selection of input/output mode, selection of pull-down/pull-up resistance input/ high-impedance input in input mode, selection of CMOS/NMOS open drain output in output mode, selection of sampling clocks when used as external interrupt input and selection of external interrupt enable/disable for Port 3. There is no selection function of sampling clocks for P3.3. Selection of pull-down/pull-up resistance input is performed by Bit 2 (PUD) of the Port 01 control register (P01CON).

Register name	Symbol	Address	Read/Write	Value at system reset
Port 4 register	P4	02H	R/W	0H
Port 40 control register	P40CON	18H	W	0H
Port 41 control register	P41CON	19H	W	0H
Port 42 control register	P42CON	1AH	W	0H
Port 43 control register	P43CON	1BH	W	0H

P4 (02H) (R/W)

b_3	b_2	b_1	b_0
P43	P42	P41	P40

P40CON (18H) (W)

b_3	b_2	b_1	b_0
P40IE	SOUT	P40DIR	P40MOD

P4.0 Selection of external interrupt disable/enable
- 0: Interrupt disable (initial value)
- 1: Interrupt enable

P4.0 Switching of SOUT pin function
- 0: Input/output port function (initial value)
- 1: Serial port data output function

P4.0 Selection of input/output mode
- 0: Input mode (initial value)
- 1: Output mode

P4.0 Selection of pull-down/pull-up resistance input or high impedance input (in input mode)
- 0: Pull-down/pull-up resistance input (initial value)
- 1: High impedance input

P4.0 Selection of CMOS output/NMOS open drain output (in output mode)
- 0: CMOS output (initial value)
- 1: NMOS open drain output

P41CON (19H) (W)

b_3	b_2	b_1	b_0
P41IE	SPR	P41DIR	P41MOD

P4.1 Selection of external interrupt disable/enable

0: Interrupt disable (initial value)
1: Interrupt enable

P4.1 Switching of /SPR pin function

0: Input/output port function (initial value)
1: Serial port ready signal output function

P4.1 Selection of input/output mode

0: Input mode (initial value)
1: Output mode

P4.1 Selection of pull-down/pull-up resistance input or high impedance input (in input mode)

0: Pull-down/pull-up resistance input (initial value)
1: High impedance input

P4.1 Selection of CMOS output/NMOS open drain output (in output mode)

0: CMOS output (initial value)
1: NMOS open drain output

P42CON (1AH) (W)

b_3	b_2	b_1	b_0
P42IE	SCLK	P42DIR	P42MOD

P4.2 Selection of external interrupt disable/enable

0: Interrupt disable (initial value)
1: Interrupt enable

P4.2 Switching of SCLK pin function

0: Input/output port function (initial value)
1: Serial port clock input/output function

P4.2 Selection of input/output mode

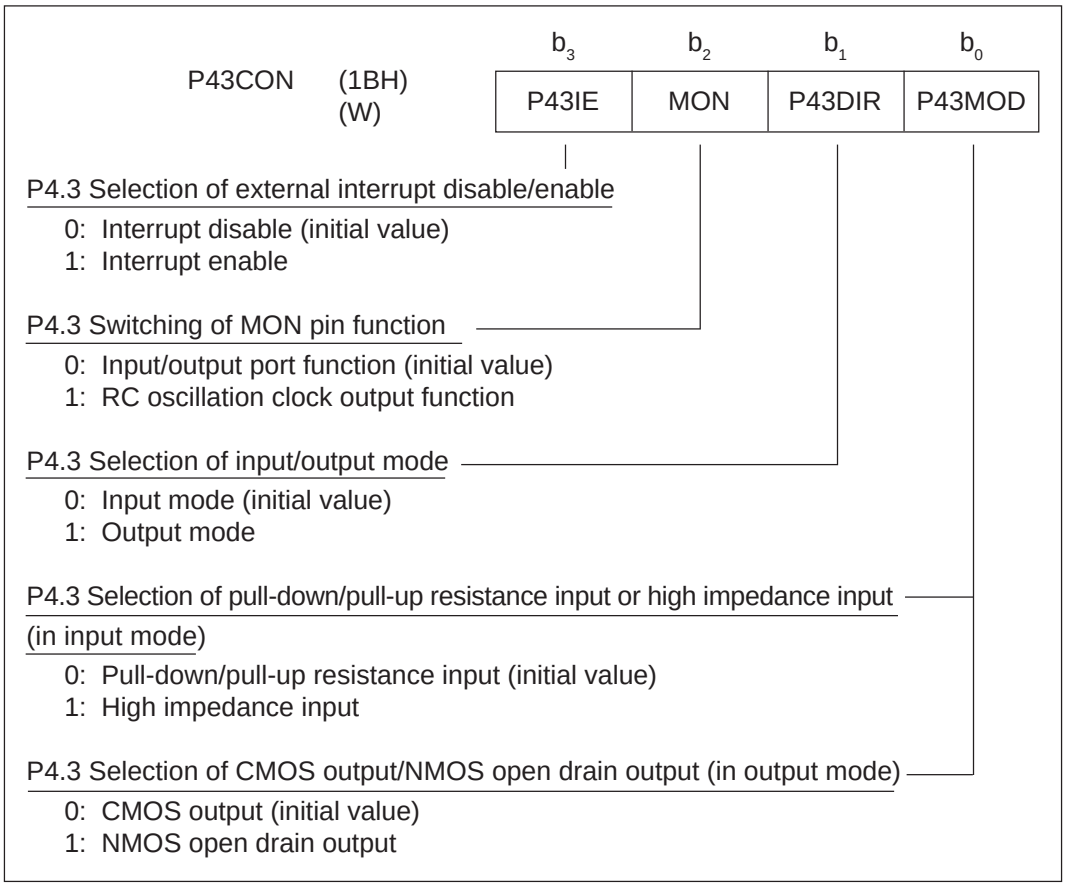
0: Input mode (initial value)
1: Output mode

P4.2 Selection of pull-down/pull-up resistance input or high impedance input (in input mode)

0: Pull-down/pull-up resistance input (initial value)
1: High impedance input

P4.2 Selection of CMOS output/NMOS open drain output (in output mode)

0: CMOS output (initial value)
1: NMOS open drain output



Description

The Port 4 register (P4) is a data register to output to Port 4. When P4 is read out while Bit 1 (each DIR bit) of P40CON to P43CON is reset to "0" in input mode, the pin level of each bit is read out for those bits where input mode is selected.

The Port 40 to 43 control registers (P40CON, P41CON, P42CON and P43CON) perform selection of input/output mode, selection of pull-down/pull-up resistance input/ high-impedance input in input mode, selection of CMOS/NMOS open drain output in output mode and selection of external interrupt enable/disable for Port 4. P4.1 can select input/output port functions/serial port data ready output functions. P4.2 can select input/ output port functions or serial port clock input/output functions. P4.3 can select input/ output port functions or clock monitor functions of the RC oscillation circuit. Selection of pull-down/pull-up resistance input is performed by Bit 2 (PUD) of the Port 01 control register (P01CON).

Register name	Symbol	Address	Read/Write	Value at system reset
Port 0 register	P0	03H	R	Depends on input value
Port 1 register	P1	04H	R/W	0H
Port 01 control register	P01CON	1CH	W	8H

P0 (03H) (R)

b_3	b_2	b_1	b_0
P03	P02	P01	P00

Pin level of each bit of Port 0

0: "L" level

1: "H" level

Description

The Port 0 register (P0) is a read-only port and each pin level of Port 0 is read out.

P1 (04H) (R/W)

b_3	b_2	b_1	b_0
P13	P12	P11	P10

Description

The Port 1 register (P1) is a data register to output data to Port 1.

P01CON (1CH) (W)

b_3	b_2	b_1	b_0
-----*	PUD	P1MOD	P0MOD

Selection of P0, P2, P3 and P4 input mode

0: Pull-up resistance input (initial value)
1: Pull-down resistance input

Selection of P1 output mode

0: CMOS output (initial value)
1: NMOS open drain output

Selection of P0 input mode

0: Pull-down/pull-up resistance input (initial value)
1: High-impedance input

*Reserved bit: Not valid for write.

Description

Bit 2 (PUD) of the Port 01 control register (P01CON) selects pull-down resistance input or pull-up resistance input when pull-down/pull-up resistance input is selected at P0, P2, P3 and P4.

Bit 1 (P1MOD) of P01CON selects CMOS output or NMOS open drain output of Port 1.

Bit 0 (P0MOD) of P01CON selects pull-down/pull-up resistance input or high impedance input of Port 0.

Register name	Symbol	Address	Read/Write	Value at system reset
Serial port buffer lower register	SBUFL	06H	R/W	0H
Serial port buffer upper register	SBUFH	07H	R/W	0H
Serial port control register	SCON	08H	R/W	0H

SBUFL (06H)
(R/W)

b_3	b_2	b_1	b_0
SD3	SD2	SD1	SD0
			(LSB)

Value of lower 4 bits of the serial port buffer

SBUFH (07H)
(R/W)

b_3	b_2	b_1	b_0
SD7	SD6	SD5	SD4
(MSB)			

Value of upper 4 bits of the serial port buffer

SCON (08H)
(R/W)

b_3	b_2	b_1	b_0
SDIR	EXSC	SEND	ENTR

Selection of transfer data
- 0: MSB (SD7) head (initial value)
- 1: LSB (SD0) head

Selection of serial clock
- 0: Internal clock (initial value)
- 1: External clock

Serial transfer completion flag
- 0: Transfer not completed (initial value)
- 1: Transfer completed

Serial transfer enable flag
- 0: Transfer halted (initial value)
- 1: Transfer started

Description

The Serial port buffer lower register (SBUFL) and the Serial port buffer upper register (SBUFH) are used to write send data and to read receive data.

The Serial port control register (SCON) selects the direction of serial transfer data, selection of the internal or the external system clock and confirms the start and the end of serial transfer. Bit 1 (SEND) of SCON is a read only bit.

Register name	Symbol	Address	Read/Write	Value at system reset
Frequency control register	FCON	09H	R/W	0EH

FCON (09H) (R/W)

b_3	b_2	b_1	b_0
-----*	-----*	-----*	CPUCLK

Selection of system clock

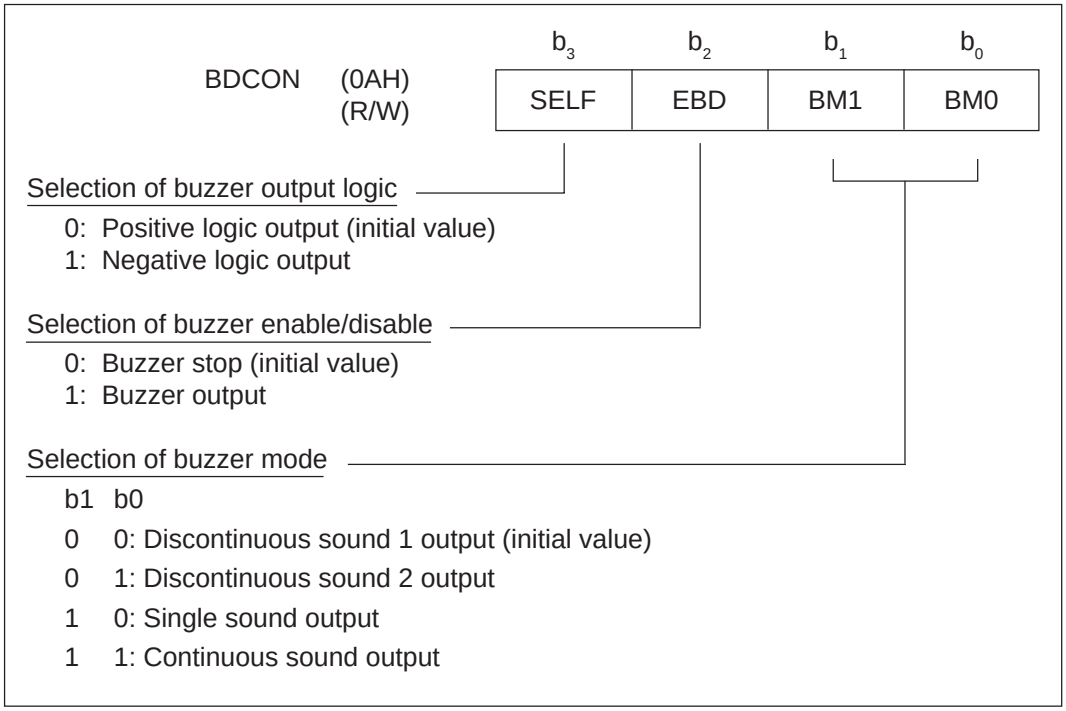
0: Crystal oscillation output (initial value)
1: 700 kHz RC oscillation output

*Reserved bit: "1" is always read out. Not valid for write.

Description

The Frequency control register (FCON) selects system clocks. When reset to "0", the crystal oscillation output (32.768 kHz) is selected and when set to "1", the RC oscillation output is selected.

Register name	Symbol	Address	Read/Write	Value at system reset
Buzzer driver control register	BDCON	0AH	R/W	0H
Buzzer frequency control register	BFCON	0BH	R/W	0H



BFCON (0BH) (R/W)

b_3	b_2	b_1	b_0
BF3	BF2	BF1	BF0

Selection of buzzer output frequency

b3	b2	b1	b0	
0	0	0	0:	Output stops (initial value)
0	0	0	1:	5.461 kHz
0	0	1	0:	4.096 kHz
0	0	1	1:	3.277 kHz
0	1	0	0:	2.730 kHz
0	1	0	1:	2.341 kHz
0	1	1	0:	2.048 kHz
0	1	1	1:	1.820 kHz
1	0	0	0:	1.638 kHz
1	0	0	1:	1.489 kHz
1	0	1	0:	1.365 kHz
1	0	1	1:	1.260 kHz
1	1	0	0:	1.170 kHz
1	1	0	1:	1.092 kHz
1	1	1	0:	1.024 kHz
1	1	1	1:	0.964 kHz

Description

The Buzzer driver control register (BDCON) is a register to select buzzer output logic, buzzer output enable/disable and buzzer sound mode.

The Buzzer frequency control register (BFCON) is a register to select output frequencies of buzzer.

Register name	Symbol	Address	Read/Write	Value at system reset
Capture control register	CAPCON	0EH	R/W	0H
Capture register 0	CAPR0	0CH	R	0H
Capture register 1	CAPR1	0DH	R	0H

CAPCON (0EH) (R/W)

b_3	b_2	b_1	b_0
CRF1	CRF0	ECAP1	ECAP0

Selection of capture 1 data latch
- 0: Does not do capture 1 data latch (initial value)
- 1: Does capture 1 data latch

Selection of capture 0 data latch
- 0: Does not do capture 0 data latch (initial value)
- 1: Does capture 0 data latch

Selection of capture 1 enable/disable
- 0: Capture 1 disable (initial value)
- 1: Capture 1 enable

Selection of capture 0 enable/disable
- 0: Capture 0 disable (initial value)
- 1: Capture 0 enable

CAPR0 (0CH) (R)

b_3	b_2	b_1	b_0
32Hz	64Hz	128Hz	256Hz

Values of 32 Hz to 256 Hz of the time base counter

CAPR1 (0DH)
(R)

b_3	b_2	b_1	b_0
32Hz	64Hz	128Hz	256Hz

Values of 32 Hz to 256 Hz of the time base counter

Description

The capture control register (CAPCON) is used to select latch and enable/disable of time base counter output data (32 to 256 Hz) of Capture 0 and Capture 1.

The capture register 0 (CAPR0) and the capture register 1 (CAPR1) are used to read time base counter output latch data of Capture 0 and Capture 1.

Register name	Symbol	Address	Read/Write	Value at system reset
Time base counter register	TBCR	0FH	R/W	0H

TBCR (0FH)
(R/W)

b_3	b_2	b_1	b_0
1Hz	2Hz	4Hz	8Hz

Values of 1 Hz to 8 Hz of the time base counter

Description

The time base counter register (TBCR) outputs the contents of the time base counter when reading. When writing, 8 Hz, 4 Hz, 2 Hz, 1 Hz and 0.1 Hz output of the time base counter are reset to "0".

Register name	Symbol	Address	Read/Write	Value at system reset
Display control register	DSPCON	1EH	R/W	0CH
Display registers 0 to 30	DSPR0 to DSPR30	40H to 5EH	R/W	0H

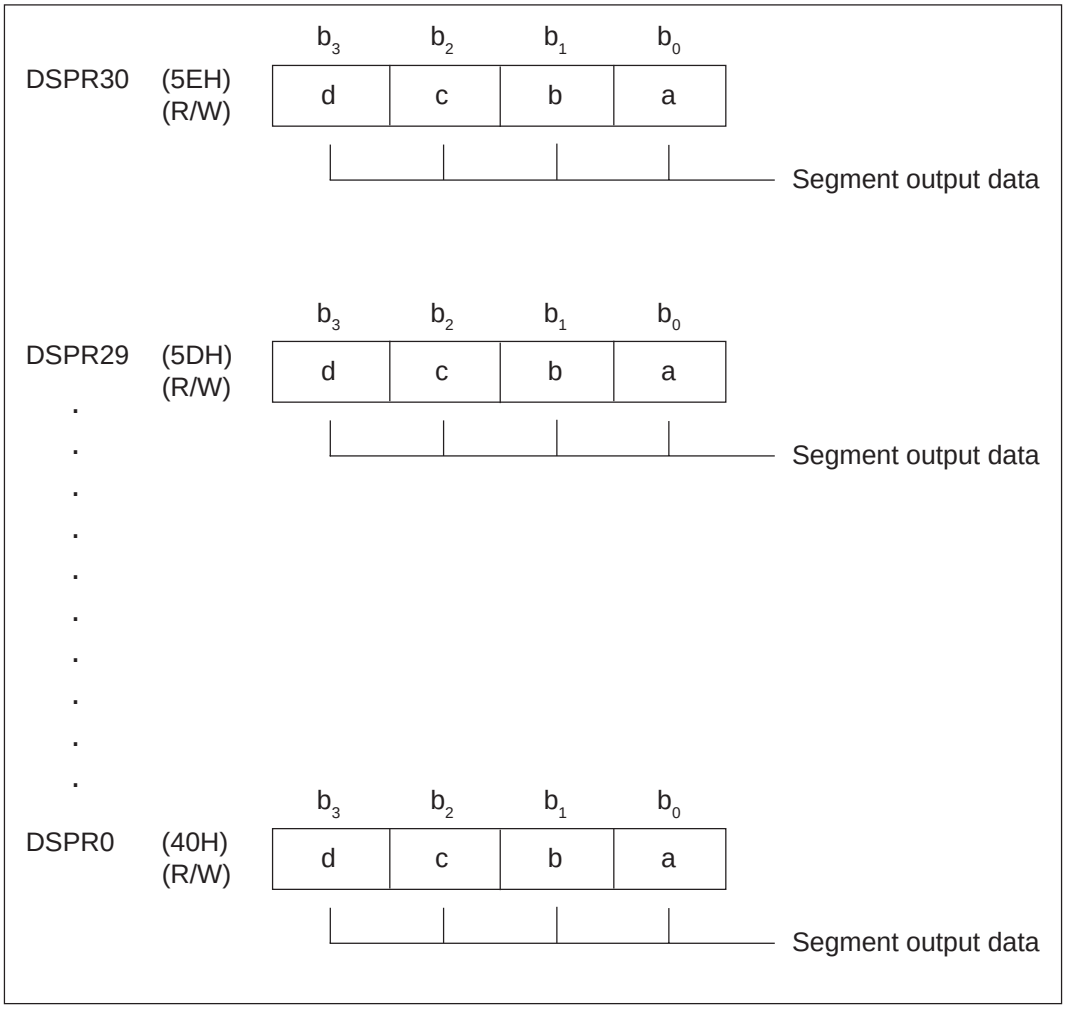
DSPCON (1EH)
(R/W)

b_3	b_2	b_1	b_0
-----*	-----*	DUTY1	DUTY0

Duty selection

b1	b0
0	0: 1/4 duty (initial value)
0	1: 1/3 duty
1	0: 1/2 duty
1	1: Disabled

*Reserved bit: "1" is always read. Not valid for write.



Description

The Display control register (DSPCON) is a register to select duty of the LCD driver.

The Display registers (DSPR0 to 30) are data registers for segment output of the LCD driver and can output to each LCD driver by specifying the mask option of the LCD part.

Register name	Symbol	Address	Read/Write	Value at system reset
A/D converter control register 0	ADCON0	2AH	R/W	0CH
A/D converter control register 1	ADCON1	2BH	R/W	0H
A/D converter counter A register 0	CNTA0	20H	R/W	0H
A/D converter counter A register 1	CNTA1	21H	R/W	0H
A/D converter counter A register 2	CNTA2	22H	R/W	0H
A/D converter counter A register 3	CNTA3	23H	R/W	0H
A/D converter counter A register 4	CNTA4	24H	R/W	8H
A/D converter counter B register 0	CNTB0	26H	R/W	0H
A/D converter counter B register 1	CNTB1	27H	R/W	0H
A/D converter counter B register 2	CNTB2	28H	R/W	0H
A/D converter counter B register 3	CNTB3	29H	R/W	0CH

ADCON0 (2AH) (R/W)

b_3	b_2	b_1	b_0
-----*	-----*	SADI	EADC

Selection of A/D interrupt request

0: Counter A overflow (initial value)
1: Counter B overflow

Selection of A/D conversion start/stop

0: RC oscillation stop (initial value)
1: RC oscillation start

*Reserved bit: "1" is always read out. Not valid for write.

ADCON1 (2BH) (R/W)

b_3	b_2	b_1	b_0
OM3	OM2	OM1	OM0

Selection of oscillation mode

b3	b2	b1	b0
0	0	0	0: IN0 pin external clock input mode (initial value)
0	0	0	1: RS0-CS0 oscillation mode
0	0	1	0: RT0-CS0 oscillation mode
0	0	1	1: RT0-1-CS0 oscillation mode
0	1	0	0: RS0-CT0 oscillation mode
0	1	0	1: RS1-CS1 oscillation mode
0	1	1	0: RT1-CS1 oscillation mode
0	1	1	1: IN1 pin external clock input mode

CNTA0 (20H) (R/W)

b_3	b_2	b_1	b_0
a3	a2	a1	a0

Value of Bits 0 to 3 of Counter A

CNTA1 (21H) (R/W)

b_3	b_2	b_1	b_0
a7	a6	a5	a4

Value of Bits 4 to 7 of Counter A

CNTA2 (22H)
(R/W)

b_3	b_2	b_1	b_0
a11	a10	a9	a8

Value of Bits 8 to 11 of Counter A

CNTA3 (23H)
(R/W)

b_3	b_2	b_1	b_0
a15	a14	a13	a12

Value of Bits 12 to 15 of Counter A

CNTA4 (24H)
(R/W)

b_3	b_2	b_1	b_0
-----*	a18	a17	a16

Value of Bits 16 to 18 of Counter A

*Reserved bit: "1" is always read out. Not valid for write.

CNTB0 (26H)
(R/W)

b_3	b_2	b_1	b_0
b3	b2	b1	b0

Value of Bits 0 to 3 of Counter B

CNTB1 (27H)
(R/W)

b_3	b_2	b_1	b_0
b7	b6	b5	b4

Value of Bits 4 to 7 of Counter B

CNTB2 (28H)
(R/W)

b_3	b_2	b_1	b_0
b11	b10	b9	b8

Value of Bits 8 to 11 of Counter B

CNTB3 (29H)
(R/W)

b_3	b_2	b_1	b_0
-----*	-----*	b13	b12

Value of Bits 12, 13 of Counter B

*Reserved bit: "1" is always read out. Not valid for write.

Description

The A/D converter control register 0 (ADCON0) selects interrupt by overflow of either Counter A or Counter B and selects operation or stop of A/D conversion. The A/D converter control register 1 (ADCON1) is a register to select various RC oscillation modes. The A/D converter counter A registers 0 to 4 (CNTA0 to 4) are registers to read/write the contents of Counter A. The A/D converter counter B registers 0 to 3 (CNTB0 to 3) are registers to read/write the contents of Counter B.

Register name	Symbol	Address	Read/Write	Value at system reset
Watchdog timer control register	WDTCON	36H	W	0H

WDTCON (36H) (W)

b_3	b_2	b_1	b_0
d3	d2	d1	d0

Description

The Watchdog timer control register (WDTCON) is a register to reset the watchdog timer. WDTCON is a write-only register.

Register name	Symbol	Address	Read/Write	Value at system reset
Backup control register	BUPCON	37H	R/W	08H

BUPCON (37H) (R/W)

b_3	b_2	b_1	b_0
-----*	CMPF	ECMP	BUPF

Battery check flag

0: Input voltage level of P0.3 is higher than reference voltage (initial value)
1: Input voltage level of P0.3 is lower than reference voltage

Battery check enable

0: Battery check disabled (initial value)
1: Battery check enabled

V_{DDL} level

0: 1.3 V level (initial value)
1: V_{DD} level

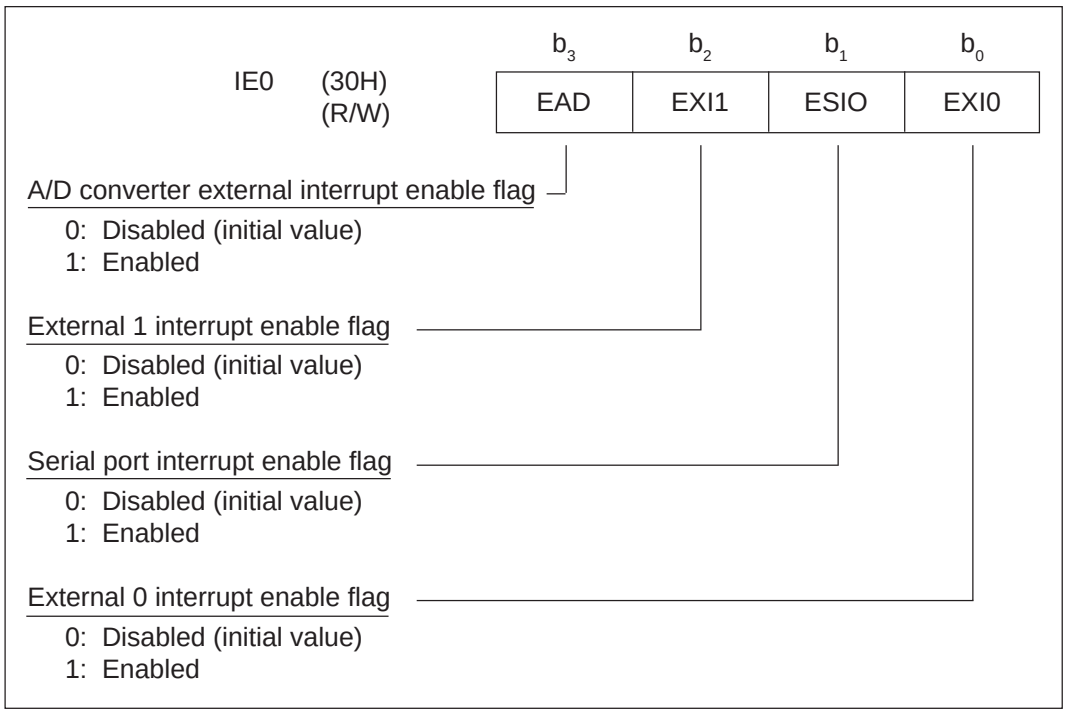
*Reserved bit: "1" is always read out. Not valid for write.7.

Note: The OTP version has different specifications. See Page 17-7.

Description

The Backup control register is a register to select the voltage level of V_{DDL}.

Register name	Symbol	Address	Read/Write	Value at system reset
Interrupt enable register 0	IE0	30H	R/W	0H
Interrupt enable register 1	IE1	31H	R/W	0H
Interrupt enable register 2	IE2	32H	R/W	0EH



IE1 (31H) (R/W)

b_3	b_2	b_1	b_0
E1Hz	E16Hz	E32Hz	E256Hz

1 Hz interrupt enable flag
- 0: Disabled (initial value)
- 1: Enabled

16 Hz interrupt enable flag
- 0: Disabled (initial value)
- 1: Enabled

32 Hz interrupt enable flag
- 0: Disabled (initial value)
- 1: Enabled

256 Hz interrupt enable flag
- 0: Disabled (initial value)
- 1: Enabled

IE2 (32H) (R/W)

b_3	b_2	b_1	b_0
-----*	-----*	-----*	E01Hz

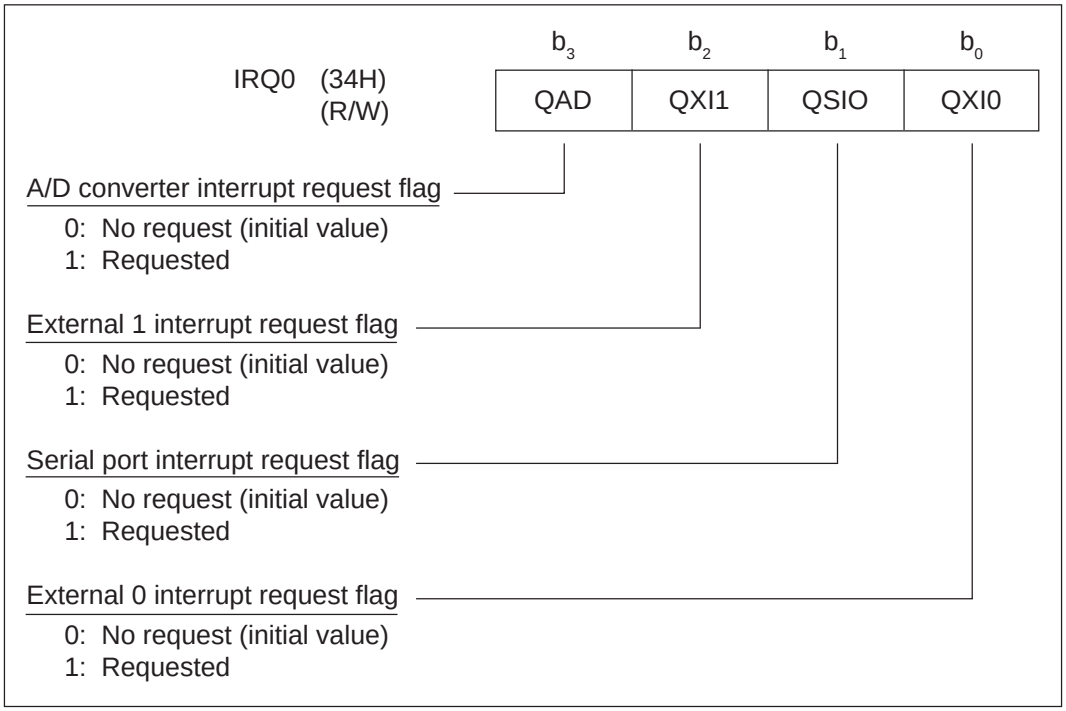
0.1 Hz interrupt enable flag
- 0: Disabled (initial value)
- 1: Enabled

*Reserved bit: "1" is always read out. Not valid for write.

Description

These are registers to set disable/enable of each interrupt.

Register name	Symbol	Address	Read/Write	Value at system reset
Interrupt request register 0	IRQ0	34H	R/W	0H
Interrupt request register 1	IRQ1	35H	R/W	0H
Interrupt request register 2	IRQ2	33H	R/Q	0CH



IRQ1 (35H) (R/W)

b_3	b_2	b_1	b_0
Q1Hz	Q16Hz	Q32Hz	Q256Hz

1 Hz interrupt request flag
- 0: No request (initial value)
- 1: Requested

16 Hz interrupt request flag
- 0: No request (initial value)
- 1: Requested

32 Hz interrupt request flag
- 0: No request (initial value)
- 1: Requested

256 Hz interrupt request flag
- 0: No request (initial value)
- 1: Requested

IRQ2 (33H) (R/W)

b_3	b_2	b_1	b_0
-----*	-----*	QWDT	Q01Hz

Watchdog timer interrupt request flag
- 0: No request (initial value)
- 1: Requested

0.1 Hz interrupt request flag
- 0: No request (initial value)
- 1: Requested

*Reserved bit: "1" is always read out. Not valid for write.

Description

These bits are set by each interrupt request. When interrupt is enabled by IE0, IE1 and IE2, the CPU receives interrupts only when the master interrupt enable flag (MI) is set to "1" and the execution is advanced to the vector address of each interrupt. The watchdog timer interrupt does not have interrupt mask functions by the IE register and the MI flag.

Register name	Symbol	Address	Read/Write	Value at system reset
Master interrupt enable register	MIEF	7CH	R/W	0EH

MIEF (7CH) (R/W)

b_3	b_2	b_1	b_0
-----*	-----*	-----*	MI

Master interrupt enable flag

0: Interrupt disabled (initial value)
1: Interrupt enabled

*Reserved bit: "1" is always read out. Not valid for write.

Description

When MI is set to "1", interrupt is enabled and interrupts by the interrupt enable registers (IE0, IE1 and IE2) and the interrupt request registers (IRQ0, IRQ1 and IRQ2) are received by the CPU.

Register name	Symbol	Address	Read/Write	Value at system reset
Halt mode register	HALT	7DH	R/W	0EH

HALT (7DH) (R/W)

b_3	b_2	b_1	b_0
-----*	-----*	-----*	HLT

Halt mode transition selection flag

0: Normal operation (initial value)
1: Halt mode

*Reserved bit: "1" is always read out. Not valid for write.

Description

A flag to enter halt mode. When the HLT flag is set to "1", the CPU enters halt mode at the first machine cycle of the next instruction.

Register name	Symbol	Address	Read/Write	Value at system reset
Stack pointer	SP	7EH	R/W	0FFH

SP (7EH) (R/W)

b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
-----*	SP6	SP5	SP4	SP3	SP2	SP1	-----*

Contents of the stack pointer

*Reserved bit: "1" is always read out. Not valid for write.

Description

This is a pointer to indicate a stack address. At reset, it becomes "0FFH" and addresses 0FFH and 0FEH on the data memory of Bank 7 are selected.

An access to the stack pointer is valid only for byte access instructions as 8-bit transfer instructions and 8-bit arithmetic instructions.

Appendix C:

Package Dimension Diagrams and Pad Coordinates

ML64168-xxxGP

(Unit: mm)

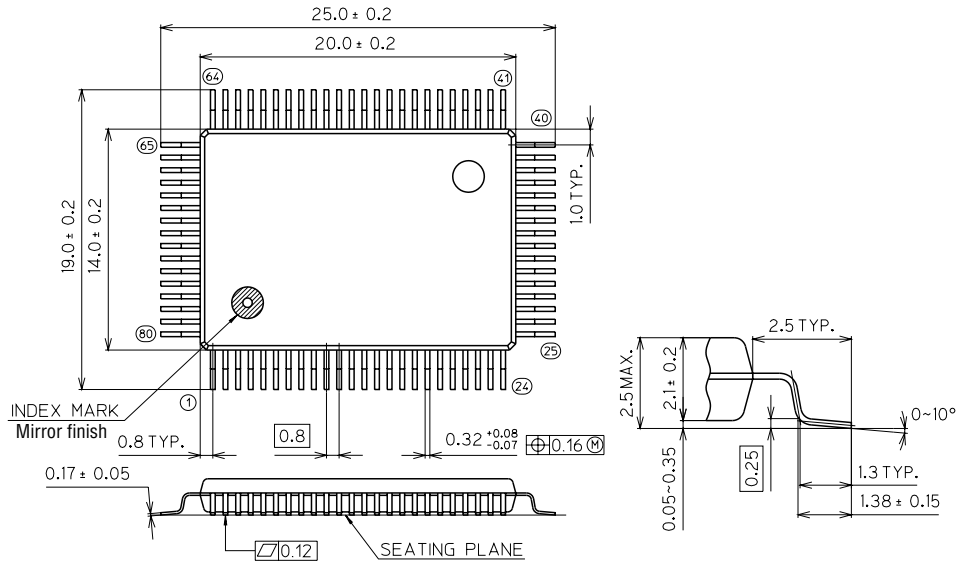


Figure C-1 80-Pin QFP: GP Package Dimension Diagram

ML64168-xxxGA

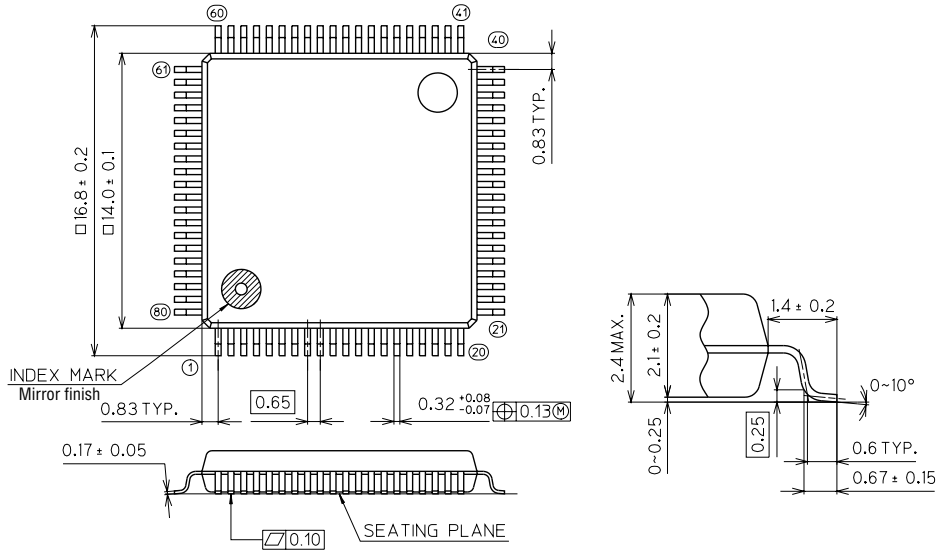


Figure C-2 80-Pin QFP: GA Package Dimension Diagram

ML64168-xxxTB

(Unit: mm)

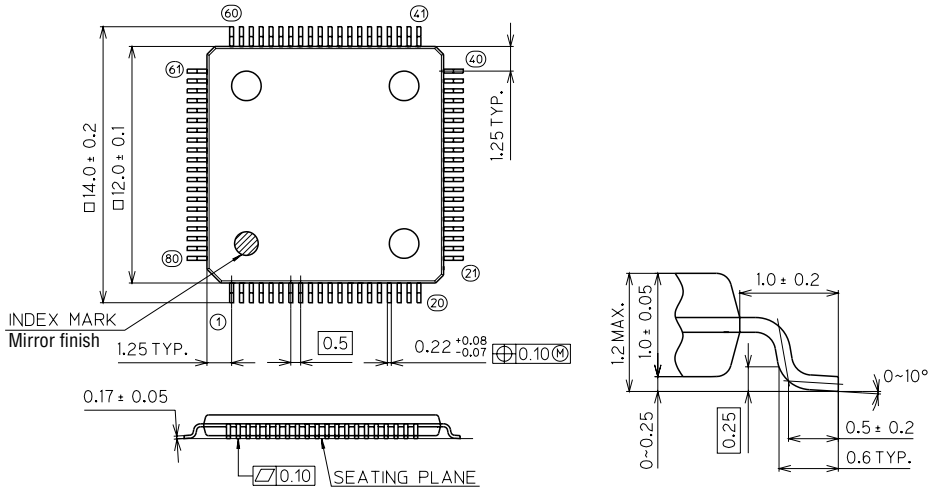


Figure C-3 80-Pin TQFP: TB Package Dimension Diagram

Table C-1 Pad Coordinates

ML64168-xxx

Center of chip : x = 0, y = 0

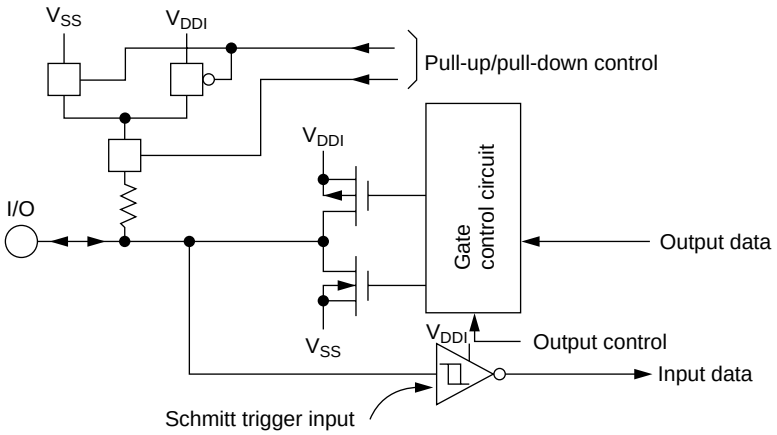
Pad No.	Pad Name	X (µm)	Y (µm)	Pad No.	Pad Name	X (µm)	Y (µm)
1	L2	–2115.0	–2555.0	41	V_{DDI}	2110.0	2555.0
2	L3	–1843.5	–2555.0	42	V_{DD2}	1845.0	2555.0
3	L4	–1575.0	–2555.0	43	V_{DD3}	1575.0	2555.0
4	L5	–1365.0	–2555.0	44	C1	1365.0	2555.0
5	L6	–1155.0	–2555.0	45	C2	1155.0	2555.0
6	L7	–945.0	–2555.0	46	L17	945.0	2555.0
7	L8	–735.0	–2555.0	47	L18	765.0	2555.0
8	L9	–525.0	–2555.0	48	L19	585.0	2555.0
9	L10	–315.0	–2555.0	49	L20	405.0	2555.0
10	L11	–105.0	–2555.0	50	L21	225.0	2555.0
11	L12	105.0	–2555.0	51	L22	45.0	2555.0
12	L13	315.0	–2555.0	52	L23	–135.0	2555.0
13	L14	525.0	–2555.0	53	L24	–315.0	2555.0
14	L15	735.0	–2555.0	54	L25	–667.0	2508.0
15	L16	945.0	–2555.0	55	L26	–987.0	2508.0
16	P2.0	1155.0	–2555.0	56	L27	–1307.0	2508.0
17	P2.1	1365.0	–2555.0	57	L28	–1487.0	2508.0
18	P2.2	1575.0	–2555.0	58	L29	–1697.0	2508.0
19	P2.3	1819.5	–2555.0	59	L30	–1907.0	2508.0
20	P3.0	2110.0	–2555.0	60	L31	–2117.0	2508.0
21	P3.1	2390.0	–2285.0	61	L32	–2390.0	2285.0
22	P3.2	2390.0	–2005.0	62	L33	–2390.0	2005.0
23	P3.3	2390.0	–1725.0	63	OSC2	–2390.0	1725.0
24	P4.0	2390.0	–1495.0	64	OSC1	–2390.0	1495.0
25	P4.1	2390.0	–1265.0	65	V_{DD}	–2390.0	1265.0
26	P4.2	2390.0	–1035.0	66	$\overline{XT}$	–2390.0	1035.0
27	P4.3	2390.0	–805.0	67	XT	–2390.0	805.0
28	BD	2390.0	–575.0	68	$\overline{RESET}$	–2390.0	575.0
29	V_{DDL}	2390.0	–345.0	69	$\overline{TST1}$	–2390.0	345.0
30	V_{SS}	2390.0	–115.0	70	$\overline{TST2}$	–2390.0	115.0
31	RT0	2390.0	115.0	71	P1.0	–2390.0	–115.0
32	CRT0	2390.0	345.0	72	P1.1	–2390.0	–345.0
33	RS0	2390.0	575.0	73	P1.2	–2390.0	–575.0
34	CS0	2390.0	805.0	74	P1.3	–2390.0	–805.0
35	IN0	2390.0	1035.0	75	P0.0	–2390.0	–1035.0
36	IN1	2390.0	1265.0	76	P0.1	–2390.0	–1265.0
37	CS1	2390.0	1495.0	77	P0.2	–2390.0	–1495.0
38	RS1	2390.0	1725.0	78	P0.3	–2390.0	–1725.0
39	RT1	2390.0	2005.0	79	L0	–2390.0	–2005.0
40	V_{DD1}	2390.0	2285.0	80	L1	–2390.0	–2285.0

Bonding pad size : 110 µm × 110 µm

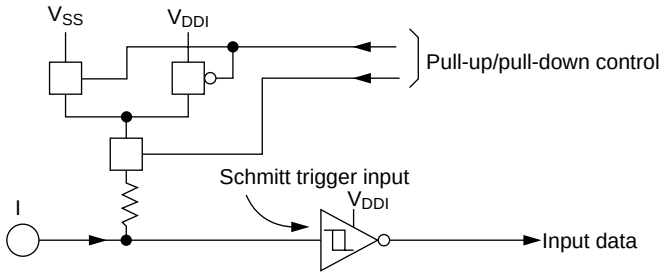
Appendix D:

Layout of Input/Output Circuits

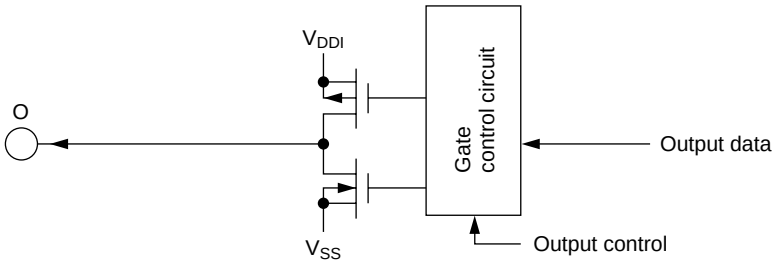
A. Input/output ports (P2.0 to P2.3, P3.0 to P3.3, P4.0 to P4.3)



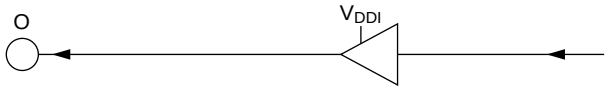
B. Input ports (P0.0 to P0.3)



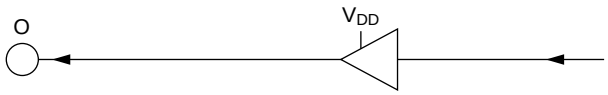
C. Output ports (P1.0 to P1.3)



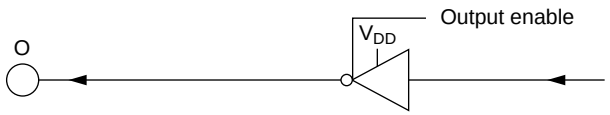
D. Output port (L26/P5.0 to L29/P5.3, L30/P6.0 to L33/P6.3 pins at the mask option)



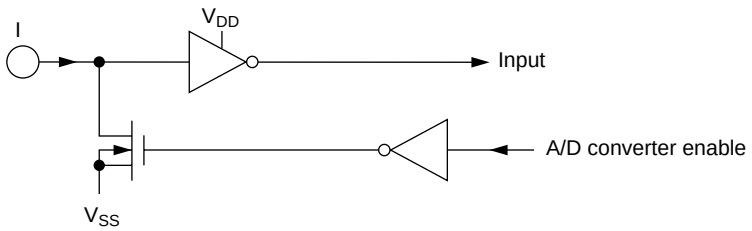
E. BD and CS1 outputs



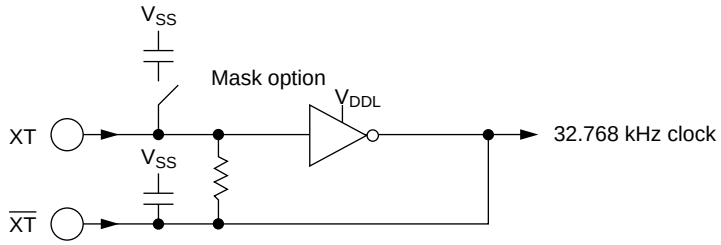
F. RS0, RS1, RT0, RT1, CS0 and CRT0 outputs



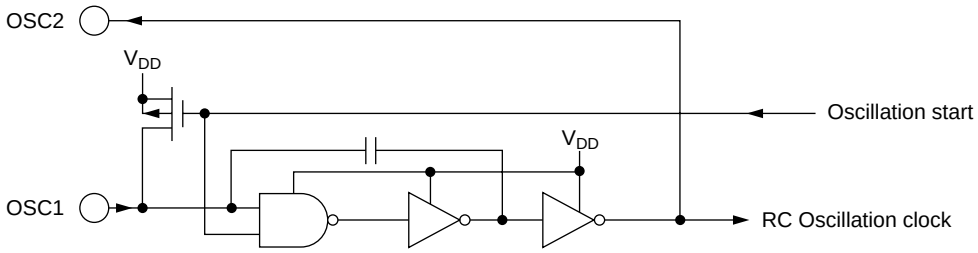
G. IN0 and IN1 inputs



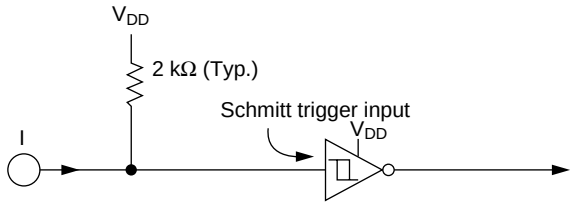
H. Crystal oscillation circuit



I. 400 kHz RC oscillation circuit



J. $\overline{RESET}$, $\overline{TST1}$, and $\overline{TST2}$ inputs



Appendix E:

Examples of Application Circuits

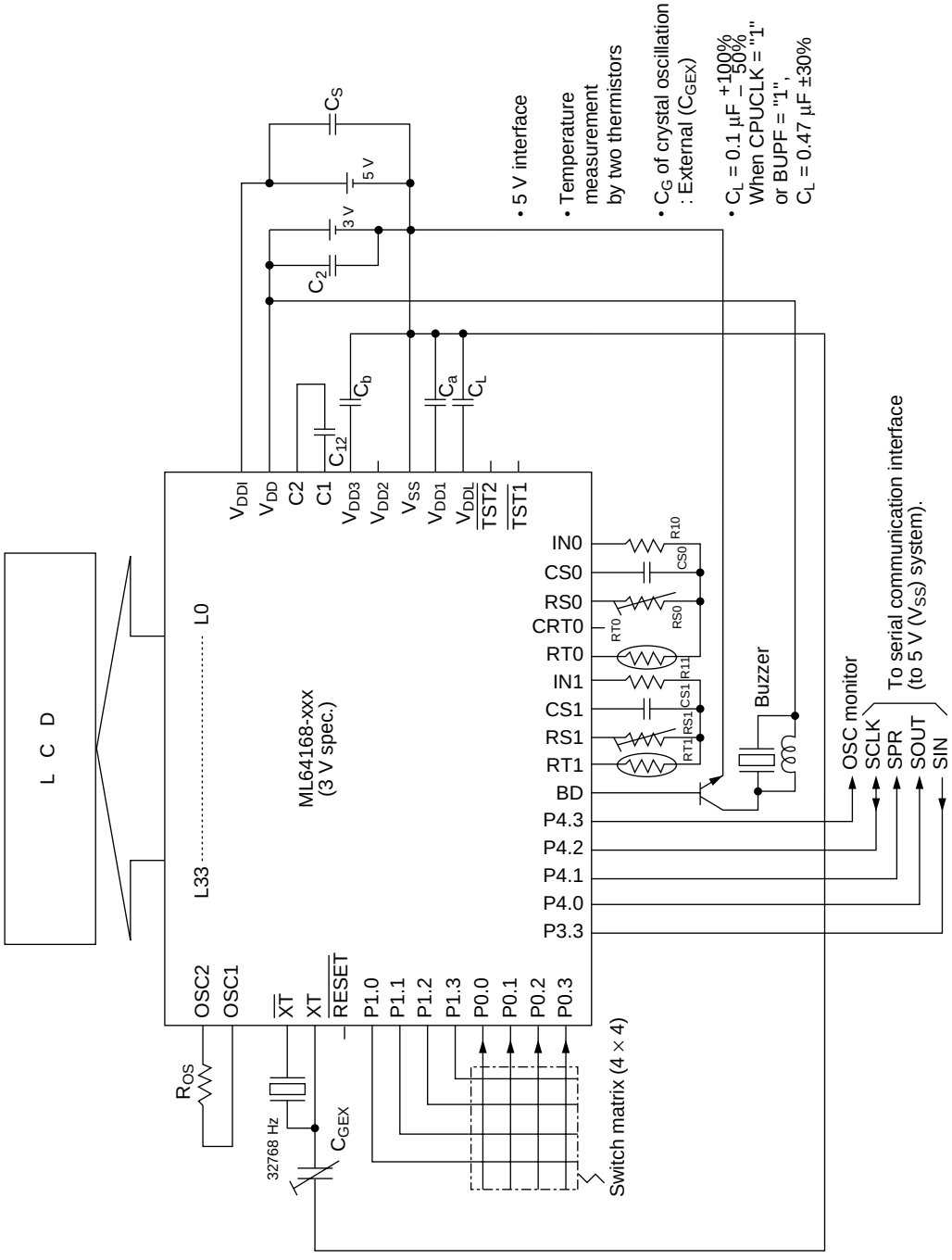


Figure E-1 Example of 3 V Spec. Applied Circuit

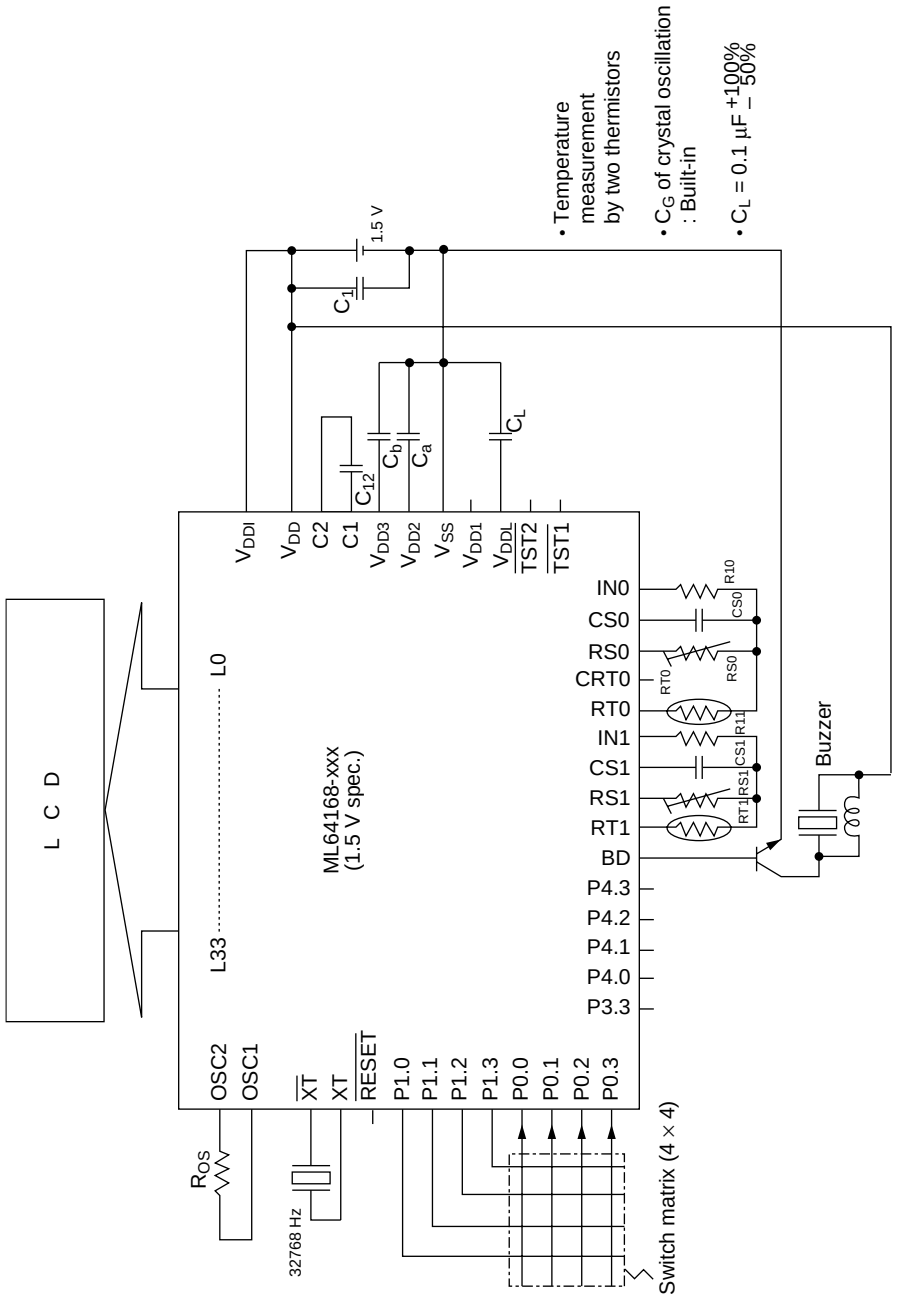


Figure E-2 Example of 1.5 V Spec. Applied Circuit

Appendix F:

Mask Options

● Table of power supply voltage and C_G selection mask options

Item	Mask specification	Selection
Power supply voltage	1.5 V	
	3.0 V	
C_G of crystal oscillator	Built-in	
	External	
LCD-VR	Used	
	Not used	

● Table of LCD driver mask options

[Description of LCD driver mask options]

SEG LCD driver pin name

SIGNAL Write the name of each segment corresponding each common signal.

C/S/P Indicates whether L0 to L33 of the LCD driver are selected as segment driver or common driver or output port. When selected as segment driver, "S" is written. When selected as common driver, "C" is written and when used as output port,"P" is written. When not used, blank is written.

DATA Writes the bit name of the display register corresponding to the signal name (a to d).

DSPR Writes the number of the display register (0 to 30). When not used, blank is written.

Notes:

(1) There is no need to use all 0 to 30 of the display registers.

(2) The same name (i.e. the same display register number and the same bit name) can be used for 2 or more segments.

(3) When "P" is selected, DSPR becomes either "0" or "1". DATA and DSPR are assigned to COM1 when "P" is selected. Selection of "P" is possible only for the LCD drivers of L26 to L33.

(4) To make a table of the mask options, use the MASK164 mask option generator. For details of input, refer to "MASK164 Mask Option Generator User's Manual".

(5) When the display registers are used as the data register and flag, not for indication, the display registers must be assigned per bit by using the empty segments in the LCD driver mask option table.
When the empty segments do not exist on the LCD driver mask option table, the display register cannot be used as the data register and flag.

[Example of how to make a LCD driver mask options]

(1) When L0 is assigned to Common 2, L1 to segment and L2 as unused (1/4 duty)

SEG	SIGNAL	C/S/P	COM1		COM2		COM3		COM4	
			DATA	DSPR	DATA	DSPR	DATA	DSPR	DATA	DSPR
L0	/ COM2 / /	C								
L1	ALARM / MODE / 4f / 4g	S	b	5	d	6	b	14	c	14
L2	/ / /									

(2) When L27 is assigned to Common 1, L28 to segment and L29 as an output port (1/4 duty)

SEG	SIGNAL	C/S/P	COM1		COM2		COM3		COM4	
			DATA	DSPR	DATA	DSPR	DATA	DSPR	DATA	DSPR
L27	COM1 / / /	C								
L28	1a / 1b / 1c / DP1	S	a	2	b	2	c	2	d	2
L29	OUT / / /	P	a	0						

Table of LCD Driver Mask Options (1/4 duty)

SEG	SIGNAL	C/S/P	COM1		COM2		COM3		COM4	
			DATA	DSPR	DATA	DSPR	DATA	DSPR	DATA	DSPR
L0	/ / /									
L1	/ / /									
L2	/ / /									
L3	/ / /									
L4	/ / /									
L5	/ / /									
L6	/ / /									
L7	/ / /									
L8	/ / /									
L9	/ / /									
L10	/ / /									
L11	/ / /									
L12	/ / /									
L13	/ / /									
L14	/ / /									
L15	/ / /									
L16	/ / /									
L17	/ / /									
L18	/ / /									
L19	/ / /									
L20	/ / /									
L21	/ / /									

Table of LCD Driver Mask Options (1/4 duty) (continued)

SEG	SIGNAL	C/S/P	COM1		COM2		COM3		COM4	
			DATA	DSPR	DATA	DSPR	DATA	DSPR	DATA	DSPR
L22	/ / /									
L23	/ / /									
L24	/ / /									
L25	/ / /									
L26	/ / /									
L27	/ / /									
L28	/ / /									
L29	/ / /									
L30	/ / /									
L31	/ / /									
L32	/ / /									
L33	/ / /									

Table of LCD Driver Mask Options (1/3 duty)

SEG	SIGNAL	C/S/P	COM1		COM2		COM3	
			DATA	DSPR	DATA	DSPR	DATA	DSPR
L0	/ /							
L1	/ /							
L2	/ /							
L3	/ /							
L4	/ /							
L5	/ /							
L6	/ /							
L7	/ /							
L8	/ /							
L9	/ /							
L10	/ /							
L11	/ /							
L12	/ /							
L13	/ /							
L14	/ /							
L15	/ /							
L16	/ /							
L17	/ /							
L18	/ /							
L19	/ /							
L20	/ /							
L21	/ /							

Table of LCD Driver Mask Options (1/3 duty) (continued)

SEG	SIGNAL	C/S/P	COM1		COM2		COM3	
			DATA	DSPR	DATA	DSPR	DATA	DSPR
L22	/ /							
L23	/ /							
L24	/ /							
L25	/ /							
L26	/ /							
L27	/ /							
L28	/ /							
L29	/ /							
L30	/ /							
L31	/ /							
L32	/ /							
L33	/ /							

Table of LCD Driver Mask Options (1/2 duty)

SEG	SIGNAL	C/S/P	COM1		COM2	
			DATA	DSPR	DATA	DSPR
L0	/					
L1	/					
L2	/					
L3	/					
L4	/					
L5	/					
L6	/					
L7	/					
L8	/					
L9	/					
L10	/					
L11	/					
L12	/					
L13	/					
L14	/					
L15	/					
L16	/					
L17	/					
L18	/					
L19	/					
L20	/					
L21	/					

Table of LCD Driver Mask Options (1/2 duty) (continued)

SEG	SIGNAL	C/S/P	COM1		COM2	
			DATA	DSPR	DATA	DSPR
L22	/					
L23	/					
L24	/					
L25	/					
L26	/					
L27	/					
L28	/					
L29	/					
L30	/					
L31	/					
L32	/					
L33	/					

[ML64P168]

Appendix G:

Package Dimension Diagrams

ML64P168-xxxGA

(Unit: mm)

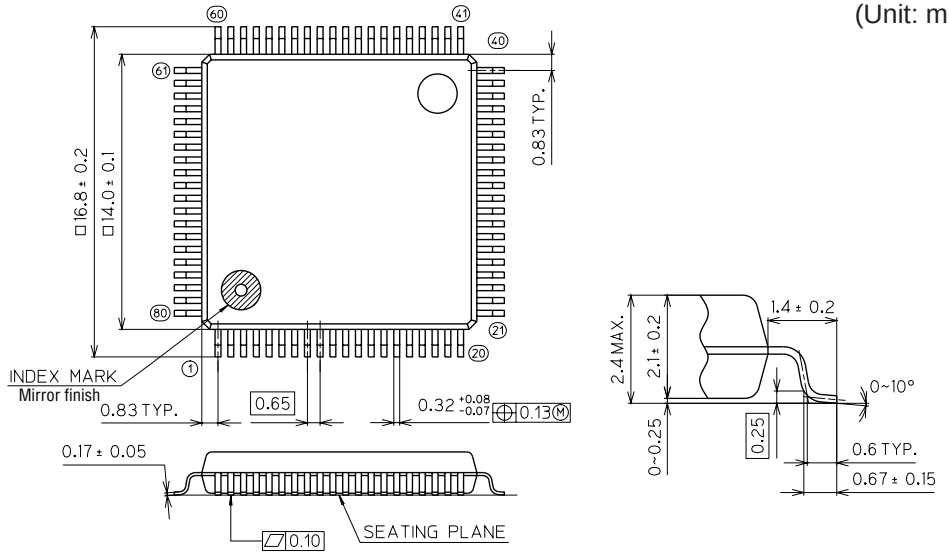


Figure G-1 80-Pin QFP: GA Package Dimension Diagram

ML64P168-xxxGP

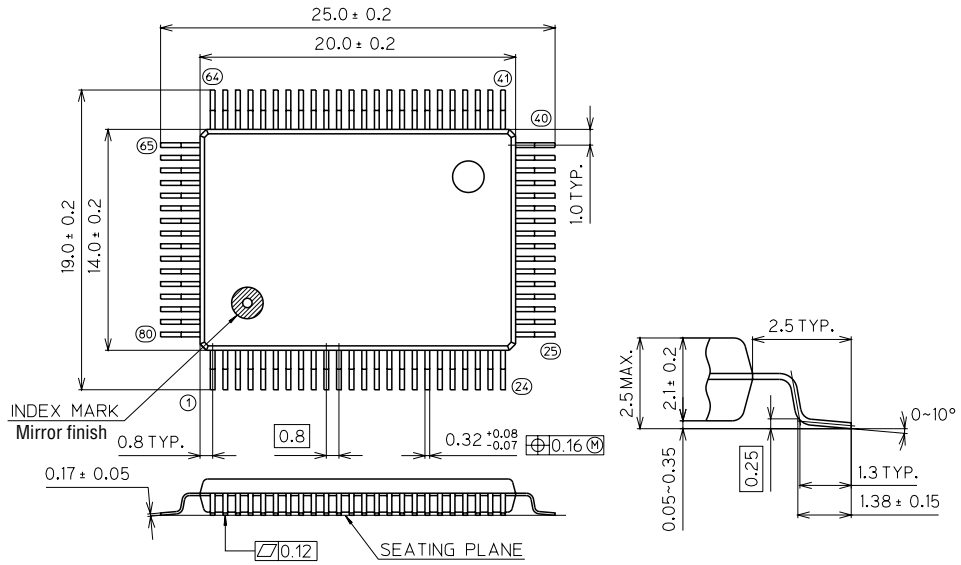


Figure G-2 80-Pin QFP: GP Package Dimension Diagram

Appendix H:

Examples of Application Circuits

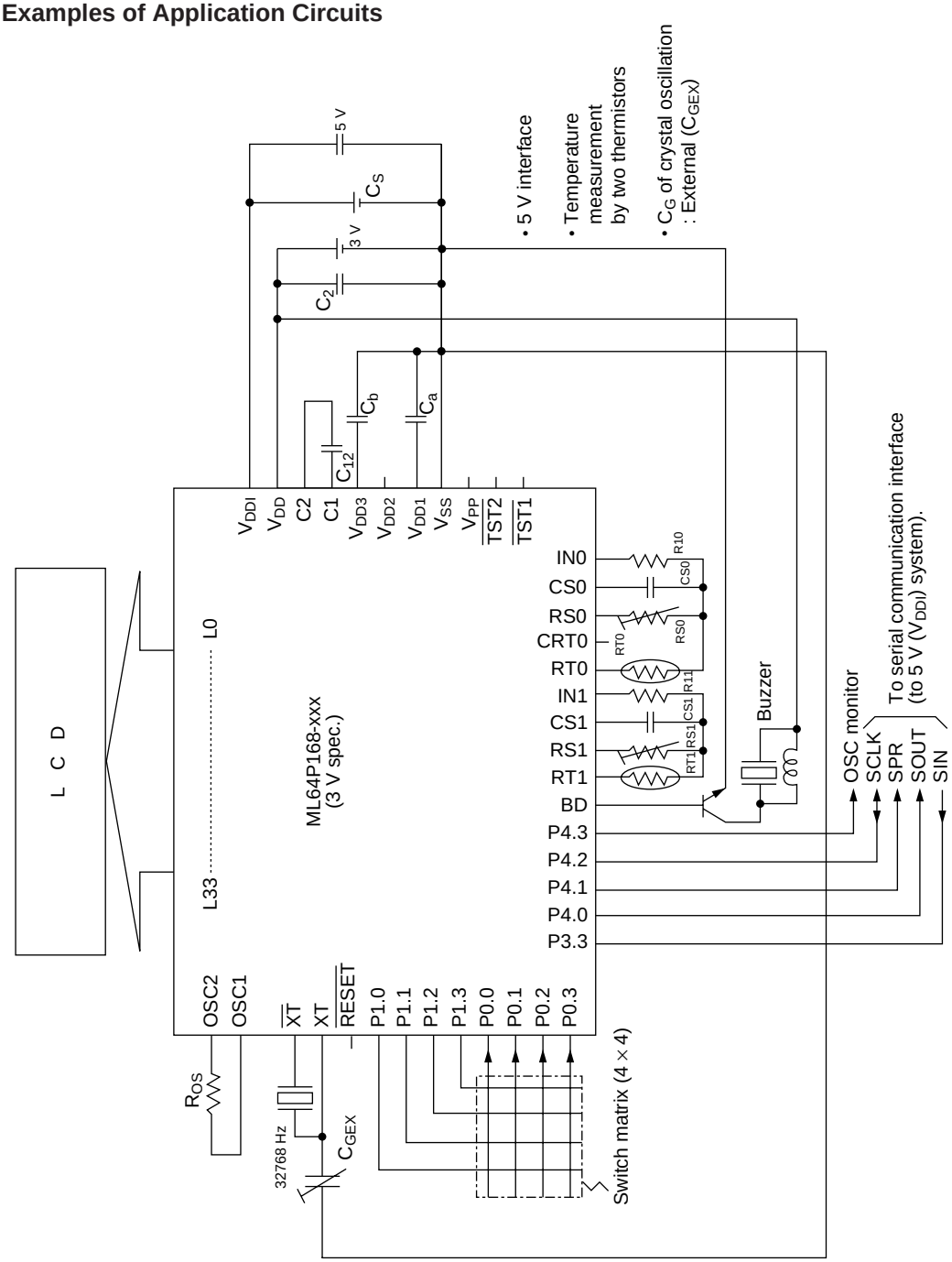


Figure H-1 Example of 3 V Spec. Applied Circuit

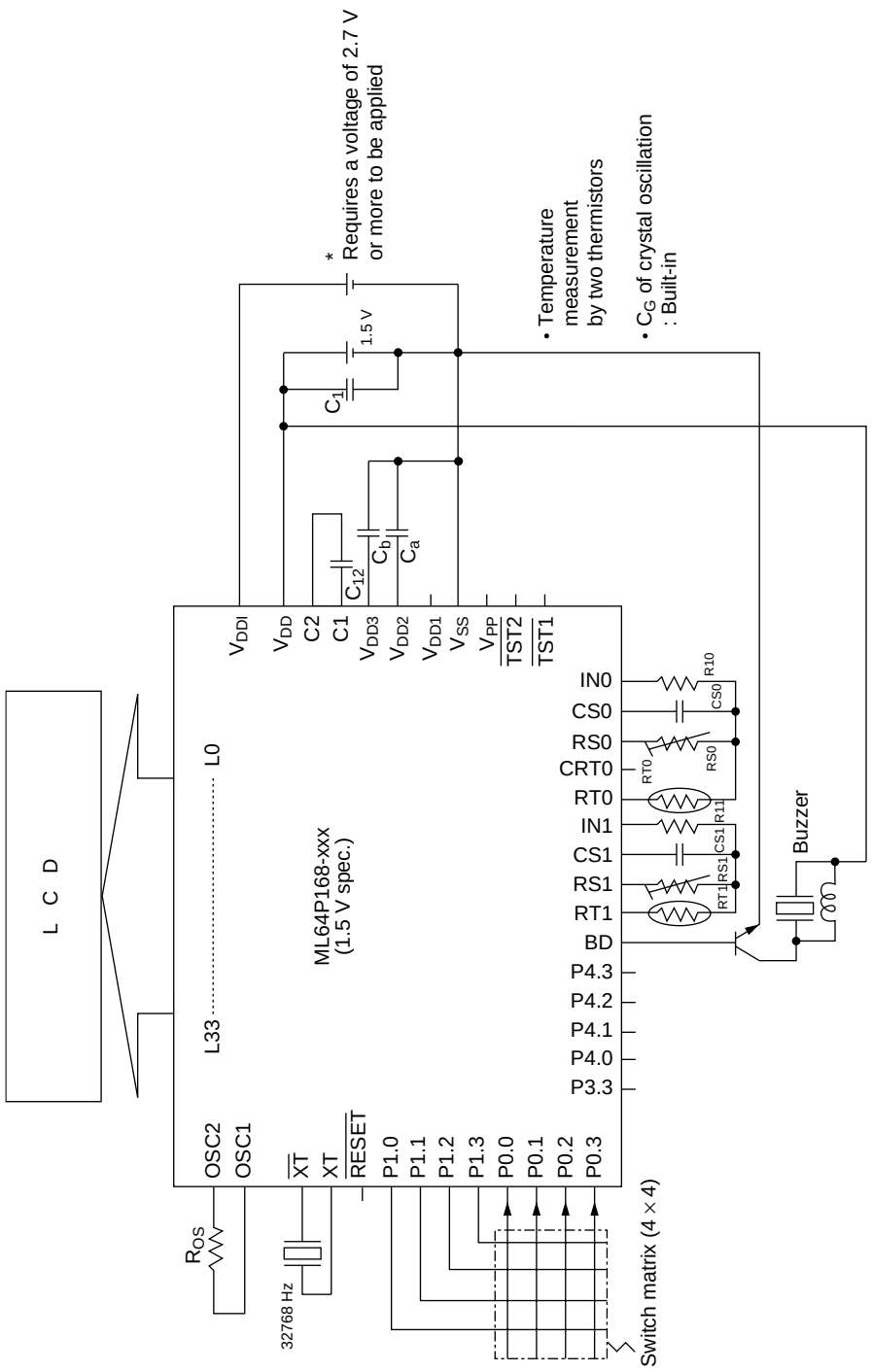


Figure H-2 Example of 1.5 V Spec. Applied Circuit

Appendix I:

Mask Options

For the method of setting mask options, see "Appendix F (ML64168)" because it is the same as the mask ROM chip.

Oki provides standard mask option products provided for the OTP version. To each of their product names is added a code number for identification, as shown in the Table below.

Table I-1 Line-up of Standard Mask Option Products

Code No.	Power supply voltage	Built-in C_G	LCD-VR	LCD allocation
001	1.5 V	No	No	See Mask Option Allocation Table 1.
002	3 V	Yes	No	See Mask Option Allocation Table 1.
003	1.5 V	No	Yes	See Mask Option Allocation Table 2.
004	3 V	Yes	Yes	See Mask Option Allocation Table 2.

- LCD Driver Mask Option Allocation Table 1 (1/4 duty)

SEG	SIGNAL				C/S/P	COM1		COM2		COM3		COM4	
						DATA	DSPR	DATA	DSPR	DATA	DSPR	DATA	DSPR
L0	COM1	/	/	/	C	—	—	—	—	—	—	—	—
L1		/COM2	/	/	C	—	—	—	—	—	—	—	—
L2		/	COM3	/	C	—	—	—	—	—	—	—	—
L3		/	/	/COM4	C	—	—	—	—	—	—	—	—
L4	SG1	/SG2	/SG3	/SG4	S	a	0	b	0	c	0	d	0
L5	SG5	/SG6	/SG7	/SG8	S	a	1	b	1	c	1	d	1
L6	SG9	/SG10	/SG11	/SG12	S	a	2	b	2	c	2	d	2
L7	SG13	/SG14	/SG15	/SG16	S	a	3	b	3	c	3	d	3
L8	SG17	/SG18	/SG19	/SG20	S	a	4	b	4	c	4	d	4
L9	SG21	/SG22	/SG23	/SG24	S	a	5	b	5	c	5	d	5
L10	SG25	/SG26	/SG27	/SG28	S	a	6	b	6	c	6	d	6
L11	SG29	/SG30	/SG31	/SG32	S	a	7	b	7	c	7	d	7
L12	SG33	/SG34	/SG35	/SG36	S	a	8	b	8	c	8	d	8
L13	SG37	/SG38	/SG39	/SG40	S	a	9	b	9	c	9	d	9
L14	SG41	/SG42	/SG43	/SG44	S	a	10	b	10	c	10	d	10
L15	SG45	/SG46	/SG47	/SG48	S	a	11	b	11	c	11	d	11
L16	SG49	/SG50	/SG51	/SG52	S	a	12	b	12	c	12	d	12
L17	SG53	/SG54	/SG55	/SG56	S	a	13	b	13	c	13	d	13
L18	SG57	/SG58	/SG59	/SG60	S	a	14	b	14	c	14	d	14
L19	SG61	/SG62	/SG63	/SG64	S	a	15	b	15	c	15	d	15
L20	SG65	/SG66	/SG67	/SG68	S	a	16	b	16	c	16	d	16
L21	SG69	/SG70	/SG71	/SG72	S	a	17	b	17	c	17	d	17
L22	SG73	/SG74	/SG75	/SG76	S	a	18	b	18	c	18	d	18
L23	SG77	/SG78	/SG79	/SG80	S	a	19	b	19	c	19	d	19
L24	SG81	/SG82	/SG83	/SG84	S	a	20	b	20	c	20	d	20
L25	SG85	/SG86	/SG87	/SG88	S	a	21	b	21	c	21	d	21
L26	SG89	/SG90	/SG91	/SG92	S	a	22	b	22	c	22	d	22
L27	SG93	/SG94	/SG95	/SG96	S	a	23	b	23	c	23	d	23
L28	SG97	/SG98	/SG99	/SG100	S	a	24	b	24	c	24	d	24
L29	SG101	/SG102	/SG103	/SG104	S	a	25	b	25	c	25	d	25
L30	SG105	/SG106	/SG107	/SG108	S	a	26	b	26	c	26	d	26
L31	SG109	/SG110	/SG111	/SG112	S	a	27	b	27	c	27	d	27
L32	SG113	/SG114	/SG115	/SG116	S	a	28	b	28	c	28	d	28
L33	SG117	/SG118	/SG119	/SG120	S	a	29	b	29	c	29	d	29

- LCD Driver Mask Option Allocation Table 2 (1/4 duty)

SEG	SIGNAL				C/S/P	COM1		COM2		COM3		COM4	
						DATA	DSPR	DATA	DSPR	DATA	DSPR	DATA	DSPR
L0	COM1	/	/	/	C	—	—	—	—	—	—	—	—
L1		/COM2	/	/	C	—	—	—	—	—	—	—	—
L2		/	COM3	/	C	—	—	—	—	—	—	—	—
L3		/	/	/COM4	C	—	—	—	—	—	—	—	—
L4	SG1	/SG2	/SG3	/SG4	S	a	2	b	2	c	2	d	2
L5	SG5	/SG6	/SG7	/SG8	S	a	3	b	3	c	3	d	3
L6	SG9	/SG10	/SG11	/SG12	S	a	4	b	4	c	4	d	4
L7	SG13	/SG14	/SG15	/SG16	S	a	5	b	5	c	5	d	5
L8	SG17	/SG18	/SG19	/SG20	S	a	6	b	6	c	6	d	6
L9	SG21	/SG22	/SG23	/SG24	S	a	7	b	7	c	7	d	7
L10	SG25	/SG26	/SG27	/SG28	S	a	8	b	8	c	8	d	8
L11	SG29	/SG30	/SG31	/SG32	S	a	9	b	9	c	9	d	9
L12	SG33	/SG34	/SG35	/SG36	S	a	10	b	10	c	10	d	10
L13	SG37	/SG38	/SG39	/SG40	S	a	11	b	11	c	11	d	11
L14	SG41	/SG42	/SG43	/SG44	S	a	12	b	12	c	12	d	12
L15	SG45	/SG46	/SG47	/SG48	S	a	13	b	13	c	13	d	13
L16	SG49	/SG50	/SG51	/SG52	S	a	14	b	14	c	14	d	14
L17	SG53	/SG54	/SG55	/SG56	S	a	15	b	15	c	15	d	15
L18	SG57	/SG58	/SG59	/SG60	S	a	16	b	16	c	16	d	16
L19	SG61	/SG62	/SG63	/SG64	S	a	17	b	17	c	17	d	17
L20	SG65	/SG66	/SG67	/SG68	S	a	18	b	18	c	18	d	18
L21	SG69	/SG70	/SG71	/SG72	S	a	19	b	19	c	19	d	19
L22	SG73	/SG74	/SG75	/SG76	S	a	20	b	20	c	20	d	20
L23	SG77	/SG78	/SG79	/SG80	S	a	21	b	21	c	21	d	21
L24	SG81	/SG82	/SG83	/SG84	S	a	22	b	22	c	22	d	22
L25	SG85	/SG86	/SG87	/SG88	S	a	23	b	23	c	23	d	23
L26	P0	/	/	/	P	a	0	—	—	—	—	—	—
L27	P1	/	/	/	P	b	0	—	—	—	—	—	—
L28	P2	/	/	/	P	c	0	—	—	—	—	—	—
L29	P3	/	/	/	P	d	0	—	—	—	—	—	—
L30	P4	/	/	/	P	a	1	—	—	—	—	—	—
L31	P5	/	/	/	P	b	1	—	—	—	—	—	—
L32	P6	/	/	/	P	c	1	—	—	—	—	—	—
L33	P7	/	/	/	P	d	1	—	—	—	—	—	—

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User's Manual

First Edition: February 1999
Second Edition: June 1999
Third Edition: September 1999

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