



MICRF221

3.3V, QwikRadio® 850 MHz to 950 MHz Receiver

General Description

The MICRF221 is a third generation QwikRadio® receiver, offering all the benefits of Micrel's earlier QwikRadio® products with significant improvements, including: enhanced sensitivity, automatic duty-cycle feature and RSSI output.

The MICRF221, Figure 1, is a super-heterodyne receiver, designed for OOK and ASK modulation. The down-conversion mixer also provides image rejection.

The MICRF221 receiver provides a SLEEP Mode for duty-cycle operation and an enhanced, customer programmable "WAKE" function. These features are further combined into a wholly integrated "self-polling" scheme that is ideal for low and ultra-low power applications, such as RKE and RFID

All post-detection data filtering is provided on the MICRF221 receiver. Any one of four filter bandwidths may be selected externally by the user in binary steps, from 1.25 kHz to 10 kHz. The user needs only to program the device with a set of easily determined values based on data rate, code modulation format, and desired duty-cycle operation.

Features

- Complete Receiver on a Chip
- -109dBm sensitivity, 1 kbps and BER 10E-02
- Image Rejection Mixer
- 850 MHz to 950 MHz frequency range
- Low Power, 9mA @ 868 MHz, continuous on
- Data Rates to 10kbps (Manchester Encoded)
- Auto polling (sleep mode, current < 0.1 mA)
- Analog RSSI Output
- Programmable "Low Sensitivity" mode
- No IF filter required
- Excellent selectivity and noise rejection
- Low external part count
- Additional Functions Programmed through serial interface

Ordering Information

Part Number	Temperature Range	Package
MICRF221AYQS	-40° to +105°C	16-Pin QSOP

Typical Application

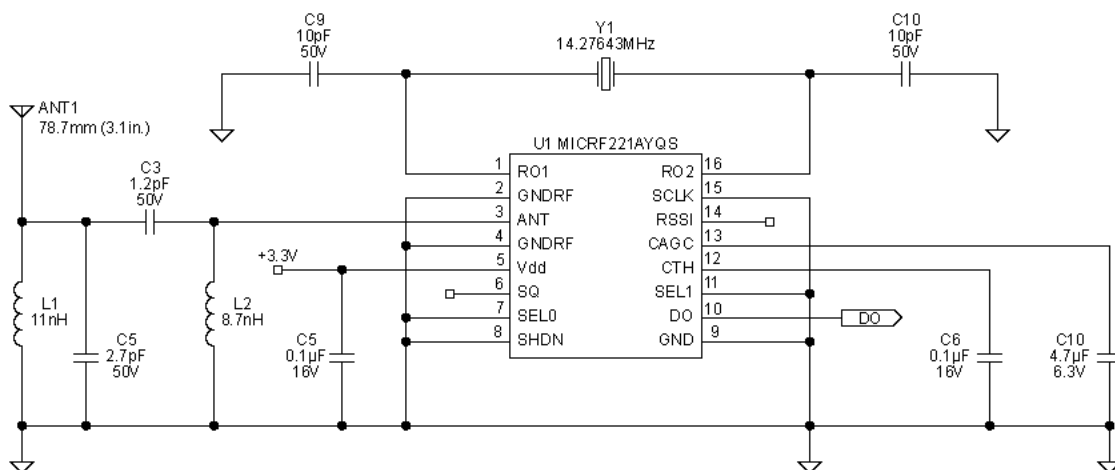


Figure 1: MICRF221 Receiver 915.0 MHz, 1kHz Baud Rate Example

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Pin Configuration

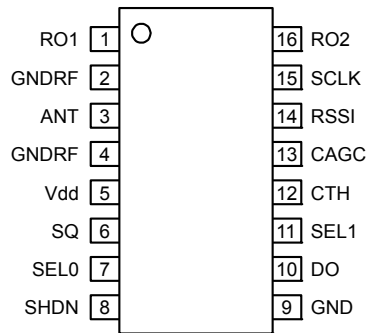


Figure 2. MICRF221AYQS Pin Configuration

Pin Description

16-Pin QSOP	Pin Name	Pin Function
1	RO1	Reference Oscillator (input): Reference resonator input connection to pierce oscillator stage. May also be driven by external reference signal of 1.5V p-p amplitude maximum. 7pF to GND during normal operation.
2	GNDRF	Negative supply connection associated with ANT RF input.
3	ANT	Antenna (input): RF signal input from antenna. Internally AC coupled. It is recommended a matching network with an inductor-to-RF ground be used to improve ESD protection.
4	GNDRF	Negative supply connection associated with ANT RF input.
5	Vdd	Positive supply connection for all chip functions.
6	SQ	Squelch control logic input with an active internal pull-up when not shut down. Low to reverse level set by serial interface bit D17. Low enables squelch for default SIF register.
7	SEL0	Select (input): Logic control input with active 3 μ A (8 μ A max) internal pull-up when not in shutdown or SLEEP mode. It does not need to be defined in SLEEP mode. Used in conjunction with SEL1 to control D3 bandwidth LSB when serial interface contains default setting.
8	SHDN	Shutdown logic control input. Active internal pull-up.
9	GND	Negative supply connection for all chip functions except for RF input.
10	DO	Demodulated data (output): May be blanked until bit checking test is acceptable. A current limited CMOS output during normal operation this pin is also used as a CMOS Schmitt input for serial interface data. A 25k Ω pull-down is present when device is in shutdown and sleep modes.
11	SEL1	Select (input): Logic control input with active 3 μ A (8 μ A max) internal pull-up when not in shutdown or SLEEP mode. It does not need to be defined in SLEEP mode. Used in conjunction with SEL0, to control D4 bandwidth MSB, when serial interface contains default setting.
12	CTH	Demodulation threshold voltage integration capacitor. Capacitor-to-GND sets the settling time for the demodulation data slicing level. Values above 1nF are recommended and should be optimized for data rate and data profile.
13	CAGC	AGC filter capacitor. A capacitor, normally greater than 0.47 μ F, is connected from this pin-to-GND
14	RSSI	Received signal strength indication (output): Output is from a switched capacitor integrating op amp with 220 Ω typical output impedance.
15	SCLK	Serial interface input clock. CMOS Schmitt input. A 25k Ω pull-down is present when device is in shutdown mode.
16	RO2	Reference resonator connection. 7pF to GND during normal operation.

Absolute Maximum Ratings⁽¹⁾

Supply Voltage (Vdd) +5V
 Input Voltage +5V
 Junction Temperature +150°C
 Lead Temperature (soldering, 10sec.) 300°C
 Storage Temperature (Ts) -65°C to +150°C
 Maximum Receiver Input Power +10dBm
 EDS Rating⁽³⁾ 2KV HBM

Operating Ratings⁽²⁾

Supply voltage (Vdd) +3.0V to +3.6V
 Ambient Temperature (T_A) -40°C to +105°C
 Input Voltage (Vin) 3.6V
 Maximum Input RF Power -20dBm
 Receive Modulation Duty Cycle⁽⁶⁾ 20~80%

Electrical Characteristics

Specifications apply for V_{DD}=3.3V, V_{SS} = 0V, C_{AGC} = 4.7uF, C_{TH} = 0.1uF, f_{RX} = 850 MHz to 950 MHz unless otherwise noted.
Bold values indicate -40°C - T_A - 105°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
Iss	MICRF221 Operating Supply Current	Continuous Operation, f _{RX} = 868 MHz		9.0		mA
		Continuous Operation, f _{RX} = 915 MHz		9.5		
Ishut	Shut down Current			50		nA

RF/IF Section

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Image Rejection			20		dB
	1 st IF Center Frequency	f _{RX} = 868 MHz		1.219		MHz
		f _{RX} = 915 MHz		1.285		
	Receiver Sensitivity @ 1kbps ⁽⁴⁾	f _{RX} = 868 MHz (matched to 50Ω)		-109		dBm
		f _{RX} = 915 MHz (matched to 50Ω)		-109		
	IF Bandwidth	f _{RX} = 868 MHz		360		kHz
		f _{RX} = 915 MHz		380		
	Antenna Input Impedance	f _{RX} = 868 MHz		9.4 - j72		Ω
		f _{RX} = 915 MHz		9 - j67		
	Receive Modulation Duty Cycle	Note 6	20		80	%
	Spurious Reverse Isolation ⁽⁵⁾	ANT pin, RSC = 50 Ω		-78		dBm
	AGC Attack / Decay Ratio	t _{ATTACK} / t _{DECAY}		0.1		
	AGC pin leakage current	T _A = 25°C		+/-2		nA
		T _A = +105°C		+/-800		

Electrical Characteristics (continued)

Reference Oscillator

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Reference Oscillator Frequency	$f_{RX} = 868 \text{ MHz}$		13.54856		MHz
		$f_{RX} = 915 \text{ MHz}$		14.27643		
	Reference Oscillator Input Impedance	RO1 Pin		1500		k Ω
	Time to Data	From Shut Down		1		msec
	Reference Oscillator Input Range	With External Drive	0.5		1.5	V _{p-p}
	Reference Oscillator Source Current	RO1 Pin, V(REFOSC) = 0V		380		μA

Autopolling Operation⁽⁷⁾

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Tsleep Programming Range		10		1300	msec
I _{sleep} ⁽⁸⁾	SLEEP Current	2msec on, 1.3 sec Off		15		μA

Demodulator

Symbol	Parameter	Condition	Min	Typ	Max	Units
	CTH Source Impedance	Frefosc = 14.27643MHz		100		k Ω
	CTH Leakage Current	$T_A = 25^\circ\text{C}$		+/-2		nA
		$T_A = +105^\circ\text{C}$		+/-800		
	Demodulator Filter Bandwidth @ 915MHz	Programmable, see application section	1712		13000	Hz

Digital / Control Functions

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Input High Voltage	Pins SCLK, DO (As input), SHDN	0.8V _{dd}			V
	Input Low Voltage	Pins SCLK, DO (As input), SHDN			0.2V _{dd}	V
	Output Voltage High	DO	0.8V _{dd}			V
	Output Voltage Low	DO			0.2V _{dd}	V
	DO pin output current	As output, source @ 0.8 V _{DD}		260		μA
		As output, sink @ 0.2 V _{DD}		600		
	Output rise and fall times	CI = 15 pF, pin DO, 10-90%		2		μsec

Electrical Characteristics (continued)

RSSI

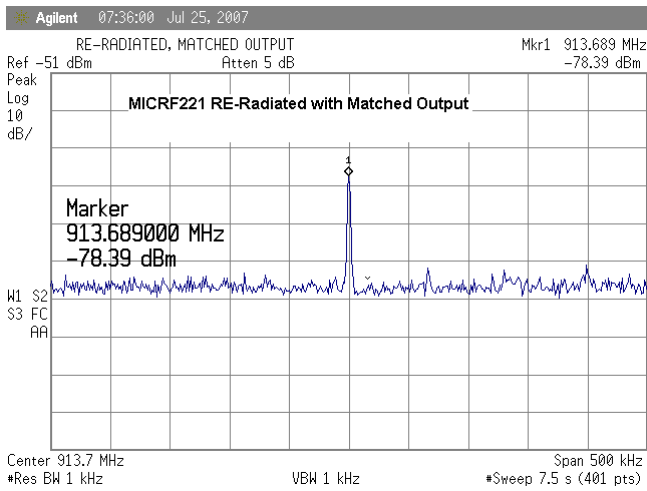
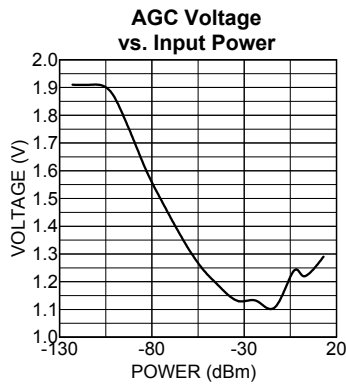
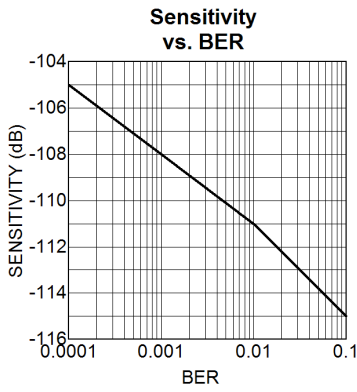
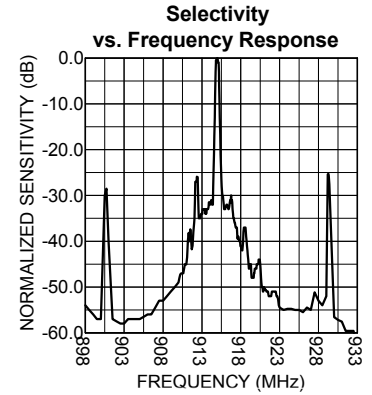
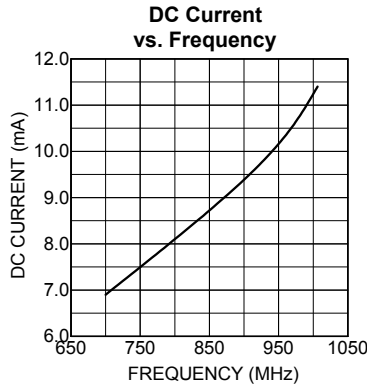
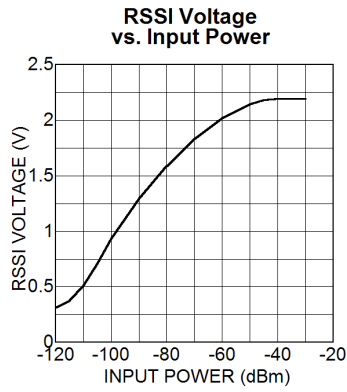
Symbol	Parameter	Condition	Min	Typ	Max	Units
	RSSI DC Output Voltage Range			0.2 to 2.0		V
	RSSI response slope	-109 dBm to -40 dBm		26		mV/dB
	RSSI Output Impedance			220		Ω

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Device is ESD sensitive. Use appropriate ESD precautions. Exceeding the absolute maximum rating may damage the device.
4. Sensitivity is defined as the average signal level measured at the input necessary to achieve 10⁻² BER (bit error rate). The input signal is defined as a return-to-zero (RZ) waveform with 50% average duty cycle (Manchester encoded).
5. Spurious reverse isolation represents the spurious component which appears on the RF input pin (ANT), measured into 50 Ohms with an input RF matching network.
6. When data burst does not contain preamble, duty cycle is defined as total duty cycle, including any "quiet" time between data bursts. When data bursts contain preamble sufficient to charge the slice level on capacitor C_{TH}, then duty cycle is the effective duty cycle of the burst alone. [For example, 100msec burst with 50% duty cycle, and 100msec "quiet" time between bursts). If burst includes preamble, duty cycle is $T_{ON}/(T_{ON} + T_{OFF}) = 50\%$; without preamble, duty cycle is $T_{ON}/(T_{ON} + T_{OFF} + T_{QUIET}) = 50\text{msec}/200\text{msec} = 25\%$. T_{ON} is the number of 1's during the burst time \times bit time T_{OFF} = T_{BURST} - T_{ON}.
7. Auto-polling refers to power-cycling mode of operation where characteristics of the received signal are used to determine the likelihood of an incoming data signal at the beginning of the Ton period. If there is no signal detected within a period programmable by the user, the user can program the number of bits: 0,2,4,8 that must be good for device to wake up. The time will depend on the data rate. If two bad bits are detected this will cause device to revert to SLEEP. If no bits are detected device will revert to SLEEP in 5ms, 10ms, or 20ms depending on selected demodulator bandwidth. Otherwise, the device remains "On" until commanded into SLEEP by an external source e.g., decoder or microprocessor. This technique minimizes the average Ton time. Refer to Serial Interface and Applications sub-sections for further details.
8. Average SLEEP mode current depends on the SLEEP time programmed and the SLEEP oscillator variation which is $\sim \pm 20\%$ independent of ref osc.

Typical Characteristics

Sensitivity Graphs



Functional Diagram

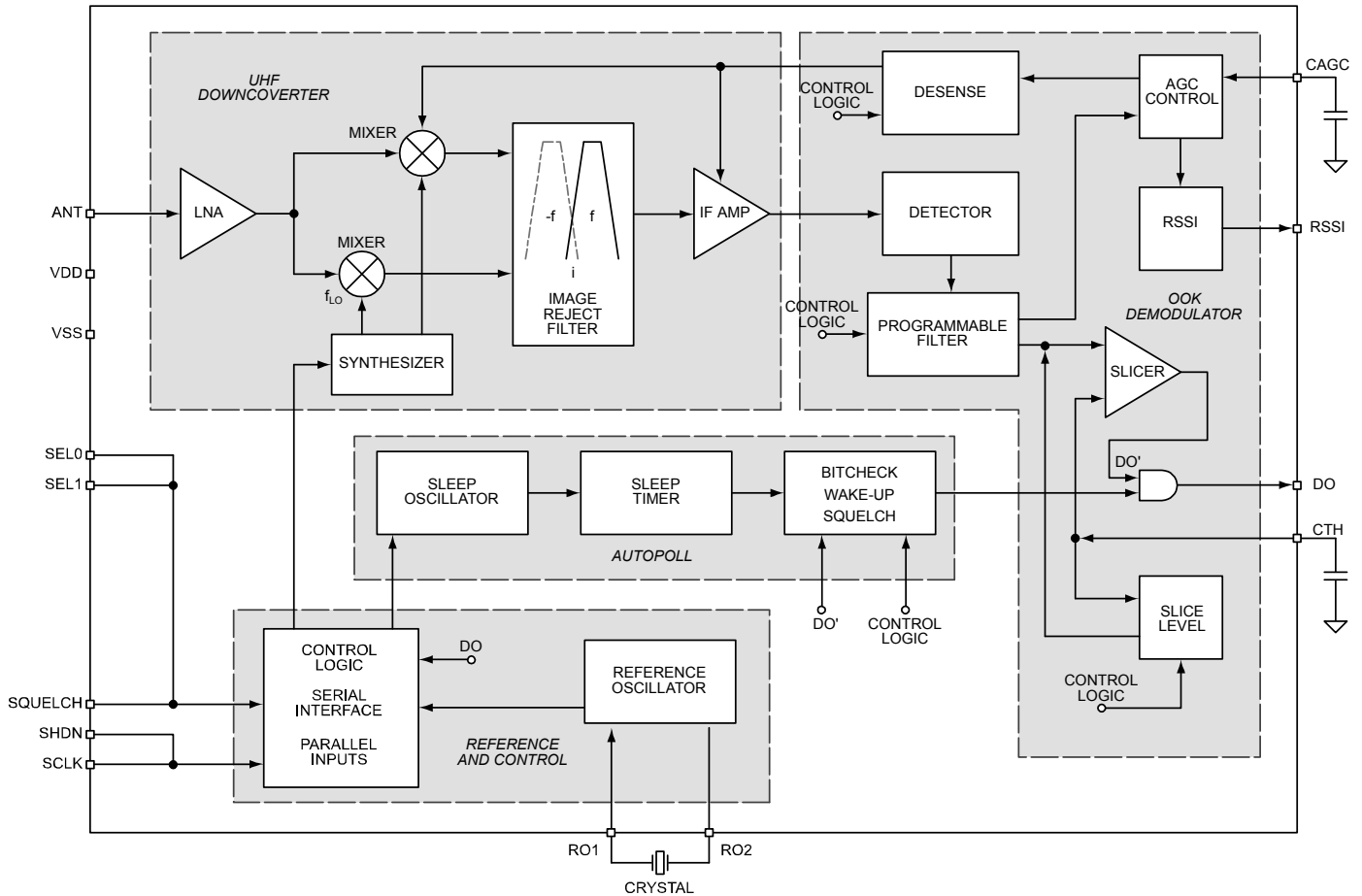


Figure 3. Simplified Block Diagram

Functional Description

The simplified block diagram, shown in Figure 3, illustrates the basic structure of the MICRF221 receiver. It is made of four sub-blocks:

- UHF Down-converter
- OOK Demodulator
- Reference and Control logic
- Auto-poll circuitry.

Outside the device, the MICRF221 receiver requires just three components to operate: two capacitors (CTH, and CAGC) and the reference frequency device (usually a quartz crystal). An additional five components are used to improve performance: a power supply decoupling capacitor, two components for the matching network, and two components for the

pre-selector band-pass filter.

Receiver Operation

UHF Downconverter

The UHF down-converter has six components: LNA, mixers, synthesizer, image reject filter, band pass filter and IF amp.

LNA

The RF input signal is AC-coupled into the gate circuit of the grounded source LNA input stage. The LNA is a Cascoded NMOS amplifier. The amplified RF signal is then fed to the RF ports of two double balanced mixers.

Mixers and Synthesizer

The LO port of the mixers are driven by quadrature local oscillators of the synthesizer block. The synthesizer block produces the local oscillator signal on the low side of the desired RF signal with suppression of the image frequency, at twice the IF frequency below the wanted signal. The local oscillator is set to 64 times the crystal reference frequency by way of a phase locked loop synthesizer with a fully integrated loop filter.

Image Reject Filter and Band-Pass Filter

The IF ports of the mixer produce quadrature down-converted IF signals. The IF signal is filtered by the image reject filter to remove image frequency components and then follow up with a third order band-pass filter. The IF center frequency is 1.285MHz. The IF BW is 380kHz @ 915 MHz, and the IF BW varies with RF operating frequency. The IF BW can be calculated via direct scaling.

$BW_{IF} = BW_{IF@915MHz} * (\text{Operating Freq (MHz)} / 915)$

These filters are fully integrated inside the MICRF221.

After filtering, four active gain controlled amplifier stages enhance the IF signal to proper level for demodulation.

OOK Demodulator

The demodulator section is comprised of detector, programmable low pass filter, slicer, AGC and Desense.

Detector and Programmable Low-Pass Filter

The demodulation starts with the detector removing the carrier from the IF signal. Post detection, the signal becomes baseband information. The programmable low-pass filter further enhances the baseband information. There are four settings for programmable low-pass filter BW options: 1625Hz, 3250Hz, 6500Hz, 13000Hz. for 915MHz operation. Low pass filter BW will vary with RF Operating Frequency. Filter BW values can easily calculated by direct scaling. See equation below for filter BW calculation:

$BW_{Operating\ Freq} = BW_{@915MHz} * (\text{Operating Freq (MHz)} / 915)$

It is very important to choose filter setting that fits best for the intended data rate to minimize data distortion.

Demod BW is set at 13000Hz @ 915MHz as default (assuming both SEL0 and SEL1 pins are floating). The low pass filter can be hardware set by external pins SEL0 and SEL1, or via serial programming through register D3 and D4

D3 SEL0	D4 SEL1	Demod BW (@ 915MHz)
0	0	1625Hz
1	0	3250Hz
0	1	6500Hz
1	1	13000Hz - default

Slicer and Slicing Level

The signal prior to the slicer is still AM. The data slicer converts the AM signal into ones and zeros based upon the threshold voltage built up in the CTH capacitor. After the slicer, the signal is ASK or OOK digital data.

The slicing threshold defaults at 50%. The slicing threshold can be set via serial programming through register D5 and D6.

D5	D6	Slicing Level
1	0	Slice Level 30%
0	1	Slice Level 40%
1	1	Slice Level 50% - default
0	0	Slice Level 60%

AGC

AGC monitors the signal amplitude from the output of the programmable low-pass filter. When the output signal is less than 750mV threshold, AGC increases the gain of the mixer and the IF amplifier. When the output signal is greater than 750mV, the AGC lowers the gain of the mixer and the IF amplifier.

Desense

Desense is a function designed to reduce the sensitivity of the MICRF221 receiver to a maximum of 45dB for training the MICRF221 receiver to recognize an intended transmitter. Very often, a receiver needs to learn how to recognize a particular transmitter. It is important for the receiver not to learn the signal of a stray transmitter near by. The simplest solution is to turn down the receiver gain, so the receiver only recognizes the transmitter at close range.

The desense function is accessible only through serial programming.

D0	D1	D2	MODE: Desense
0	X	X	No Desense - default
1	0	0	7dB Desense
1	1	0	19dB Desense
1	0	1	32dB Desense
1	1	1	42dB Desense

Reference Control

There are two components in the Reference and Control sub-block: 1) Reference Oscillator and 2) Control Logic, Serial Interface and Parallel Inputs.

Reference Oscillator

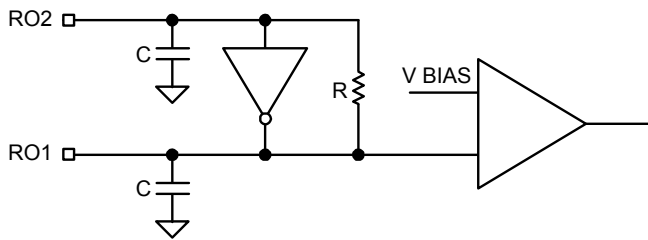


Figure 4. MICRF221 Reference Oscillator Circuit

The reference oscillator in the MICRF221 uses a basic Pierce crystal oscillator configuration with MOS transconductor to provide negative resistance. MICRF221 has built-in load capacitors for the crystal oscillator, shown in Figure 4, even though external load capacitors are still needed for tuning to the right frequency. RO1 and RO2 are external pins of the MICRF221 and are to connect to the reference oscillator crystal.

The reference oscillator crystal frequency can be calculated as follows:

$$FREF OSC = FRF / (64 + 1.1/12)$$

For 868.35 MHz,

$$FREF OSC = 13.54856 MHz$$

For 915 MHz

$$FREF OSC = 14.27643 MHz$$

To operate the MICRF221 with minimum offset, crystal frequencies should be specified with 10pF loading capacitance.

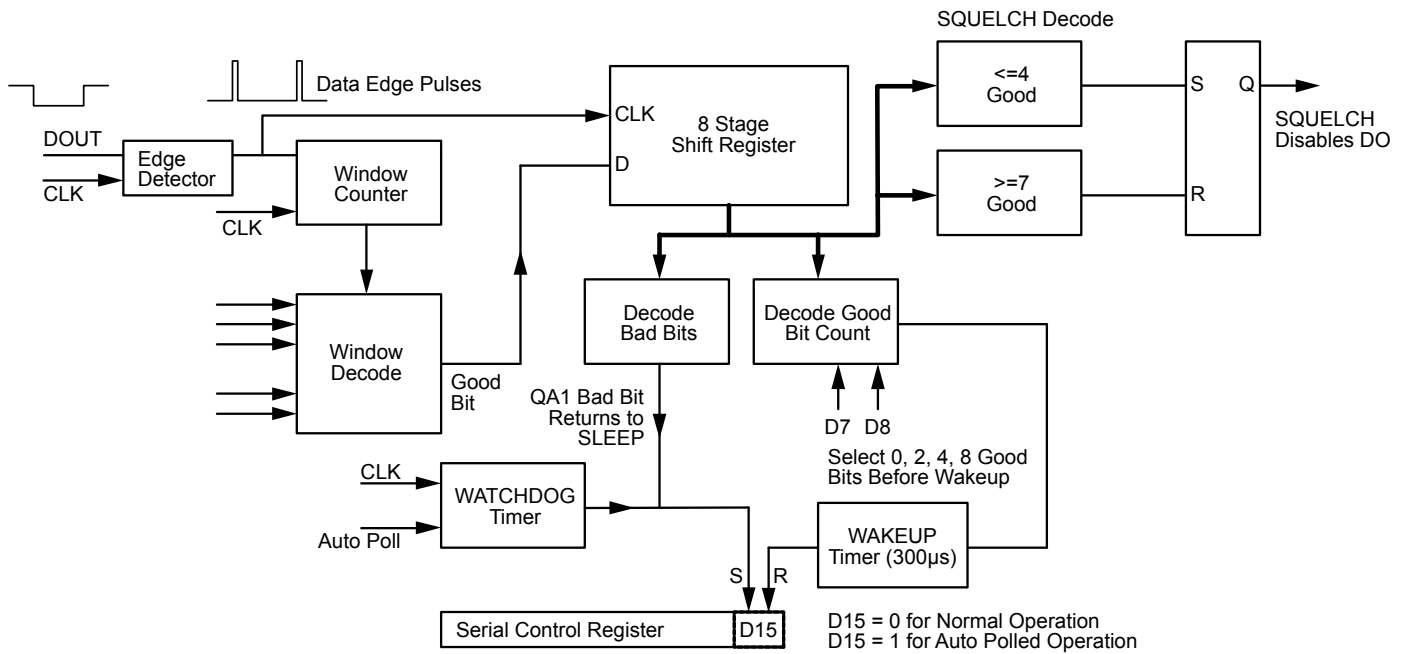


Figure 4. MICRF221 Autopoll-Bitcheck-Block Diagram

Auto-Polling

The auto-poll block (Figure 4) contains a low power oscillator to drive the sleep timer when the rest of the device is powered down, plus circuits to check whether the received bits are good. Auto-polling is controlled by bit D15 in the serial register, in conjunction with bits D12,13,14 to set the sleep timer period. Bits D7, D8, are used for control of the bitchecking operation and bits D9, D10, D11 are used to adjust the sensitivity of the bitcheck action.

For simple auto-polling without bitchecking, send a serial command with bit 15 set high and bits D12, D13, D14 set to the desired sleep time. The device will go to sleep for the programmed timer duration then wake up to receive data if present. Device will stay awake until serial bit D15 is set low then set high again to enable a further sleep period. Sleep duty cycle may be controlled by the timing of serial commands.

For polling with bitchecking the serial register bits D7 and D8 need to be set for the number of bits to be checked as good, before the receiver outputs data at the DO pin. The bitcheck window bits D9, D10, D11

must also be set to match the data period. The default shortest window time gives the least critical bitcheck action. For better discrimination, the window setting may be increased up towards the normal minimum time expected between data edges. Note that a window time set longer than this will result in all bits being tested as bad and the device will remain in sleep polling mode. Now when the serial command is sent to set bit D15 high the device will go to sleep for the timer period, then will start to receive and check bits. The device will output data again at DO as soon as the programmed number of good RTZ bits have been received. If a bad bit is seen the device will return to sleep mode and poll again for good data after the timeout period. Both high and low periods are checked for each RTZ bit. If data transitions are not received the device will return to sleep after the bitcheck watchdog timeout period unless bit D18 has been sent, in which case the device will continue to check bits until sufficient good bits enable the device to wake up, or bad bits return the device to sleep.

Operation

Trigger pulses are generated from internal D0 edges and compare with programmable window generated from the reference clock frequency. If time between data edges falls within the window data pulse width is bad. Detected stable bits are counted. Wakeup will occur allowing data to output if sufficient data bits are detected. Two bad pulses or lack of pulse cause device to go to sleep for sleep timer duration.

Squelch action

During normal operation, if 4 or less out of 8 bit pulses are good squelch output is activated. If good bit count increases to 7 or more in any 8 sequential bits squelch output is set low allowing data to output at DO pin.

Serial Interface

Control Register Individual Truth Tables:

D0	D1	D2	MODE: Desense
0	X	X	No Desense - default
1	0	0	7dB Desense
1	1	0	19dB Desense
1	0	1	32dB Desense
1	1	1	42dB Desense

D3	D4	MODE: Demod Bandwidth (at 915MHz)
0	0	1625Hz
1	0	3250Hz
0	1	6500Hz
1	1	13000Hz - default

D5	D6	MODE
1	0	Slice Level 30%
0	1	Slice Level 40%
1	1	Slice Level 50% - default
0	0	Slice Level 60%

D7	D8	MODE: Bit Check Setting
0	0	Bitcheck 0 bits - default
1	0	Bitcheck 2 bits
0	1	Bitcheck 4 bits
1	1	Bitcheck 8 bits

D9	D10	D11	MODE: Bitcheck Window Times (915MHz)
0	0	0	67us, 136us, 270us, 541us
1	0	0	64us, 126us, 252us, 505us
0	1	0	59us, 118us, 234us, 469us
1	1	0	54us, 108us, 216us, 434us
0	0	1	49us, 100us, 198us, 397us
1	0	1	45us, 90us, 180us, 361us
0	1	1	41us, 82us, 163us, 325us
1	1	1	36us, 72us, 144us, 289us

D12	D13	D14	MODE: Sleep Time
0	0	0	10ms
1	0	0	20ms
0	1	0	40ms
1	1	0	80ms
0	0	1	160ms
1	0	1	320ms
0	1	1	640ms
1	1	1	1280ms

D15	MODE: Auto Poll
0	Awake – does not poll - default
1	Auto-polls with Sleep periods

D16	MODE: Demod BW Select
0	Normal Demod BW's - default
1	Fast Demod BW's

D17	MODE: Squelch Enable
0	Squelch circuit off - default
1	Squelch circuit active

D18	MODE
0	Sleep polling watchdog active - default Watchdog time for D3, D4, BW setting: 11 01 10 00 5ms 5ms 10ms 20ms
1	Sleep polling watchdog disabled - unlimited poll period

D19	MODE
0	RSSI offset 0mV - default
1	RSSI offset +200mV

Application Information

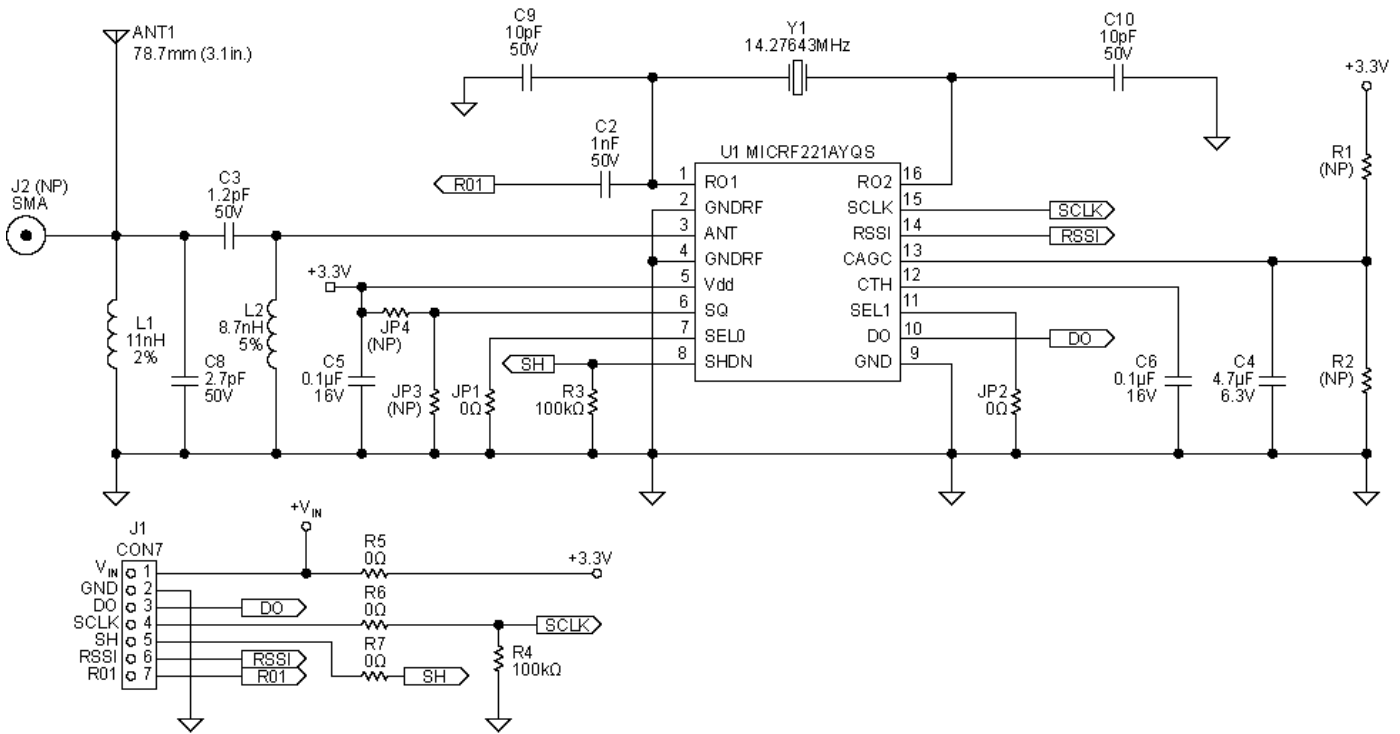


Figure 5 – QR221BPF Application Example, 915.0 MHz

The MICRF221 receiver can be fully tested by using one of the many evaluation boards designed at Micrel for this device. As an entry level, the QR221BPF (Figure 5) offers a good start for most applications. It has a connector for a whip antenna (ANT1), a band-pass filter front end (L1 & C8) as a pre-selector filter, and a matching network (C3 & L2). It also includes the minimum components required to make the device work, which are: a crystal, C_{AGC}, and C_{TH} capacitors. An RF connector (J2) can be used instead of the whip antenna when tests require an RF signal generator. Figure 5 shows the entire schematic for 915.0MHz. Other frequencies can be used. The values needed for the various components are listed in the tables below.

L1 and C8 form the pass-band filter front end. Its purpose is to attenuate undesired outside band noise which reduces the receiver performance. It is calculated by the parallel resonance equation

$$f = 1/(2 \times \pi \times (\text{SQRT } L1 \times C8))$$

Table 2 shows the most used frequency values.

Freq (MHz)	C8 (pF)	L1(nH)
868.35	2.7	12
915.0	2.7	11
916.5	2.7	11

Table 2. Band-Pass-Filter Front-End Values

There is no need for the band-pass filter front end in applications where it is proven that the outside band noise does not cause a problem. The MICRF221 receiver incorporates image reject mixers that improve the selectivity and rejection of outside band noise significantly.

Matching Calculations

Capacitor C3 and inductor L2 form the L-shaped matching network. The capacitor provides additional attenuation for low frequency outside band noise and the inductor provides additional ESD protection for the antenna pin. Two methods can be used to find these values, which are matched close to 50Ω. One method calculates the values using the equations below, and another by using a Smith chart. The Smith chart is made easier by using software that plots the values of the components C3 and L2, such as WinSmith by Noble Publishing.

To calculate matching values, you need to know the input impedance of the device. Table 3 shows the input impedance of the MICRF221 receiver and suggested matching values for the most used frequencies. These suggested values may be different if your layout is different from the layout for the QR221BPF evaluation board.

Freq (MHz)	C3 (pF)	L2(nH)	Z device (Ω)
868.35	1.2	9.5, Coilcraft	9.4-j71.8
915.0	1.2	8.7, Coilcraft	9.0-j67.4
916.5	1.2	8.7, Coilcraft	8.5-j68.0

Table 3. Matching Values for the Most Used Frequencies

For the frequency of 915.0MHz, the input impedance is $Z = 9.0-j67.4\Omega$. The matching components are calculated by:

$$\text{Equivalent parallel} = B = 1/Z = 1.95 + j14.6 \text{ msiemens}$$

$$R_p = 1 / \text{Re} (B); \quad X_p = 1 / \text{Im} (B)$$

$$R_p = 513\Omega; \quad X_p = 68.5\Omega$$

$$Q = \text{SQRT} (R_p/50 + 1)$$

$$Q = 3.35$$

$$X_m = R_p / Q$$

$$X_m = 153.1\Omega$$

Resonance Method For L-shape Matching Network:

$$L_c = X_p / (2 \times \text{Pi} \times f); \quad L_p = X_m / (2 \times \text{Pi} \times f)$$

$$L_2 = (L_c \times L_p) / (L_c + L_p); \quad C_3 = 1 / (2 \times \text{Pi} \times f \times X_m)$$

$$L_2 = 8.2\text{nH}$$

$$C_3 = 1.14\text{pF}$$

Doing the same calculation, example with the Smith Chart, it would appear as follows:

First, plot the input impedance of the device

($Z = 9.0 - j67.4\Omega$) @ 915.0MHz.(Figure 6).

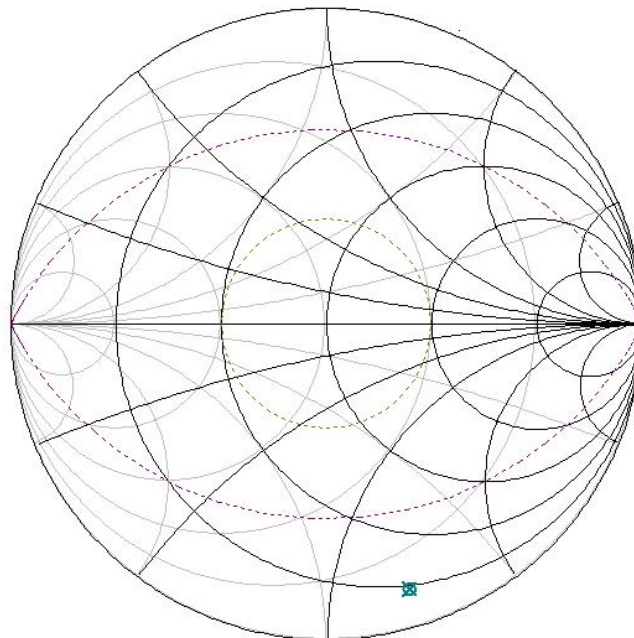


Figure 6. Device’s Input Impedance, $Z = 9.0 - j67.4\Omega$

Because stray parasitic elements can be caused by both the printed circuit board as well as the components themselves, the values plotted are slightly different from the calculated ones. Therefore, one plots the shunt inductor (8.7nH, from Coilcraft) and the series capacitor (1.2pF) for the desired input impedance (Figure 7). One can then see the matching leading to the center of the Smith Chart or close to 50Ω.

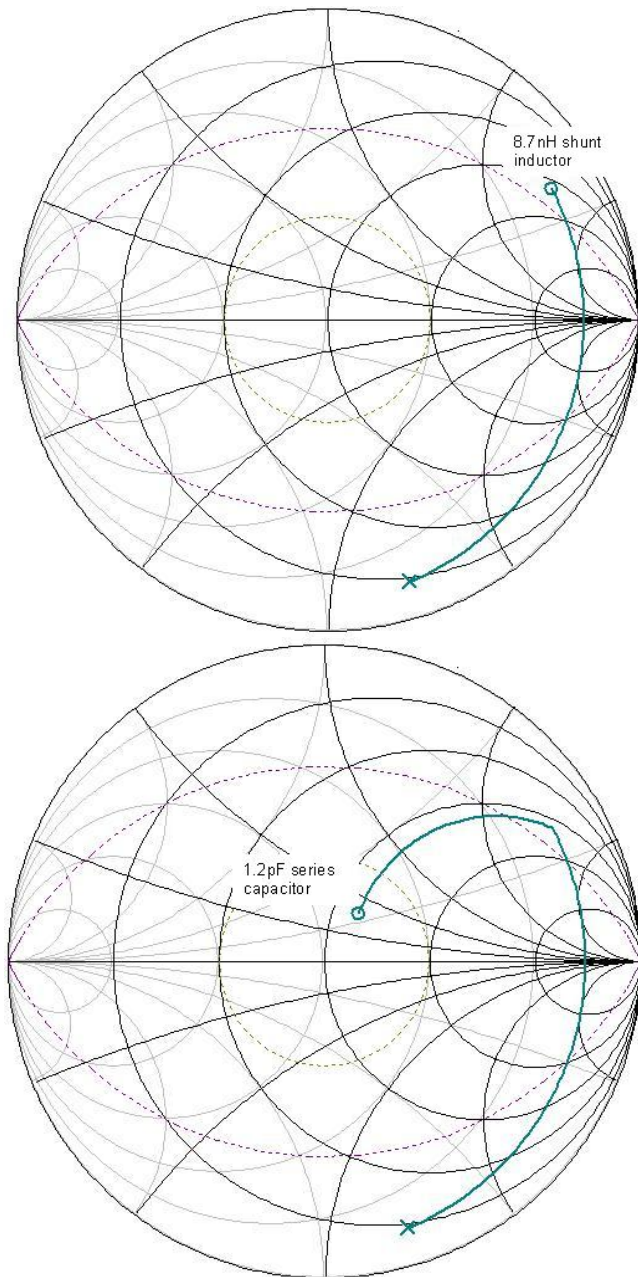


Figure 7. Plotting the Shunt Inductor and Series Capacitor

RF Oscillator Calculation

Crystal Y1 is the reference clock for all the device's internal circuits. Internally, the device has a Pierce Oscillator configuration, requiring the external capacitors, C9 and C10, to adjust the crystal center frequency. The exact values for these capacitors depend on the printed circuit board's stray capacitance.

For example, with a top ground plane or longer traces, the value of these capacitors will be less than 10pF since there will be more stray capacitance. If a different layout from the one presented here is used, the capacitor values are optimized by getting the best sensitivity of the device. Crystal characteristics of 10pF load capacitance, 30ppm, ESR < 200Ω, -40°C to +105°C temperature range are desired.

Table 4 shows the crystal frequencies and two of Micrel's approved crystal manufactures (www.hib.com.br or www.abracon.com).

Crystal frequency is calculated using:

$$REFOSC = RF\ Carrier / (64 + (1.1/12))$$

The local oscillator is a low side injection type, so for the 915.0MHz carrier, the local oscillator is calculated by:

$$64 \times REFOSC = RF\ Local\ OSC$$

$$64 \times 14.27643MHz = 913.69MHz$$

That is, its frequency is below the RF carrier frequency and the image frequency is below the LO frequency. See Figure 8. The product of the incoming RF signal and local oscillator signal will yield the IF frequency, which is demodulated by the detector circuits.

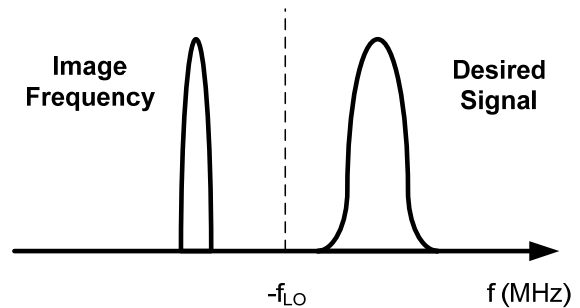


Figure 8. Low Side Injection Local Oscillator

REFOSC (MHz)	Carrier (MHz)	HIB Part Number	Abracon Part Number
13.54856	868.35	SA-13.548560-F-10-H-30-30-X	ABLS-13.54860MHz-10-J4Y
14.27643	915.0	SA-14.276430-F-10-H-30-30-X	ABLS-14.276430MHz-10-J4Y
14.29983	916.5	SA-14.299830-F-10-H-30-30-X	ABLS-14.299830MHz-10-J4Y

Table 4. Crystal Frequency and Vendors Part Number

Demodulation Bandwidth Calculation

JP1 and JP2 are used to select the bandwidth for the demodulator. To set the bandwidth correctly, it is necessary to know the shortest pulse width of the encoded data sent in the transmitter. As shown in the example of the data profile in the Figure 9 below, PW2 is shorter than PW1, so PW2 should be used for the demodulator bandwidth calculation which is found by calculating 0.65/shortest pulse width. After this value is found, the setting should be done according to Table 5.

For example, if the pulse period is 100µsec, 50% duty cycle, the pulse width will be 50µsec:

$$(PW = (100\mu\text{sec} \times 50\%) / 100)$$

So, a bandwidth of 13kHz would be necessary (0.65 / 50µsec). However, if this data stream had a pulse period with 20% duty cycle, the bandwidth required would be 32.5kHz (0.65 / 20µsec), which exceeds the maximum bandwidth of the demodulator circuit. If you try to exceed the maximum bandwidth, the pulse will appear stretched or wider.

SEL0 JP1, D3	SEL1 JP2, D4	Demod. BW (hertz)	Shortest Pulse (µsec)	Maximum baud rate for 50% Duty Cycle (hertz)
Short	Short	1712	380	1316
Open	Short	3425	190	2632
Short	Open	6850	95	5264
Open	Open	13700	47	10528

Table 5. JP1 and JP2 setting, 915 MHz

This device is capable of higher baud rates when the serial bit D16 is programmed high. More detail is provided on the following pages.

C_{TH} and C_{AGC} Selection

Capacitors C6 (C_{TH}) and C4 (C_{AGC}) provide time base reference for the data pattern received. These capacitors are selected according to the data profile, pulse duty cycle, dead time between two received

data packets and if the data pattern has or does not have a preamble. See Figure 9 for an example of a data profile.

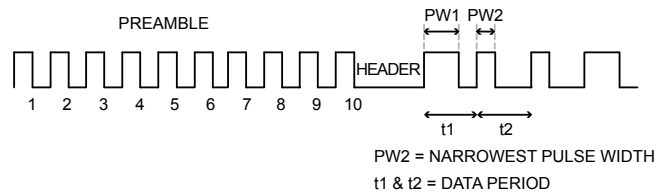


Figure 9. Example of a Data Profile

For best results C4 and C6 should be optimized for the data pattern used. As the baud rate increases, the capacitor values decrease. Table 6 shows suggested values for Manchester Encoded data at a 50% duty cycle.

SEL0 JP1	SEL1 JP2	Demod. BW (hertz)	C _{TH}	C _{AGC}
Short	Short	1712	100nF	4.7µF
Open	Short	3425	47nF	2.2µF
Short	Open	6850	22nF	1µF
Open	Open	13700	10nF	0.47µF

Table 6. Suggested C6 (C_{TH}) and C4 (C_{AGC}) Values

JP4 (pins 5 and 6) is a jumper used to configure the digital squelch function. When pin 6 (SQ) is held high (jumpered-to-V_{DD}), there is no squelch applied to the digital circuits and pin 10 (DO, data out) has a hash signal. When pin 6 (SQ) is low, the DO pin activity is considerably reduced. It will have more or less activity than is shown in Figure 11 depending upon the outside band noise. The penalty for using squelch is a delay in getting a good signal at the DO pin, that is, it takes longer for the data to show. The delay is dependent upon many factors such as RF signal intensity, data profile, data rate, C_{TH} and C_{AGC} capacitor values and outside band noise. See Figures 10 and Figure 11.

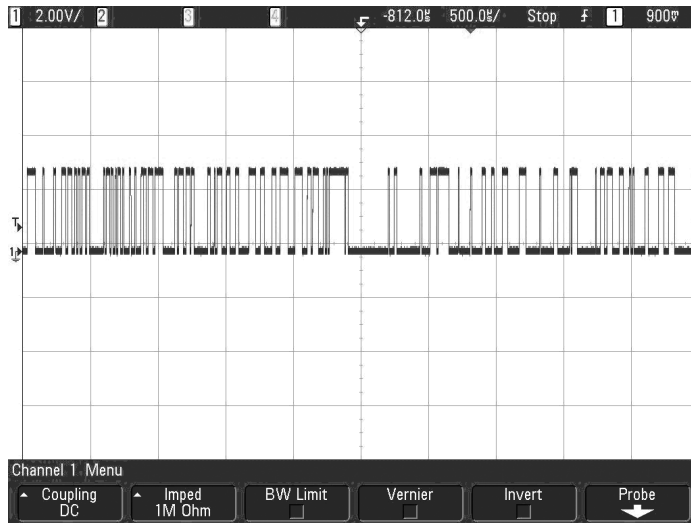


Figure 10. Data Out Pin with No Squelch (SQ = 1)

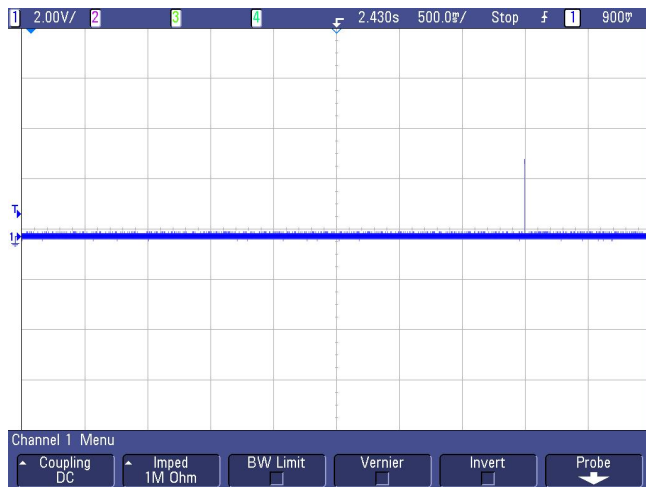


Figure 11. Data Out Pin with Squelch (SQ = 0)

Other components used include:

C5 is a decoupling capacitor for the V_{DD} line.

R4 should be referenced to ground when a microcontroller connection is not made and kept low by the microcontroller when not programming the device.

R3 is the reference for the shutdown pin (SHDN = 0, device is operation), which can be removed if that pin is connected to a microcontroller or an external switch.

R1 and R2 form a voltage divider for the AGC pin. One can purposely decrease the device sensitivity by forcing a voltage to this AGC pin. Special care is needed when doing this operation, as an

external control of the AGC voltage may vary from lot-to-lot and may not work the same for several devices.

5V Operation

5-volt operation can be obtained by replacing R5, R6, and R7 (0 Ω resistors) to R5 = 150Ω, R6 = R7 = 33 kΩ. The 5-volt source must be regulated and guaranteed never to exceed 5V. DO is equal to V_{DD} levels.

Four other pins are worthy of comment. They are the DO, RSSI, SHDN, and SCLK pins.

DO Pin

The DO pin has a driving capability of 0.4mA. This is good enough for most of the logic families ICs on the market today. It also works as an input when programming the device for the serial register control

RSSI Pin

The RSSI pin provides a transfer function of RF signal intensity versus voltage. It is useful to determine the signal-to-noise ratio of the RF link, crude range estimate from the transmitter source and AM demodulation, which requires a low C_{AGC} capacitor value.

SCLK Pin

Serial interface input clock is a CMOS Schmitt input. A 25kΩ pull-down is present when device is in shutdown mode. See “Programming the Device” section for timing diagram and functional operation

SHDN (Shut Down) Pin

The shut down pin (SHDN) can be used to save energy. If its level is close to V_{DD} (SHDN = 1), the device will not be in operation. Its DC current consumption is less than 1μA (R3 must be removed). This input pin is designed with a weak pull-up. The pull-up current is decreased once the input has switched above the threshold level, that is, the device is shut down and progressively decreases to levels below 1μA.

When shut down pin is toggling from high to low (getting out of shut down mode), there is some time required for the device to come to steady-state mode and some time needed for data to appear at the DO pin. The actual time required is dependent upon several factors, such as temperature, the crystal used and if there is an external oscillator coupled through C2 with faster startup time. Normally (assuming the suggested crystal vendors are used), the preamble data will appear at the DO pin at approximately 1msec time, and 2msec over the temperature range of the device.

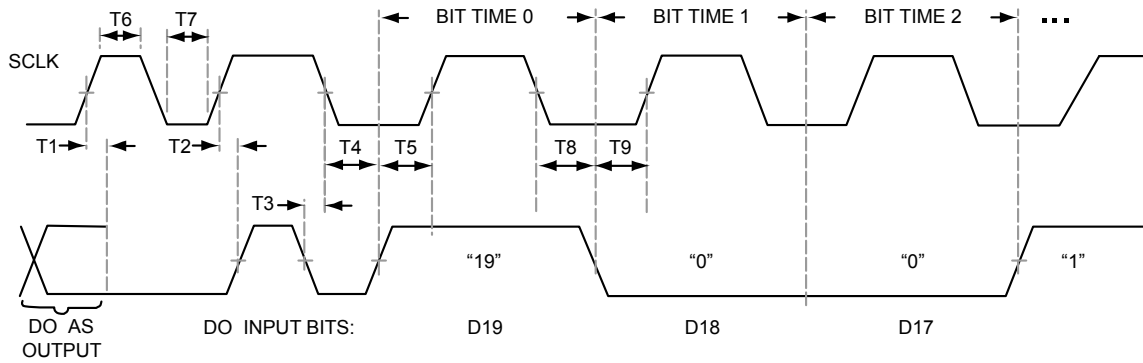


Figure 12. Serial Interface Start Sequence

When using an external oscillator or reference oscillator signal, the maximum level should not exceed 1.5V_{pp}. See Figure 13. Channel 4 is the transmitted data, which is synchronized with the shutdown shown in the oscilloscope (channel 2). Data out is shown on channel 1 and, as seen below, the preamble data starts to appear just over 1msec after the shutdown pin cycle low to high. Also note that when squelch is used time for data to appear is increased.

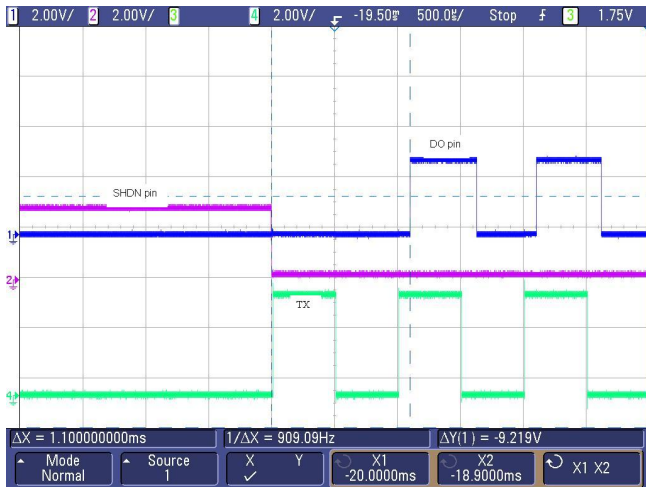


Figure 13. Time-to-Preamble Data after Shut Down Cycle, Room Temperature

Programming the Device

Several additional functions are available by the serial interface. They are:

- Desense, to reduce the device sensitivity
- Slice Level, to further optimize data profile demodulation
- Autopoll Mode, to wake an external

device through the DO pin toggling from low to data

- High Demodulator Bandwidth, for faster baud rates
- Parallel input pins SEL0, SEL1, and SQ can be programmed using the serial interface

Programming the device is accomplished by the use of pins DO and SCLK. Normally, pin 10 (DO) is outputting data and needs to switch to an input pin made by the start sequence, as shown at Figure 13. A high at the SCLK pin tri-states the DO pin, enabling the external drive into the DO pin with an initial low level. The start sequence is completed by taking SCLK low, then high while DO is low, followed by taking DO high, then low while SCLK is high. The serial interface is initialized and ready to receive the programming data.

Bits are serially programmed starting with the most significant bit (MSB = D19) if all bits are being programmed until the least significant bit (LSB =D0) For instance, if only the desense bits D0, D1, and D2 are being programmed, then these are the only bits that need to be programmed with the start sequence D2, D1, D0, plus the stop sequence. Or, if only the squelch bit D17 is needed, then the sequence must be from start sequence, D17 through D0 plus the stop sequence, making sure the other bits (besides D17) are programmed as needed. It is recommended that all parallel input pins (SEL0, SEL1, and SQ) be kept high when using the serial interface. After the programming bits are finished, a stop sequence (as shown in Figure 14) is required to end the mode and make the DO pin as an output again. To do so, the SCLK pin is kept high while the DO pin changes from low to high, then low again, followed by the SCLK pin made low. Timing of the programming bits are not critical, but should be kept as shown below:

T1 < 0.1 us, Time from SCLK to convert DO to input pin

T6 > 0.1 us, SCLK high time

T7 > 0.1 us, SCLK low time

T2, T3, T4, T5, T8, T9, T10 > 0.1 us

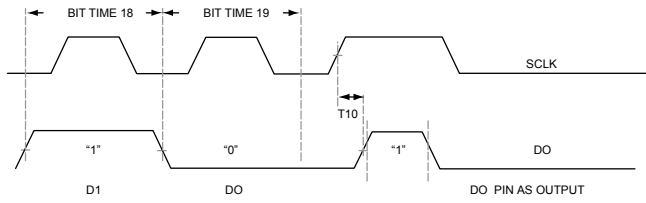


Figure 14. Serial Interface Stop Sequence

Serial Interface Examples

All bits (D19 through D0) low (channel 1 is the DO pin, and Channel 2 is the SCLK pin), see Figure 15.

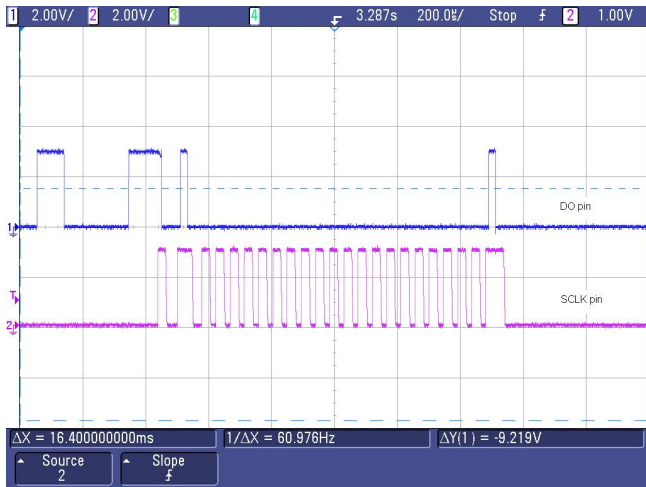


Figure 15. All bits 0s.

All bits (D19 through D0) High, Figure 16.

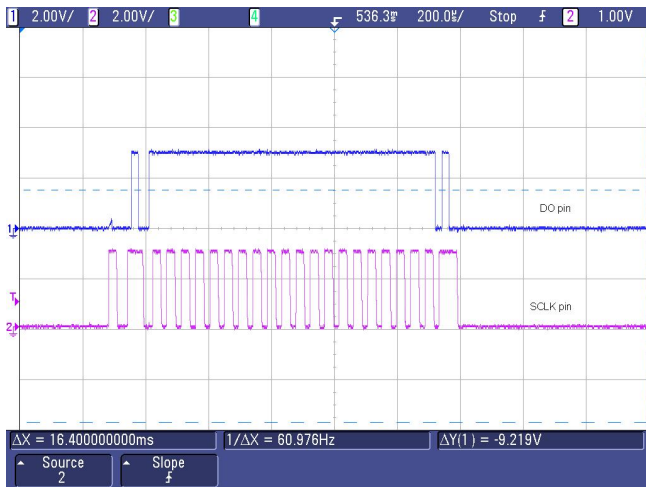


Figure 16 All bits 1s.

Only bits 19 and 18 High, Figure 17.

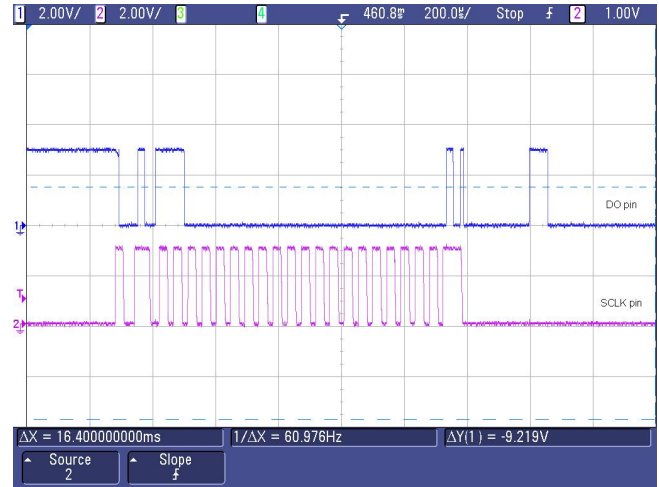


Figure 17 D19 = D18 = 1.

Autopoll example, Figure 18.

D0 = D1 = D2 = 0, no desense

D3 = D4 = 0, demodulator bandwidth = 1712 hertz, 1 kHz baud rate, pulse = 500 usec, required demodulator bandwidth is 0.65/500usec = 1300 hertz

D5 = D6 = 1, Slice level = 50%

D7 = 0, D8 = 1, bit check = 4 bits. This is the time the device is ON checking for four consecutive valid windows.

D9 = D10 = 1, D11 = 0, data rate is 1 kHz, (500 usec pulses), window set to 433 usec (< 500 usec)

D12 = D13 = 0, D14 = 1, sleep timer set to 160 msec, that is, 4 bit is ON and 160 msec is OFF.

D15 = 1, device is placed in autopoll

D16 = 0, normal demodulator bandwidth

D17 = 0, squelch is OFF

D18 = 1, watchdog timer is OFF

D19 = 0, no RSSI offset

From MSB to LSB, see Table 7:

D19	D18	D17	D16	D15	D14	D13	D12
0	1	0	0	1	1	0	0
D11	D10	D9	D8	D7	D6	D5	
0	1	1	1	0	1	1	
D4	D3	D2	D1	D0			
0	0	0	0	0			

Table 7. Autopoll example bit sequence

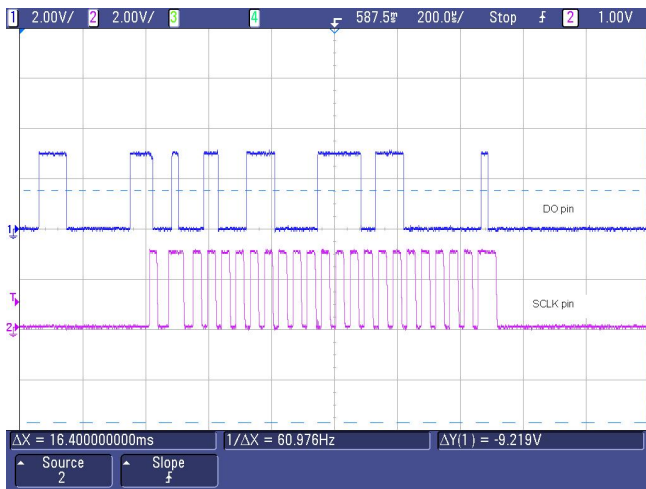


Figure 18. Autospill example

PCB LAYOUT RECOMMENDATIONS

PCB Considerations and Layout

Figures 19 to 22 below, show some of the printed circuit layers for the QR221BPF board, refer to Figure 5. Use the Gerber files provided (downloadable from the Micrel Website at: www.micrel.com), which have the remaining layers needed to fabricate this board. When copying or making one's own boards, make traces as short as possible. Long traces alter the matching network and the values suggested are no longer valid. Suggested Matching Values may vary due to PCB variations. A PCB trace 100 mills (2.5mm) long has about 1.1nH inductance.

Optimization should always be done with exhaustive range tests.

Make individual ground connections to the ground plane with a VIA for each ground connection. Do not share VIAs with ground connections. Each ground connection = one or more VIAs. The ground plane

must be solid and, if possible, without interruptions. Avoid a ground plane on the top layer next to the matching element, as it will normally add additional stray capacitance, which changes the matching.

Do not use phenolic material; use only FR4 or better materials, since phenolic material is conductive above 200MHz.

The RF path should be as straight as possible, avoiding loops and unnecessary turns.

Separate the ground and V_{DD} lines from other circuits (microcontroller, etc).

Known sources of noise should be positioned as far as possible from the RF circuits.

Avoid thick traces. The higher the frequency, the thinner the trace should be to minimize losses in the RF path.

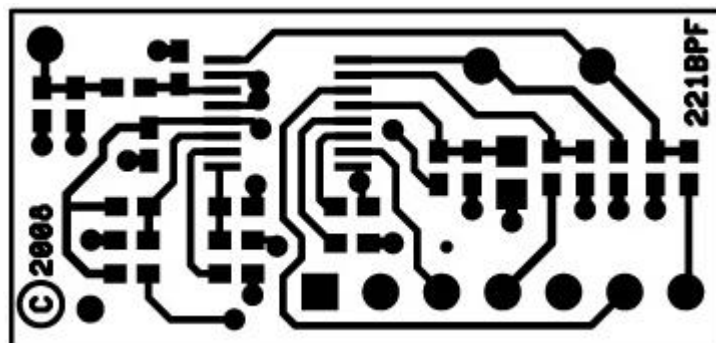


Figure 19. QR221BPF Top Layer

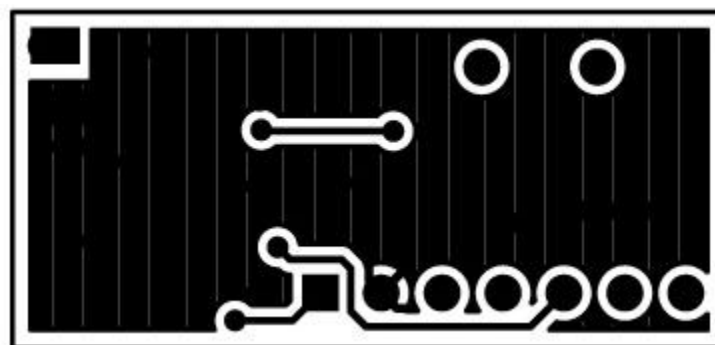


Figure 20. QR221BPF Bottom Layer, Mirror Image

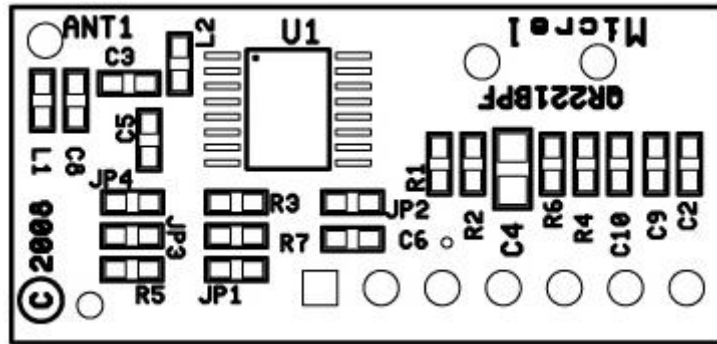


Figure 21. QR221BPF Top Silkscreen Layer

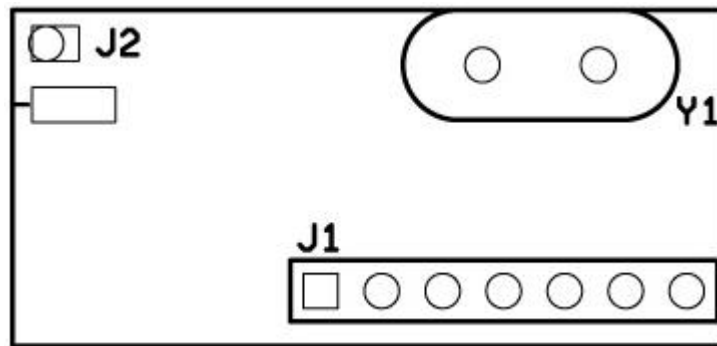


Figure 22. QR221BPF Bottom Silkscreen Layer, Mirror Image

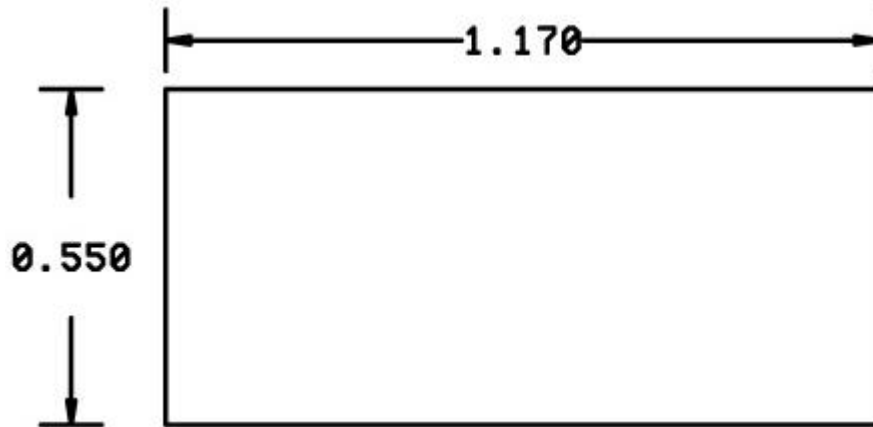


Figure 23. QR221BPF Dimensions (inches)

QR221BPF Bill of Materials, 915.0 MHz

Item	Part Number	Manufacturer	Description	Qty.
ANT1			50-Ω Ant78.7mm (3.1 inches) 20 AWG, rigid wire	1
C3	GRM39COG1R2C50	MuRata	1.2pF , 0402/0603	1
C4		Murata / Vishay	4.7μF, 0603/0805	1
C6,C5		Murata / Vishay	0.1μF, 0402/0603	2
C8	GRM39COG2R7C50	MuRata	2.7pF, 0402/0603	1
C9,C10	GRM39COG100D50	MuRata	10pF, 0402/0603	2
C2	GRM39X7R102K50	MuRata	(np)1nF, 0402/0603, not placed	1
JP1,JP2		Vishay	short, 0402/0603, 0Ω resistor	2
JP3,JP4			open, 0402/0603, not placed	2
J1			CON7	1
J2			(np)SMA, not placed	1
L1	0603CS-11NXGB	Coilcraft	11nH 2%, 0402/0603	1
L2	0603CS8N7XJB	Coilcraft	8.7nH 5%, 0402/0603	1
R1,R2			(np) 0402/0603, not placed	2
R3,R4		Vishay	100kΩ , 0402/0603	2
R5,R6, R7		Vishay	0Ω , 0402/0603	3
Y1	HC49	www.hib.com.br www.abracon.com	14.27643MHz Crystal, 10pF load,, 30ppm, -40 to +105 operating temperature	1
U1	MICRF221AYQS	Micrel Semiconductor	QSOP16	1

Table 8. QR221BPF Bill of Materials, 915.0 MHz

QR221BPF Bill of Materials, 916.5 MHz

Item	Part Number	Manufacturer	Description	Qty.
ANT1			50-Ω Ant78.7mm (3.1 inches) 20 AWG, rigid wire	1
C3	GRM39COG1R2C50	MuRata	1.2pF , 0402/0603	1
C4		Murata / Vishay	4.7μF, 0603/0805	1
C6,C5		Murata / Vishay	0.1μF, 0402/0603	2
C8	GRM39COG2R7C50	MuRata	2.7pF, 0402/0603	1
C9,C10	GRM39COG100D50	MuRata	10pF, 0402/0603	2
C2	GRM39X7R102K50	MuRata	(np)1nF, 0402/0603, not placed	1
JP1,JP2		Vishay	short, 0402/0603, 0Ω resistor	2
JP3,JP4			open, 0402/0603, not placed	2
J1			CON7	1
J2			(np)SMA, not placed	1
L1	0603CS-11NXGB	Coilcraft	11nH 2%, 0402/0603	1
L2	0603CS8N7XJB	Coilcraft	8.7nH 5%, 0402/0603	1
R1,R2			(np) 0402/0603, not placed	2
R3,R4		Vishay	100kΩ , 0402/0603	2
R5,R6, R7		Vishay	0Ω , 0402/0603	3
Y1	HC49	www.hib.com.br www.abracon.com	14.29983MHz Crystal, 10pF load,, 30ppm, -40 to +105 operating temperature	1
U1	MICRF221AYQS	Micrel Semiconductor	QSOP16	1

Table 9. QR221BPF Bill of Materials, 916.5 MHz

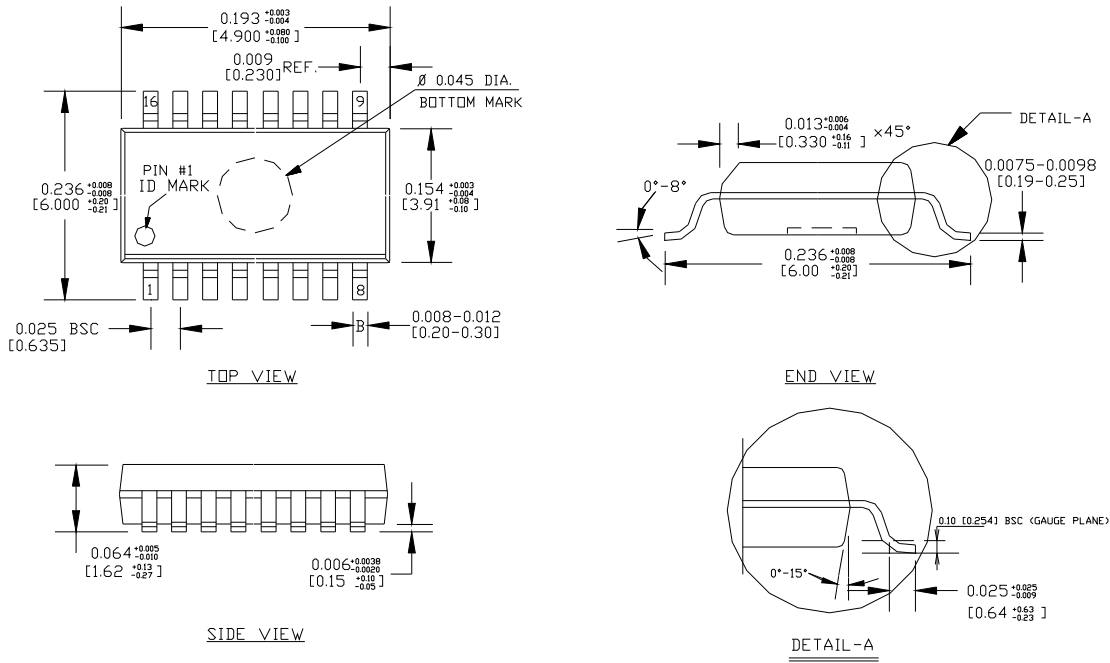
QR221BPF Bill of Materials, 868.35 MHz

Item	Part Number	Manufacturer	Description	Qty.
ANT1			50-Ω Ant83.8mm (3.3 inches) 20 AWG, rigid wire	1
C3	GRM39COG1R2C50	MuRata	1.2pF , 0402/0603	1
C4		Murata / Vishay	4.7μF, 0603/0805	1
C6,C5		Murata / Vishay	0.1μF, 0402/0603	2
C8	GRM39COG2R7C50	MuRata	2.7pF, 0402/0603	1
C9,C10	GRM39COG100D50	MuRata	10pF, 0402/0603	2
C2	GRM39X7R102K50	MuRata	(np)1nF, 0402/0603, not placed	1
JP1,JP2		Vishay	short, 0402/0603, 0Ω resistor	2
JP3,JP4			open, 0402/0603, not placed	2
J1			CON7	1
J2			(np)SMA, not placed	1
L1	0603CS-12NXGB	Coilcraft	12nH 2%, 0402/0603	1
L2	0603CS9N5XJB	Coilcraft	9.5nH 5%, 0402/0603	1
R1,R2			(np) 0402/0603, not placed	2

Item	Part Number	Manufacturer	Description	Qty.
R3,R4		Vishay	100k Ω , 0402/0603	2
R5,R6,R7		Vishay	0 Ω , 0402/0603	3
Y1	HC49	www.hib.com.br www.abracon.com	13.54856MHz Crystal, 10pF load,, 30ppm, -40 to +105 operating temperature	1
U1	MICRF221AYQS	Micrel Semiconductor	QSOP16	1

Table 8. QR221BPF Bill of Materials, 868.35 MHz

Package Information



- NOTE:
1. ALL DIMENSIONS ARE IN INCHES [MM].
 2. LEAD COPLANARITY SHOULD BE 0.004" [0.10 mm] MAX.
 3. MAX MISALIGNMENT BETWEEN TOP AND BOTTOM CENTER OF PACKAGE TO BE 0.004" [0.10 mm].
 4. THE LEAD WIDTH, B TO BE DETERMINED AT .0075 [0.19 mm] FROM THE LEAD TIP.
 5. BOTTOM MARK IS OPTIONAL, IT MAY NOT APPEAR ON THE ACTUAL UNITS.

QSOP16 Package Type (AQS16)

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
 TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB <http://www.micrel.com>

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