Preliminary

OKI Semiconductor

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MSM9563

IC for FM Multiplex Data Demodulation

GENERAL DESCRIPTION

The MSM9563 is an IC which demodulates FM character multiplex signals in the DARC (Data Radio Channel)*1 format to obtain digital data. The MSM9563 operates at 3 V.

The MSM9563 contains on one chip a band pass filter using a switched capacitor filter (SCF) and a group of circuits including frame memory, a frame synchronization circuit, and an error correction circuit.

By connecting an external FM receiver and memory for temporary data storage, and microcontroller, a system for obtaining digital data can easily be constructed.

The FM multiplex demodulation ICs, the MSM9500-series devices, are configured with minimum functions; so they will, by changing the software of the external microcontroller, be able to respond flexibly to the many FM multiplex broadcast services that are going to come about in the future.

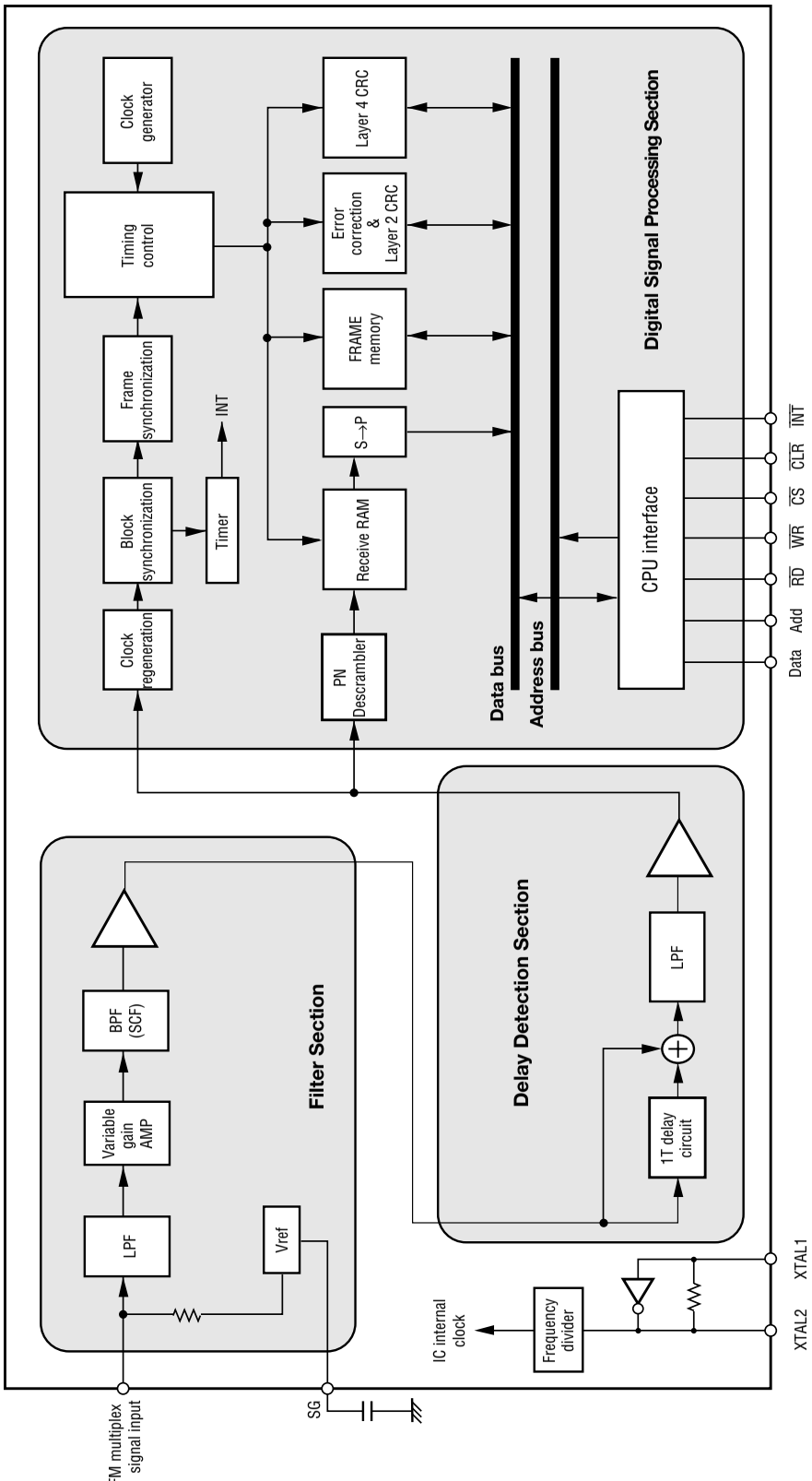
The MSM9563 is best suited to radios and information processing devices that support DARC FM multiplex broadcasting. It is also best suited to car radios and car navigation systems.

*1 DARC is a registered trademark of NHK Engineering Services.
Note that a contract needs to be made with NHK Engineering Service if a manufacturer produces/sells electronic equipment utilizing the DARC technology.

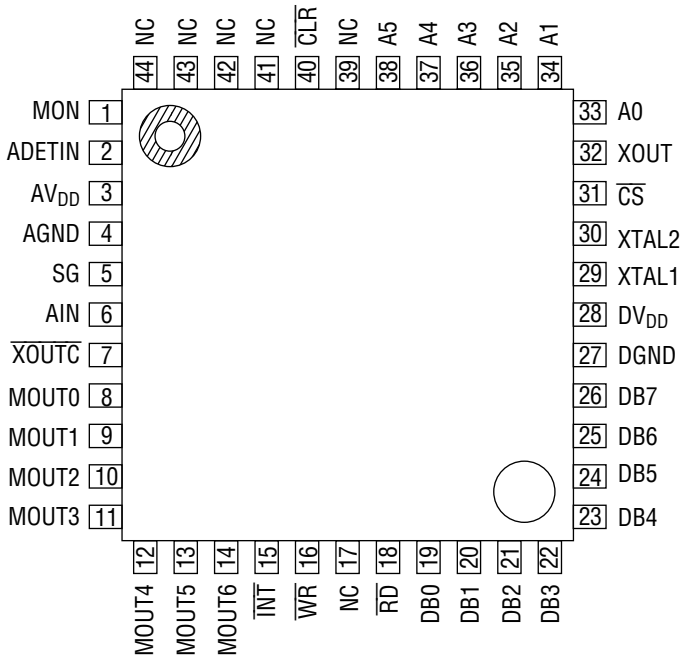
FEATURES

- Built-in two receive channels including main channel and sub-channel (one of two FM stations can be selected)
- Pin compatible with MSM9553/MSM9555
- Internal frame memory enables automatic error correction.
- Built-in bandpass filter (SCF)
- Built-in block synchronization circuit and frame synchronization circuit
- Setting of the number of synchronization protection steps can be changed.
- Data clocks are regenerated by digital PLL.
- 1T delay detection
- Built-in vertical and horizontal error correction circuits
- Built-in layer 4 and layer 2 CRC processing circuits
- Parallel interface with microcontroller
- Clock output for external devices (64 kHz to 8.192 MHz variable)
- Compatible with the international standard frame formats A (real time block also supported), B, C
- Power supply: 2.7 V to 3.6 V
- Package:
  44-pin plastic QFP (QFP44-P-910-0.80-2K) (Product name: MSM9563GA)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



NC : No-connection pin

44-Pin Plastic QFP

PIN DESCRIPTIONS

Function	Pin	Symbol	Type	Description
Microcontroller Interface	16	$\overline{WR}$	I	Write signal to internal register.
	18	$\overline{RD}$	I	Read signal to internal register.
	15	$\overline{INT}$	O	Interrupt signal to microcontroller. "L": An interrupt is generated.
	31	$\overline{CS}$	I	Chip select signal. "L": Read, write, and data bus signals become active.
	40	$\overline{CLR}$	I	"L" : the internal registers are initialized and the device enters power down mode.
	33 to 38	A0 to A5	I	Address signal to internal register.
	19 to 26	DB0 to DB7	I/O	Data bus signal to internal register.
Tuner Interface	6	AIN	I	FM multiplex signal input.
	5	SG	O	Analog reference voltage output pin. Connect a capacitor between this pin and analog ground to prevent noise.
Analog Section Test	1	MON	O	Analog section waveform monitoring pin. The analog block mode setting is specified by the analog control register.
	2	ADETIN	I	Digital signal input pin for testing analog section.
Digital Section Test	8 to 14	MOUT0 to MOUT6	O	Digital section test signal output and monitor output pins.
Clock	29	XTAL1	I	8.192 MHz crystal connection pin.
	30	XTAL2	O	8.192 MHz crystal connection pin.
	32	XOUT	O	Pin for supply of 64 kHz to 8.192 MHz variable clock to the outside.
	7	$\overline{XOUTC}$	I	XOUT output control pin. "L" = Clock output, "H" = Output disabled. Pulled up internally.
Power Supply	3	AV_{DD}	—	Analog section power supply pin.
	4	AGND	—	Analog ground pin.
	28	DV_{DD}	—	Digital section power supply pin.
	27	DGND	—	Digital ground pin.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	AV_{DD}	$AV_{DD} = DV_{DD}$ Ta = 25°C	–0.3 to +7.0	V
	DV_{DD}			
Input Voltage	V_I		–0.3 to AV_{DD} + 0.3	
Output Voltage	V_O		–0.3 to DV_{DD} + 0.3	
Maximum Power Dissipation	P_D	Ta = 25°C, per package	400	mW
		Ta = 25°C, per output	50	
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit	Applied Pin
Power Supply Voltage	AV_{DD}	$AV_{DD} = DV_{DD}$	2.7 to 3.6	V	AV_{DD}
	DV_{DD}				DV_{DD}
Crystal Oscillation Frequency	f_{XTAL}	—	8.192 MHz ±100 ppm	—	XTAL1, XTAL2
FM Multiplex Signal Input Voltage	V_{AIN}*	Variable amplifier gain: × 1	0.6 to 0.9	V_{P-P}	AIN
		Variable amplifier gain: × 1.5	0.4 to 0.6		
		Variable amplifier gain: × 2	0.3 to 0.4		
		Variable amplifier gain: × 3	0.2 to 0.3		
Operating Temperature	T_{op}	—	–40 to +85	°C	—

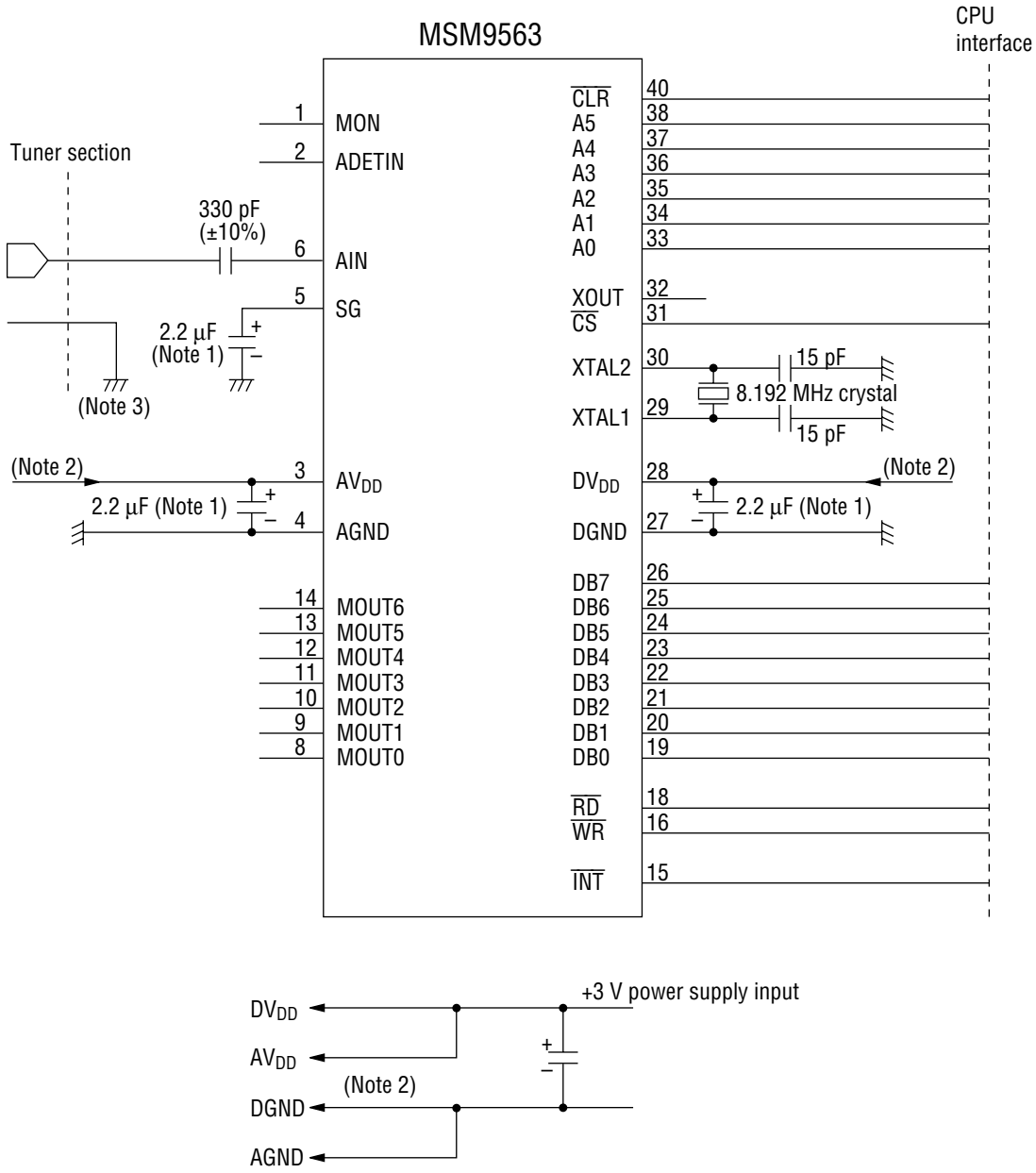
* Peak values (a total voltage of the following signals (a) to (c)) of composite signals including multiplex signals.
(a) Voice signals (100% modulated: voice max.)
(b) Pilot signal
(c) FM multiplex signals (10%: LMSK max.)
The maximum amplitude of an input signal is in the range of 0.9 V_{P-P} in which the internal IC circuit is not saturated.
Therefore, multiplex signals of up to 0.9 V_{P-P} can be input if only multiplex signals (excluding composite signals) are input from a signal generator.

ELECTRICAL CHARACTERISTICS

(DV_{DD} = AV_{DD} = 2.7 to 3.6 V, DGND = AGND = 0 V, Ta = –40 to +85°C)

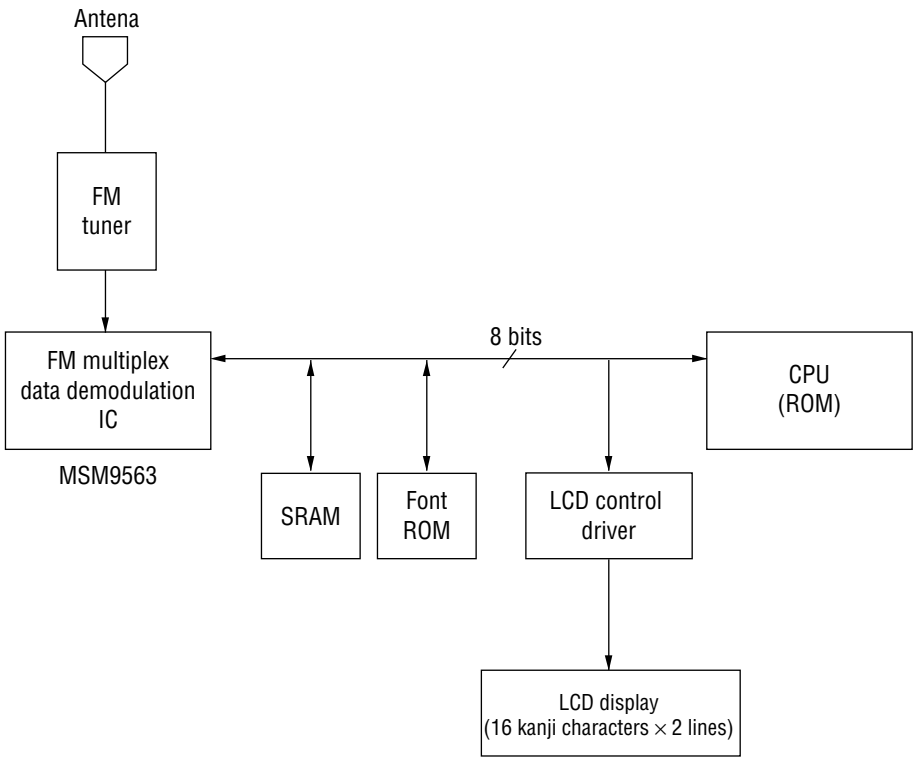
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applied Pin
Supply Current	I_{DD}	When operating, no load f = 8.192 MHz	—	14	28	mA	AV_{DD}, DV_{DD}
		When in power down mode, no load	—	—	50	μA	
BPF Pass Band Attenuation	GAIN1	72 to 80 kHz Variable gain amplifier gain: 0 dB	—	—	3.0	dB	MON
BPF Stop Band Attenuation	GAIN2	0 to 53 kHz Variable gain amplifier gain: 0 dB	50	—	—	dB	MON
BPF Stop Band Attenuation	GAIN3	100 to 500 kHz Variable gain amplifier gain: 0 dB	50	—	—	dB	MON

EXTERNAL CONNECTION EXAMPLE



(Note 1) Use a tantalum capacitor.
(Note 2) The AV_{DD} and DV_{DD} should have different paths, respectively.
(Note 3) The AGND and tuner ground should use the same ground.

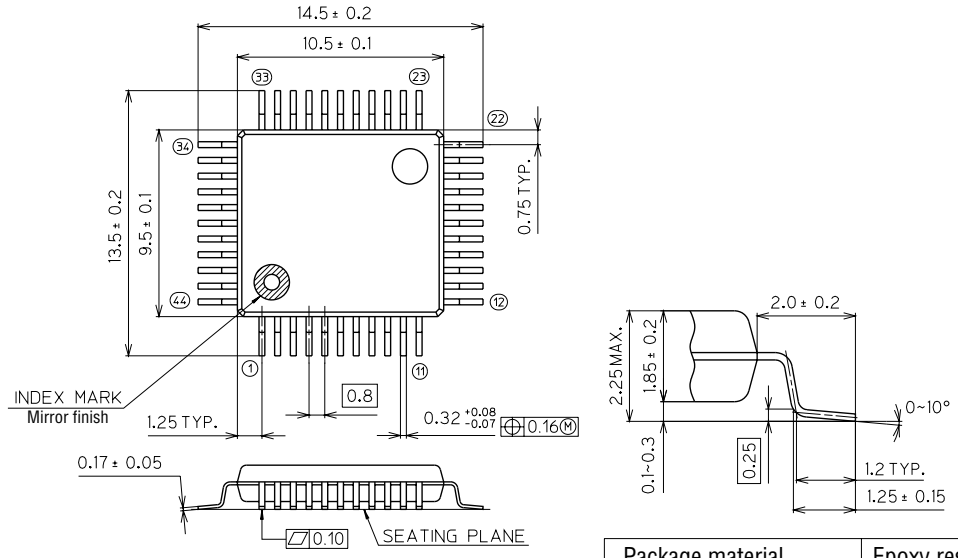
APPLICATION CIRCUIT EXAMPLE



PACKAGE DIMENSIONS

(Unit : mm)

QFP44-P-910-0.80-2K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.41 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ, QFJ (PLCC), SHP, and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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