OKI Semiconductor

This version: Sep. 2000
Previous version: Nov. 1997

MSM9005-xx

DOT MATRIX LCD CONTROLLER WITH 8-DOT COMMON DRIVER AND 65-DOT SEGMENT DRIVER

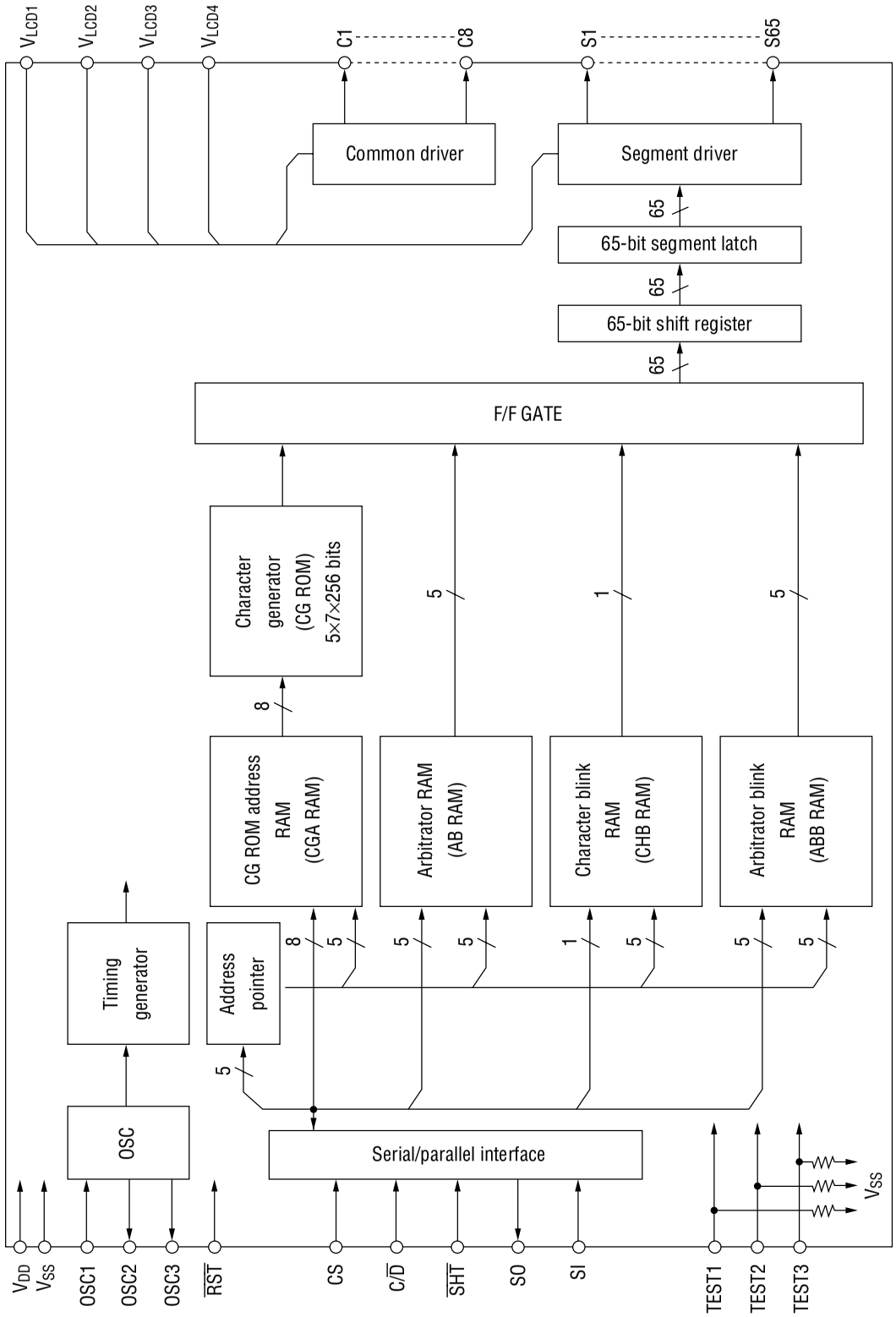
GENERAL DESCRIPTION

The MSM9005-xx is a controller / driver which displays 13 alphanumerics and symbols (5x7 dots) and 65 arbitrators on a dot matrix LCD panel that has 8 common inputs and 65 segment inputs. Command and display data are written by 8-bit serial transfer.
A maximum of 256 types of alphanumerics and symbols can be displayed using an internal character display ROM. The character display ROM is reprogrammable. The general purpose code is -01.

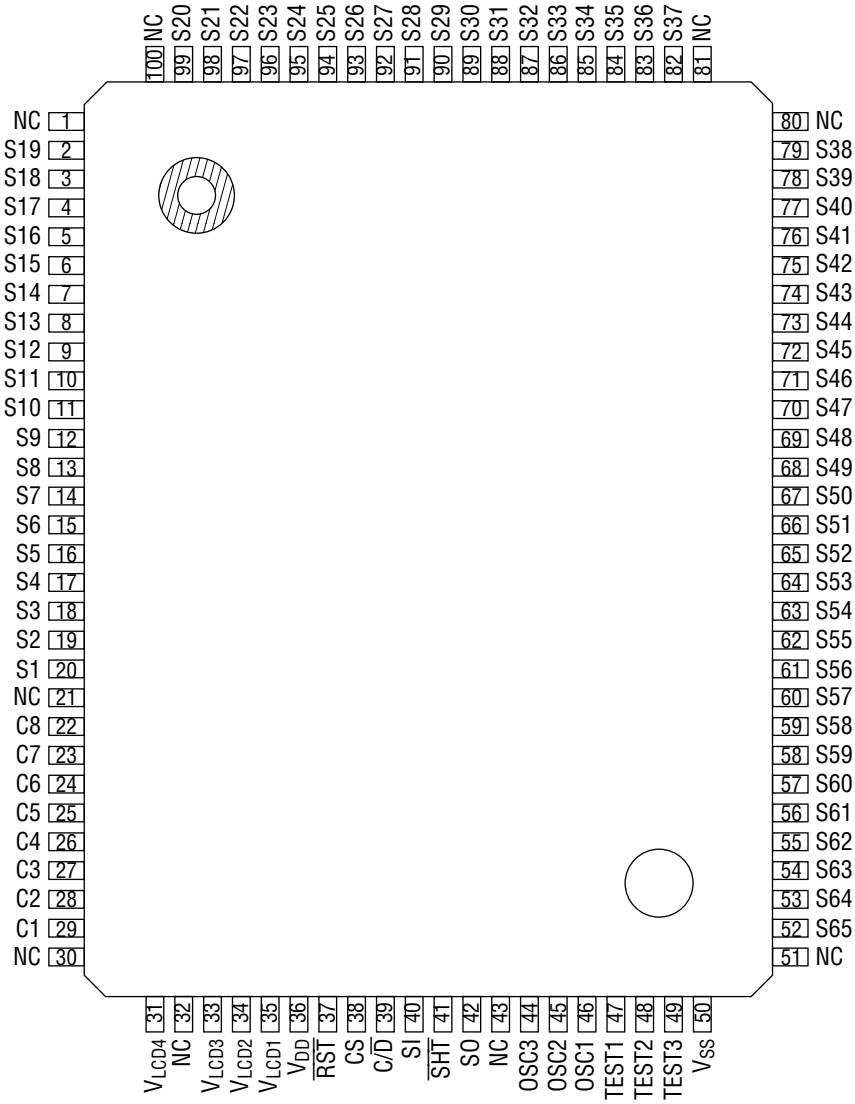
FEATURES

- Logic power supply (V_{DD}) : 2.5 to 5.5V
- LCD bias power supply (V_{BI}) : 4.0 to 8.0V
- LCD output resistance
  - Common driver (C1 to C8) : 6 kΩ
  - Segment driver (S1 to S65) : 18 kΩ
- Display content
  - Number of display characters : 13 characters, 1 line
  - Arbitrator : 65 dots
- Display control functions
  - Character blink : Characters all on or all off can be selected
  - Arbitrator blink : 1-dot unit or 5-dot units can be selected
  - All off setting possible
- 5 interfaces with microcomputer, CS, SI, SO, C/$\overline{D}$ and $\overline{SHT}$ (6 interfaces if $\overline{RST}$ is included)
- Internal character display ROM : 5 × 7 dots × 256 types (reprogrammable)
- Internal oscillation circuit : External R, C
- Package:
  100-pin plastic QFP (QFP 100-P-1420-0.65-BK) (Product name: MSM9005-xxGS-BK)
  xx indicates code number.

BLOCK DIAGRAM



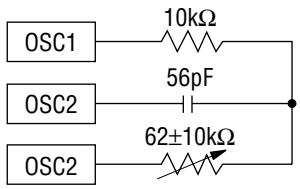
PIN CONFIGURATION (TOP VIEW)



NC : No connection

100-Pin Plastic QFP

PIN DESCRIPTIONS

Pin	Symbol	Type	Connected to	Description
2 to 20, 52 to 79 82 to 99	S1 to S65	O	LCD segment	LCD segment outputs. Output resistance: ≤18 kΩ
22 to 29	C1 to C8	O	LCD common	LCD common outputs. Output resistance: ≤6kΩ
40	SI	I	Microcontroller	Serial data input. Serial data is input through this pin in 8-bit units from the MSB side. For details on the configuration of input data, see "Command Configuration" and "Input Display Data Configuration".
39	C/$\overline{D}$	I	Microcontroller	Command/data select input. When this pin is at the "H" level, serial input data from SI is recognized as a command. When this pin is at the "L" level, serial input data from SI is recognized as display data.
41	$\overline{SHT}$	I	Microcontroller	Shift clock input. Data at SI and C/$\overline{D}$ pins are read synchronizing with the rising edge of this clock. Display data is output to the S0 pin synchronizing with the falling edge of this clock.
42	SO	I	Microcontroller	Serial data output. This pin outputs display data. For details on the configuration of output data, see "Output Display Data Configuration". This pin can be set to high impedance by the SOE/D command.
38	CS	I	Microcontroller	Chip select input. When this pin is at the "H" level, chip is selected, and command and display data can be transferred. When this pin is at the "L" level, SO output is set to high impedance, $\overline{SHT}$ input is set to the "H" level, and SI and C/$\overline{D}$ inputs are set to the "L" level, and command and display data transfer are disabled.
37	$\overline{RST}$	I	Microcontroller	Reset input. Setting this pin at the "L" level resets to initial status.
47 48 49	TEST1 TEST2 TEST3	I	—	Test signal inputs. Set these pins to the same potential as V_{SS} or unconnected. An error may occur by another setting.
46 45 44	OSC1 OSC2 OSC3	I O O	—	Pins for an 80 kHz RC oscillation circuit. Connect resistors and a capacitor as shown below. 

Pin	Symbol	Type	Connected to	Description
36 50	V_{DD} V_{SS}	—	—	These are power pins. Set V_{DD} = 2.5 to 5.5V and V_{SS} = 0V.
35 34 33 31	V_{LCD1} V_{LCD2} V_{LCD3} V_{LCD4}	—	—	These are bias power pins for driving the LCD. Set the bias voltage as follows. $4\ V \leq V_{DD} - V_{LCD4} \leq 8\ V$ $V_{LCD1}=V_{DD}-\frac{1}{4}(V_{DD}-V_{LCD4})$ $V_{LCD2}=V_{DD}-\frac{2}{4}(V_{DD}-V_{LCD4})$ $V_{LCD3}=V_{DD}-\frac{3}{4}(V_{DD}-V_{LCD4})$

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta=25°C	–0.3 to +7.0	V
Bias Voltage	V_{BI}	Ta=25°C	V_{DD}–10 to V_{DD}+0.3	V
Input Voltage	V_I	Ta=25°C	–0.3 to V_{DD}+0.3	V
	V_{ILCD}	Ta=25°C	V_{BI}–0.3 to V_{DD}+0.3	V
Power Dissipation	P_D	Ta=85°C	620	mW
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Power Supply Voltage	V_{DD}	*1	2.5 to 5.5	V
Bias Voltage	V_{BI}	*1, *2	V_{DD}–8.0 to V_{DD}–4.0	V
Operating Frequency	f_{op}	—	60 to 110	kHz
Operating Temperature	T_{op}	—	–40 to +85	°C

*1: Voltage values are with respect to V_{SS}.

*2: Add the following voltages to V_{LCD1}, V_{LCD2}, V_{LCD3} and V_{LCD4}, respectively.

$$V_{LCD1}=V_{DD}-\frac{1}{4}(V_{DD}-V_{BI})$$

$$V_{LCD2}=V_{DD}-\frac{2}{4}(V_{DD}-V_{BI})$$

$$V_{LCD3}=V_{DD}-\frac{3}{4}(V_{DD}-V_{BI})$$

$$V_{LCD4}=V_{DD}-\frac{4}{4}(V_{DD}-V_{BI})=V_{BI}$$

ELECTRICAL CHARACTERISTICS

DC Characteristics (1)

(Ta=–40 to +85°C, V_{DD}=2.5 to 4.5V, V_{BI}=(V_{DD}–8V) to (V_{DD}–4V))

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
"H" Input Voltage	V_{IH1}	—	0.8V_{DD}	—	V_{DD}	V	Input pins other than OSC1
	V_{IH2}	—	0.8V_{DD}	—	V_{DD}	V	OSC1
"L" Input Voltage	V_{IL1}	—	0.0	—	0.2V_{DD}	V	Input pins other than OSC1
	V_{IL2}	—	0.0	—	0.2V_{DD}	V	OSC1
"H" Input Current	I_{IH1}	V_{IN}=V_{DD}	—	—	1	µA	Input pins other than TEST
	I_{IH2}	V_{DD}, V_{IN}=2.5V	5	—	500	µA	TEST
"L" Input Current	I_{IL}	V_{IN}=0V	—	—	–1	µA	All input pins
"H" Output Voltage	V_{OH}	I_{OH}=–0.5mA	V_{DD}–0.5	—	—	V	SO
"L" Output Voltage	V_{OL}	I_{OL}=0.5mA	—	—	0.5	V	
Output Off Leakage Current	I_{OFF}	V_{IN}=V_{DD}	—	—	1	µA	
		V_{IN}=0V	—	—	–1	µA	
OSC "H" Output Current	I_{OH}	V_{OH}=V_{DD}–0.5V	—	—	–0.15	mA	OSC2, OSC3
OSC "L" Output Current	I_{OL}	V_{OL}=0.5V	0.15	—	—	mA	
COM Output Resistance	R_C	I_O=+/–50µA	—	—	6	kΩ	C1 to C8
SEG Output Resistance	R_S	I_O=+/–10µA	—	—	18	kΩ	S1 to S65
Supply Current	I_{SS}	V_{DD}=2.5V, V_{BI}=V_{DD}–8V, f_{OSC}=80kHz (External resistor, capacitor) C=56pF, R_S=10kΩ, R=66kΩ	—	—	0.2	mA	V_{SS}
	I_{BI}		—	—	50	µA	V_{LCD4}

DC Characteristics (2)

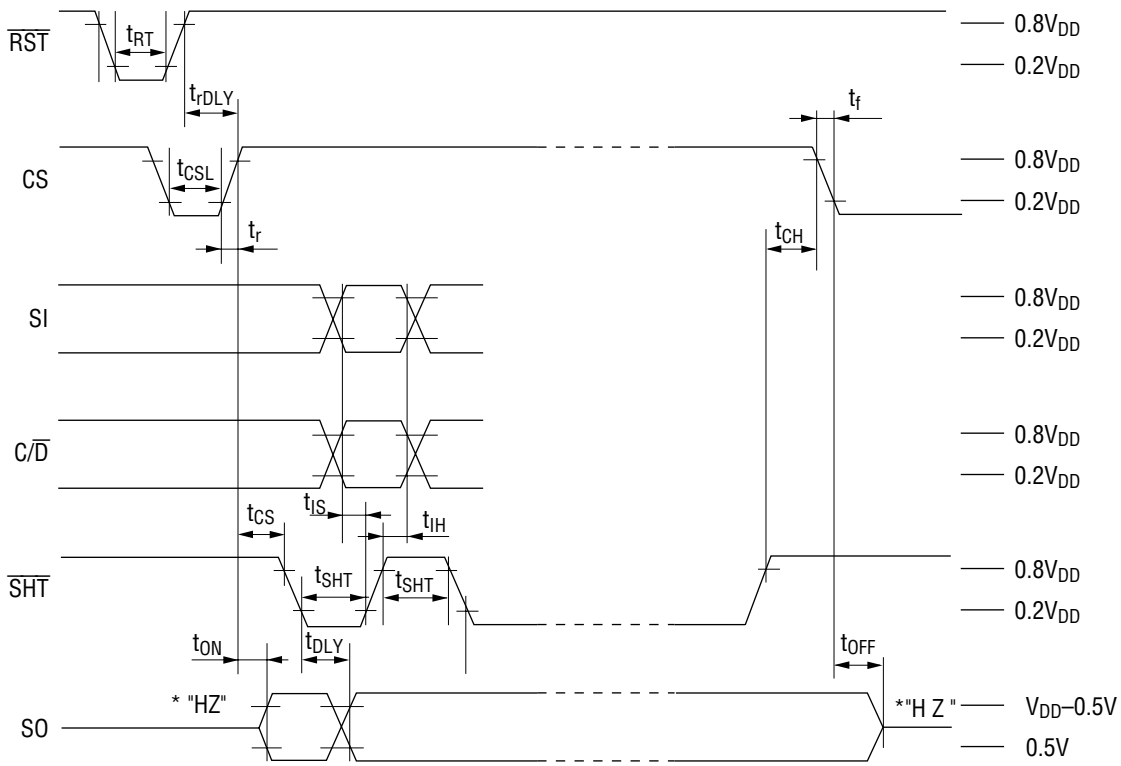
(Ta=–40 to +85°C, V_{DD}=4.5 to 5.5V, V_{BI}=(V_{DD}–8V) to (V_{DD}–4V))

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
"H" Input Voltage	V_{IH1}	—	0.8V_{DD}	—	V_{DD}	V	Input pins other than OSC1
	V_{IH2}	—	0.8V_{DD}	—	V_{DD}	V	OSC1
"L" Input Voltage	V_{IL1}	—	0.0	—	0.2V_{DD}	V	Input pins other than OSC1
	V_{IL2}	—	0.0	—	0.2V_{DD}	V	OSC1
"H" Input Current	I_{IH1}	V_{IN}=V_{DD}	—	—	1	µA	Input pins other than TEST
	I_{IH2}	V_{DD}, V_{IN}=5.5V	5	—	1000	µA	TEST
"L" Input Current	I_{IL}	V_{IN}=0V	—	—	–1	µA	All input pins
"H" Output Voltage	V_{OH}	I_{OH}=–0.5mA	V_{DD}–0.5	—	—	V	SO
"L" Output Voltage	V_{OL}	I_{OL}=0.5mA	—	—	0.5	V	
Output Off Leakage Current	I_{OFF}	V_{IN}=V_{DD}	—	—	1	µA	
		V_{IN}=0V	—	—	–1	µA	
OSC "H" Output Current	I_{OH}	V_{OH}=V_{DD}–0.5V	—	—	–0.15	mA	OSC2, OSC3
OSC "L" Output Current	I_{OL}	V_{OL}=0.5V	0.15	—	—	mA	
COM Output Resistance	R_C	I_O=+/–50µA	—	—	6	kΩ	C1 to C8
SEG Output Resistance	R_S	I_O=+/–10µA	—	—	18	kΩ	S1 to S65
Supply Current	I_{SS}	V_{DD}=5.5V, V_{BI}=V_{DD}–8V, f_{OSC}=80kHz (External resistor, capacitor) C=56pF, R_S=10kΩ, R=66kΩ	—	—	0.8	mA	V_{SS}
	I_{BI}		—	—	50	µA	V_{LCD4}

AC Characteristics

(Ta=–40 to +85°C, V_{DD}=2.5 to 5.5V, V_{BI}=(V_{DD}–8V) to (V_{DD}–4V))

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CS Setup Time	t_{CS}	—	300	—	—	ns
CS Hold Time	t_{CH}	—	200	—	—	ns
CS "L" Time	t_{CSL}	—	500	—	—	ns
SO ON Delay Time	t_{ON}	C_L=45pF	—	—	200	ns
SO OFF Delay Time	t_{OFF}	C_L=45pF	—	—	200	ns
SO Output Delay Time	t_{DLY}	C_L=45pF	0	—	200	ns
Input Setup Time	t_{IS}	—	200	—	—	ns
Input Hold Time	t_{IH}	—	200	—	—	ns
Input Rise, Fall Time	t_r/t_f	All inputs	—	—	50	ns
$\overline{RST}$ Pulse Width	t_{RT}	—	5	—	—	µs
Wait Time After $\overline{RST}$ Pulse	t_{rDLY}	—	500	—	—	ns
$\overline{SHT}$ Frequency	f_{SHT}	—	—	—	2	MHz
$\overline{SHT}$ Pulse Width	t_{SHT}	—	200	—	—	ns



* "HZ" : High impedance.

FUNCTIONAL DESCRIPTION

General Description of Block Diagram

1. Address Pointer
   An address pointer is a 5-bit counter which assigns the write destination or read destination address of CGA RAM and AB RAM, and the write destination address of CHB RAM and ABB RAM. The value of the address pointer can be set by the LPA command. The value of the address pointer is automatically incremented by 1 after executing the AINC and CHB commands, or after transferring input display data.

2. Character Generator Address RAM (CGA RAM)
   The character generator address RAM stores 8-bit character codes of the character generator ROM. A maximum of thirteen 8-bit character codes can be stored.

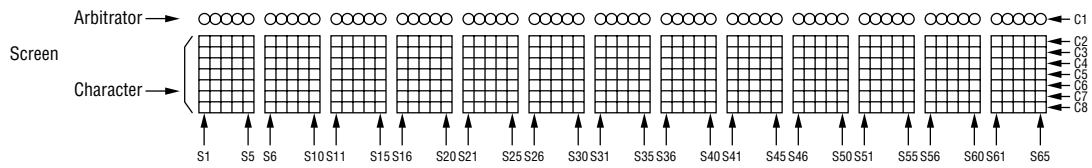
3. Arbitrator RAM (AB RAM)
   The arbitrator RAM stores the lighting data of the arbitrator. Lighting data is stored in 5 dot units, and a maximum of 65 dots of lighting data can be stored.

4. Character Blink RAM (CHB RAM)
   The character blink RAM stores character blink data. A maximum of 13 characters of blink data can be stored.

5. Arbitrator Blink RAM (ABB RAM)
   The arbitrator blink RAM stores blink data of the arbitrator. Blink data is stored in 5 dot units, and a maximum of 65 dots of blink data can be stored.

6. Character Generator ROM (CG ROM)
   The character generator ROM generates character patterns with 5×7 dots. This ROM can store a maximum of 256 types of characters, numerics, and symbols.
   When an 8-bit character code of CG ROM is written to CGA RAM, character patterns with 5 × 7 dots corresponding to 8-bit character code are displayed at the LCD display position corresponding to the CGA RAM address.

Relationship between display screen, LCD output and memory address



RAM Address map													
Arbitrator	10000b	10001b	10010b	10011b	10100b	10101b	10110b	10111b	11000b	11001b	11010b	11011b	11100b
Character	00000b	00001b	00010b	00011b	00100b	00101b	00110b	00111b	01000b	01001b	01010b	01011b	01100b

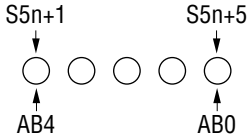
Command Configuration

	Command		MSB Input data LSB								Comment
	Mnemonic	Operation	D7	D6	D5	D4	D3	D2	D1	D0	
1	LPA	Load Pointer Address	1	1	*	A4	A3	A2	A1	A0	Sets address pointer value A0, A1, A2, A3 A4: address pointer value (binary)
2	DISP	DISPlay on/off	1	0	0	*	1	0	0	DI	Sets on/off of LCD panel Panel is on when DI = "1" Panel is off when DI = "0"
3	CHB	CHaracter Blink on/off	0	*	*	*	0	0	CB	*	Sets blink in 5 dot units Blink starts in 5 dot units when CB = "1" Blink is cleared when CB = "0"
4	ABBC 1/5	ArBitrator Blink Control 1/5 dot	1	0	0	1	1	1	0	BC	Sets writing method to arbitrator blink RAM Writing in 1 dot unit is enabled when BC = "1" Writing in 5 dot unit is enabled when BC = "0"
5	ABB	ArBitrator Blink	1	0	0	0	1	1	0	AB	Sets start/stop of writing to arbitrator blink RAM Writing in 1 dot unit starts when AB = "1" Writing in 1 dot unit stops when AB = "0"
6	BPC	Blink Pattern Control	1	0	0	*	0	0	1	BP	Sets blink pattern of characters When BP = 1, all off ↔ character blink When BP = 0, all on ↔ character blink
7	AINC	Address INCrement	1	0	0	*	1	*	1	*	Increments address pointer value by 1
8	LOT	Load OpTion	1	0	1	1	*	*	I1	I0	Sets additional function of AINC command
9	SOE/D	Serial Out Enable/Disable	1	0	0	*	0	1	1	S	Set SO pin SO pin is a CMOS output when S = "1" SO pin is in a high impedance state when S = "0"

*: Don't care

The commands listed above requires the wait time ($21 \times 1/f_{OSC}$).
The address pointer value is incremented by 1 when CG ROM code data, arbitrator display data and arbitrator blink data are input and when AINC and CHB commands are executed.

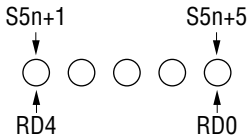
Input Display Data Configuration

	Command	MSB Input data LSB								Comment
		D7	D6	D5	D4	D3	D2	D1	D0	
1	CG ROM code data	C7	C6	C5	C4	C3	C2	C1	C0	C0 to C7: CG ROM address
2	Arbitrator display data	*	*	*	AB4	AB3	AB2	AB1	AB0	Relationship between AB0 to AB4 and segments pins is as follows. 
3	Arbitrator blink data	*	*	*	AB4	AB3	AB2	AB1	AB0	

*: Don't care

n = 0 to 12

Output Display Data Configuration

	Command	MSB Input data LSB								Comment
		D7	D6	D5	D4	D3	D2	D1	D0	
1	CG ROM code data	C7	C6	C5	C4	C3	C2	C1	C0	C0 to C7: CG ROM address
2	Arbitrator display data	0	0	0	RD4	RD3	RD2	RD1	RD0	Relationship between RD0 to RD4 and segment pins is as follows. 

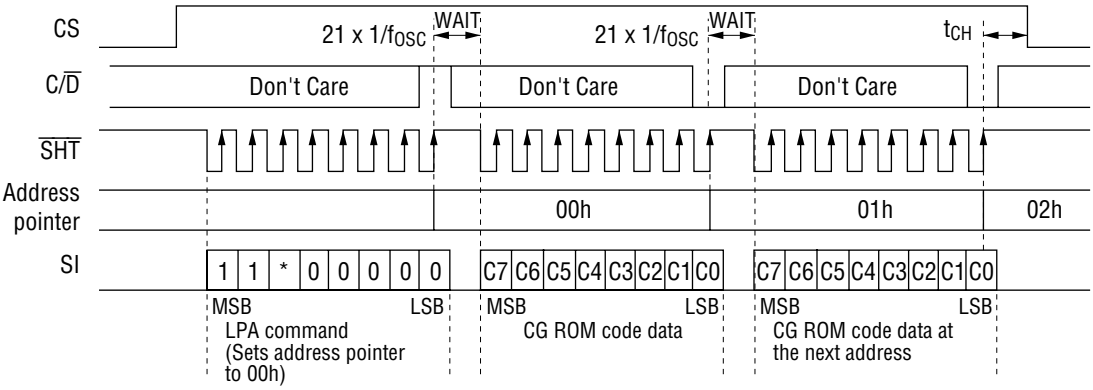
n = 0 to 12

How to Write Command and Display Data

- Input a command and display data into the SI pin sequentially from MSB in 8-bit units (MSB first).
- Setting CS pin at "H" level enables transfer of a command and display data.
- Setting CS pin at a "L" level disables data transfer.
- As shown in the figure below, data is shifted at the rising edge of the shift clock that is input to the $\overline{SHT}$ pin. When 8 shift clocks are input, internal load signals are automatically generated and a command or display data is loaded. It is unnecessary to provide load signals externally.
- Loaded 8-bit data is recognized as a command if the C/$\overline{D}$ pin is set at "H" level, and is recognized as display data if the C/$\overline{D}$ pin is set at "L" level on the rising edge of the 8th shift clock input to the $\overline{SHT}$ pin.

Write timing is shown below.

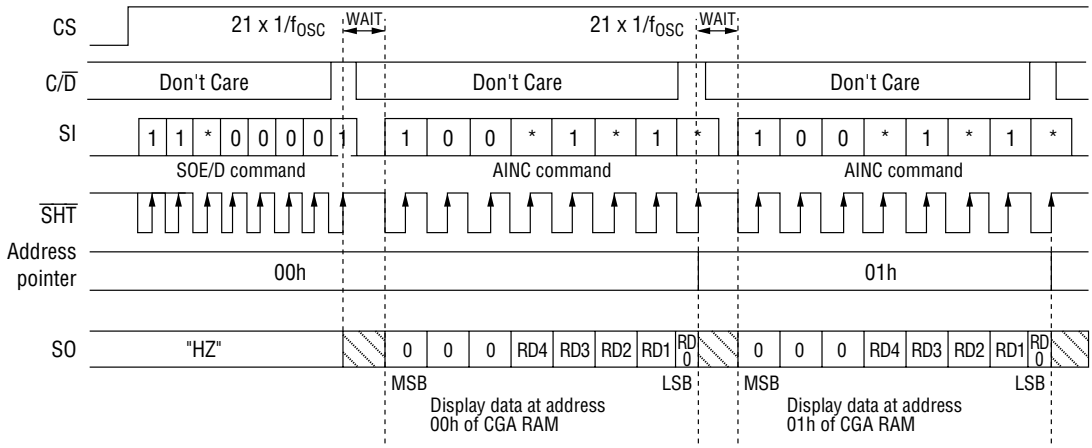
(Example) Writing CG ROM address data The wait time of $21 \times 1/f_{OSC}$ is required



How to Read Display Data

- Display data is output sequentially from MSB in 8-bit units (MSB first).
- Setting S = "1" by the SOE/D command after setting the CS pin at "H" level enables the output of display data from the SO pin.
- Setting the CS pin at "L" level or setting S = "0" by the SOE/D command sets the SO pin to high impedance and disables output of display data.
- CGARAM or ABRAM data corresponding to the address pointer value is output.
- Display data is output from MSB on the falling edge of the shift clock that is input to the $\overline{SHT}$ pin, as shown in the figure below.
  Read timing is shown below.

(Example) Reading by AINC command The wait time of $21 \times 1/f_{OSC}$ is required



Reset Function

Reset is enabled when the $\overline{RST}$ pin is set at "L" level at such timing as at power-on, which initializes all functions and turns off the LCD panel.

The initial state after reset is as follows.

Data of each RAM ..... All contents are held. (Contents are undefined when power is turned on.)

Arbitrator blink ..... Writing in 5 dot units is set.

Character blink ..... Repeat of all display-on and character display is set.

Display on and
all display off ..... All display off mode is selected.

Segment output ..... All segment outputs go to V_{DD} level.

Common output ..... All common outputs go to V_{DD} level.

SO pin ..... High impedance state

Command Description

1. Load pointer address command (LPA command)
   This command is used to set the value of the address pointer. Execute this command before transferring other commands, CG ROM code data and arbitrator display data.
   After this command is executed, setting the C/$\overline{D}$ pin from "1" to "0" enables writing CG ROM code data to CG ROM address RAM (CGA RAM) and arbitrator display data to arbitrator RAM (ABRAM). After CG ROM code data or arbitrator display data is transferred, the address pointer is automatically incremented (+1), and CG ROM code data and arbitrator display data can be transferred continuously.

[How to transfer LPA command and CG ROM code data]

LPA command

D8	D7	D6	D5	D4	D3	D2	D1
1	1	*	0	0	0	0	0

*: Don't care

Specify address pointer value
(Example: Set address pointer value to 00H.)

CG ROM code data

D8	D7	D6	D5	D4	D3	D2	D1
C7	C6	C5	C4	C3	C2	C1	C0

CG ROM code data is written to CGA RAM address 00H, and the character corresponding to the specified CG ROM code is displayed in segments 1 to 5.
After this data transfer is executed, the address pointer value becomes 01H.

CG ROM code data

D8	D7	D6	D5	D4	D3	D2	D1
C7	C6	C5	C4	C3	C2	C1	C0

CG ROM code data is written to CGA RAM address 01H, and the character corresponding to the specified CG ROM code is displayed at segments 6 to 10.
After this data transfer is executed, the address pointer value becomes 02H.

CG ROM code data

D8	D7	D6	D5	D4	D3	D2	D1
C7	C6	C5	C4	C3	C2	C1	C0

CG ROM code data is written to CGA RAM address 02H, and the character corresponding to the specified CG ROM code can be displayed at segments 11 to15.
After this data transfer is executed, the address pointer value becomes 03H.

(Repeats eight times.)

CG ROM code data

D8	D7	D6	D5	D4	D3	D2	D1
C7	C6	C5	C4	C3	C2	C1	C0

CG ROM code data is written to CGA RAM address 0BH, and the character corresponding to the specified CG ROM code can be displayed at segments 56 to 60.
After this data transfer is executed, the address pointer value becomes 0CH.

CG ROM code data

D8	D7	D6	D5	D4	D3	D2	D1
C7	C6	C5	C4	C3	C2	C1	C0

CG ROM code data is written to CGA RAM address 0CH, and the character corresponding to the specified CG ROM code can be displayed at segments 61 to 65.
After this data transfer is executed, the address pointer value becomes 0DH.

CG ROM code data

D8	D7	D6	D5	D4	D3	D2	D1
C7	C6	C5	C4	C3	C2	C1	C0

CGA RAM address is only 00H to 0CH. **The address pointer value becomes 0DH. However, this CG ROM data is ignored.**

[How to transfer LPA command and arbitrator display data]

LPA command

D8	D7	D6	D5	D4	D3	D2	D1
1	1	*	1	0	0	0	0

Specify address pointer value
(Example: Set address pointer value to 10H.)

Arbitrator display data

D8	D7	D6	D5	D4	D3	D2	D1
*	*	*	A4	A3	A2	A1	A0

Arbitrator display data is written to AB RAM address 10H, and the specified arbitrator of segments 1 to 5 can be displayed.
After this data transfer is executed, the address pointer value becomes 11H.

Arbitrator display data

D8	D7	D6	D5	D4	D3	D2	D1
*	*	*	A4	A3	A2	A1	A0

Arbitrator display data is written to AB RAM address 11H, and the specified arbitrator of segments 6 to 10 can be displayed.
After this data transfer is executed, the address pointer value becomes 12H.

Arbitrator display data

D8	D7	D6	D5	D4	D3	D2	D1
*	*	*	A4	A3	A2	A1	A0

Arbitrator display data is written to AB RAM address 12H, and the specified arbitrator of segments 11 to 15 can be displayed.
After this data transfer is executed, the address pointer value becomes 13H.

(Repeats eight times.)

Arbitrator display data

D8	D7	D6	D5	D4	D3	D2	D1
*	*	*	A4	A3	A2	A1	A0

Arbitrator display data is written to AB RAM address 1BH, and the specified arbitrator of segments 59 to 60 can be displayed.
After this data transfer is executed, the address pointer value becomes 1CH.

Arbitrator display data

D8	D7	D6	D5	D4	D3	D2	D1
*	*	*	A4	A3	A2	A1	A0

Arbitrator display data is written to AB RAM address 1CH, and the specified arbitrator of segments 61 to 65 can be displayed.
After this data transfer is executed, the address pointer value becomes 1DH.

Arbitrator display data

D8	D7	D6	D5	D4	D3	D2	D1
*	*	*	A4	A3	A2	A1	A0

AB RAM address is only 10H to 1CH. **The address pointer value becomes 1DH. However, this arbitrator display data is ignored.**

*: Don't care

2. Display on/off command (DISP command)
   This command is used to select LCD panel display-on mode and display-off mode. Setting DI = "0" enters display-off mode. At this time, the output voltage of all segments and common output pins go to V_{DD} level and the LCD panel goes out. Setting DI = "1" enters display-on mode. At this time, the LCD panel restarts the status display before entering display-off mode.

[DISP command format]

	D8	D7	D6	D5	D4	D3	D2	D1	
DISP command	1	0	0	*	1	0	0	DI	Display-off mode is set when DI = "0" Display-on mode is set when DI = "1"

*: Don't care

3. Arbitrator Blink Control 1/5 command (ABBC 1/5 command)
   This command is used to select the type of writing arbitrator blink data to the Arbitrator Blink RAM (ABB RAM). This command is used along with the Character Blink on/off command or with the Arbitrator Blink command, explained below.

   Setting BC = "0" enables writing arbitrator blink data in 5-bit units using the CHB command.
   Setting BC = "1" enables writing arbitrator blink data in 1 bit unit using the ABB command.

[ABBC 1/5 command format]

	D8	D7	D6	D5	D4	D3	D2	D1	
DISP command	1	0	0	1	1	1	0	BC	BC = "0" enables writing in 5-bit unit. BC = "1" enables writing in 1-bit unit.

4. Character Blink on/off command (CHB command)
   This command is used to blink a character and arbitrator in 5-dot units. Blinking can be set for each address pointer value. This command is used with the ABBC 1/5 command, explained above.

   If CB = "0" is set when the address pointer value is 00H to 0CH, "0" is written to Character Blink RAM (CHB RAM), and the blinking of a character displayed in the segments corresponding to the address pointer value stops. If CB = "1" is set, "1" is written to CHB RAM, and the character displayed in the segments corresponding to the address pointer value starts blinking.
   If CB = "0" is set when the address pointer value is 10H to 1CH, "0" is written to the arbitrator blink RAM (ABB RAM) and the blinking of the arbitrator displayed in the segments corresponding to the address pointer value stops. If CB = "1" is set, "1" is written to the ABB RAM, and the arbitrator displayed in the segments corresponding to the address pointer value starts blinking.
   Set the address pointer value by the LPA command before executing this command.

   Transfer the LPA command, ABBC 1/5 command and CHB command as follows.

[How to transfer LPA command, ABBC 1/5 command and CHB command (character blink setting)]

LPA command

D8	D7	D6	D5	D4	D3	D2	D1
1	1	*	0	0	0	0	0

Specify the address pointer value.
(Example: Set the address pointer value to 00H.)

CHB command

D8	D7	D6	D5	D4	D3	D2	D1
0	*	*	*	0	0	CB	*

CB value is written to CHB RAM address 00H and the blinking of characters displayed in segments 1 to 5 is set. After this command is executed, the address pointer value becomes 01H.

CHB command

D8	D7	D6	D5	D4	D3	D2	D1
0	*	*	*	0	0	CB	*

CB value is written to CHB RAM address 01H, and the blinking of characters displayed in segments 6 to 10 is set. After this command is executed, the address pointer value becomes 02H.

(Repeats nine times.)

CHB command

D8	D7	D6	D5	D4	D3	D2	D1
0	*	*	*	0	0	CB	*

CB value is written to CHB RAM address 0BH and the blinking of characters displayed in segments 56 to 60 is set. After this command is executed, the address pointer value becomes 0CH.

CHB command

D8	D7	D6	D5	D4	D3	D2	D1
0	*	*	*	0	0	CB	*

CB value is written to CHB RAM address 0CH, and the blinking of characters displayed in segments 61 to 65 is set. After this command is executed, the address pointer value becomes 0DH.

CHB command

D8	D7	D6	D5	D4	D3	D2	D1
0	*	*	*	0	0	CB	*

CHB RAM address is only 00H to 0CH. **The address pointer value becomes 0DH. However, this CHB command is ignored.**

*: Don't care

[How to transfer LPA command, ABBC 1/5 command and CHB command (arbitrator blink setting)]

LPA command

D8	D7	D6	D5	D4	D3	D2	D1
1	1	*	1	0	0	0	0

Specify address pointer value
(Example: Set address pointer value to 10H.)

ABBC1/5 command

D8	D7	D6	D5	D4	D3	D2	D1
1	0	0	1	1	1	0	0

Set BC = "0" to enable writing in 5-dot units.

CHB command

D8	D7	D6	D5	D4	D3	D2	D1
0	*	*	*	0	0	CB	*

CB value is written to ABB RAM address 10H, and the blinking of arbitrator displayed in segments 1 to 5 is set. After this command is executed, the address pointer value becomes 11H.

CHB command

D8	D7	D6	D5	D4	D3	D2	D1
0	*	*	*	0	0	CB	*

CB value is written to ABB RAM address 11H, and the blinking of arbitrator displayed in segments 6 to 10 is set. After this command is executed, the address pointer value becomes 12H.

(Repeats nine times.)

CHB command

D8	D7	D6	D5	D4	D3	D2	D1
0	*	*	*	0	0	CB	*

CB value is written to ABB RAM address 1BH, and the blinking of arbitrator displayed in segments 56 to 60 is set. After this command is executed, the address pointer value becomes 1CH.

CHB command

D8	D7	D6	D5	D4	D3	D2	D1
0	*	*	*	0	0	CB	*

CB value is written to ABB RAM address 1CH and the blinking of arbitrator displayed in segments 61 to 65 is set. After this command is executed, the address pointer value becomes 1DH.

CHB command

D8	D7	D6	D5	D4	D3	D2	D1
0	*	*	*	0	0	CB	*

ABB RAM address is only 10H to 1CH. **The address pointer value becomes 1DH. However, this CHB command is ignored.**

*: Don't care

5. Arbitrator Blink command (ABB command)

This command is used to start writing arbitrator blink data to ABB RAM in 1-dot unit. This command is used with the ABB 1/5 command described above.

After setting AB = "1", setting the C/D pin from "1" to "0" enables writing arbitrator blink data to ABB RAM in 1-dot unit. After arbitrator blink data is transferred, the address pointer is automatically incremented by 1, and arbitrator blink data can be transferred continuously.

Set the address pointer value by the LPA command before executing this command. Transfer the ABBC 1/5 command, ABB command and arbitrator blink data as follows.

[How to transfer LPA command, ABBC 1/5 command, ABB command and arbitrator blink data]

	D8	D7	D6	D5	D4	D3	D2	D1	
LPA command	1	1	*	0	0	0	0	0	Specify the address pointer value. (Example: Set the address pointer to 10H.)
ABBC1/5 command	1	0	0	1	1	1	0	1	Set BC = “1” to enable writing in 1-dot unit.
ABB command	1	0	0	0	1	1	0	1	Set AB = “1” to start writing in 1-dot unit.
Arbitrator blink data	*	*	*	AB4	AB3	AB2	AB1	AB0	Arbitrator blink data is written to ABB RAM address 10H, and the arbitrator specified in segments 1 to 5 starts blinking. After this command is executed, the address pointer value becomes 11H.
Arbitrator blink data	*	*	*	AB4	AB3	AB2	AB1	AB0	Arbitrator blink data is written to ABB RAM address 11H, and the arbitrator specified in segments 6 to 10 starts blinking. After this command is executed, the address pointer value becomes 12H.
					(Repeats nine times.)				
Arbitrator blink data	*	*	*	AB4	AB3	AB2	AB1	AB0	Arbitrator blink data is written to ABB RAM address 1BH, and the arbitrator specified in segments 59 to 60 starts blinking. After this command is executed, the address pointer value becomes 1CH.

*: Don't care

Arbitrator blink data

D8	D7	D6	D5	D4	D3	D2	D1
*	*	*	AB4	AB3	AB2	AB1	AB0

Arbitrator blink data is written to ABB RAM address 1CH, and the arbitrator specified in segment 61 to 65 starts blinking. After this command is executed, the address pointer value becomes 1DH.

Arbitrator blink data

D8	D7	D6	D5	D4	D3	D2	D1
*	*	*	AB4	AB3	AB2	AB1	AB0

ABB RAM address is only 10H to 1CH. **The address pointer value becomes 1DH. However, this ABB command is ignored.**

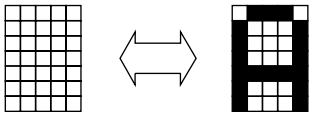
*: Don't care

6. Blink Pattern Control Command (BPC command)
   This command is used to select the blink pattern of characters.
   If BP = "1" is set, the display repeats all lighting off and character displays. If BP = "0" is set, the display repeats all light on and character displays.
   This command cannot be set for each address pointer value. If this command is executed, 13 characters are set at the same blink pattern.

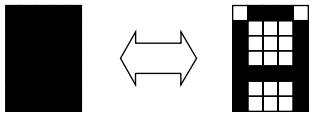
   [BPC Command Format]

D8	D7	D6	D5	D4	D3	D2	D1
1	0	0	*	0	0	1	BP

   *: Don't care



When BP = "1"



When BP = "0"

7. Address Increment Command (AINC Command)
   This command is used to increment the address pointer value by +1. After this command is executed, the processing being set by the LOT command, described below, is performed on the RAM corresponding to the address pointer value before being incremented by +1.

   [AINC Command Format]

D8	D7	D6	D5	D4	D3	D2	D1
1	0	0	*	1	*	1	*

   *: Don't care

8. Load Option Command (LOT Command)
   This command is used to process the display corresponding to the address pointer value before being incremented by 1 when the AINC command is executed.
   If I0 = "1" is set, all "0s" are written to CGA RAM and AB RAM each time the AINC command is executed. CG ROM code "00h" is displayed on the character display and the arbitrator goes out.
   If I1 = "1" is set, all "0"s are written to CHB RAM and ABB RAM each time the AINC command is executed. Therefore character and arbitrator blinking is cleared.
   I0 and I1 can be set independently. If I0 = "1" and I1 = "1" are set, "0" is written to all CG RAM, AB RAM, CHB RAM and ABB RAM.

   [LOT Command Format]

D8	D7	D6	D5	D4	D3	D2	D1
1	0	1	1	*	*	I1	I0

   *: Don't care

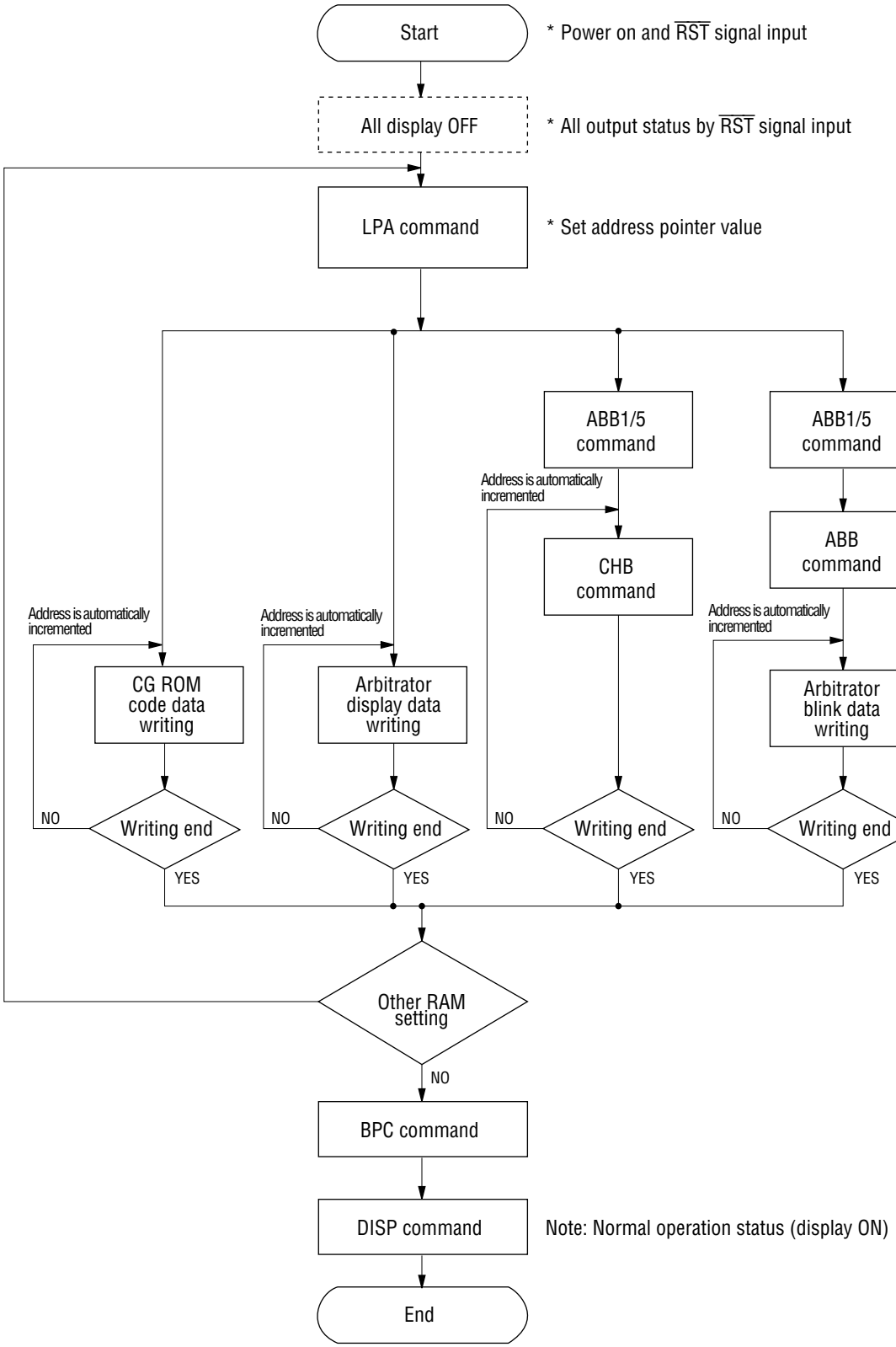
9. Serial Out Enable/Disable Command (SOE/D Command)
   This command is used to select the output impedance of the SO pin.
   When S = "1" is selected, the S0 pin becomes CMOS output and it outputs displays data. While S = "0" is selected, the S0 pin becomes high impedance status.

   [SOE/D Command Format]

D8	D7	D6	D5	D4	D3	D2	D1
1	0	0	*	0	1	1	S

   *: Don't care

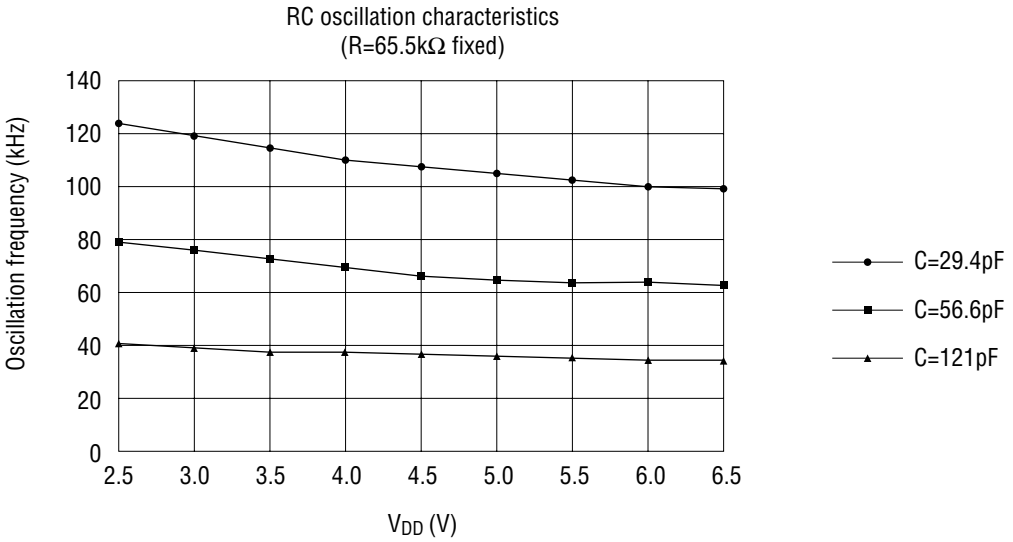
Initial Setting Operation Flow Chart

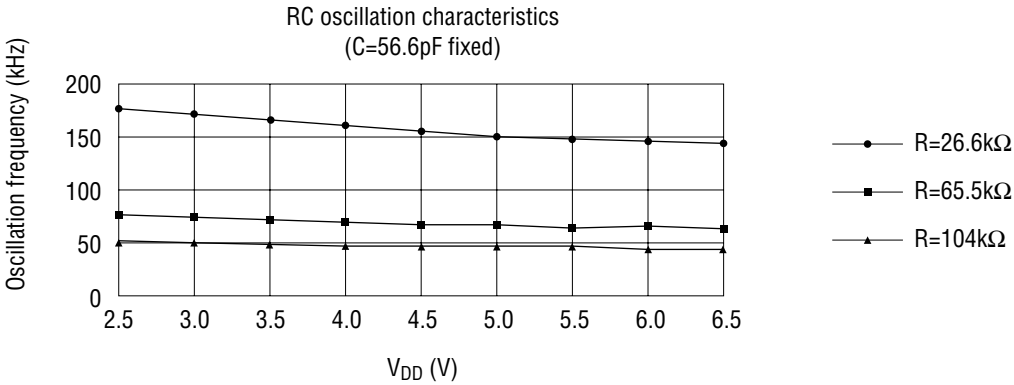


MSM9005-01 CG ROM Code

REFERENCE DATA

Oscillation Circuit Characteristics

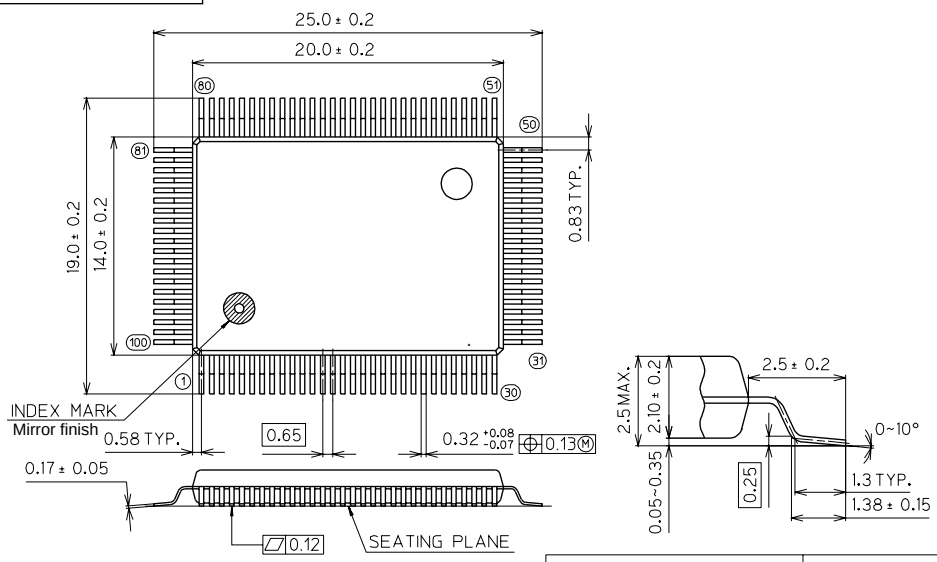




PACKAGE DIMENSIONS

(Unit : mm)

QFP100-P-1420-0.65-BK



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5 μm)
Package weight (g)	1.29 TYP.
Rev. No./Last Revised	4/Nov. 28, 1996

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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