Preliminary

OKI Semiconductor

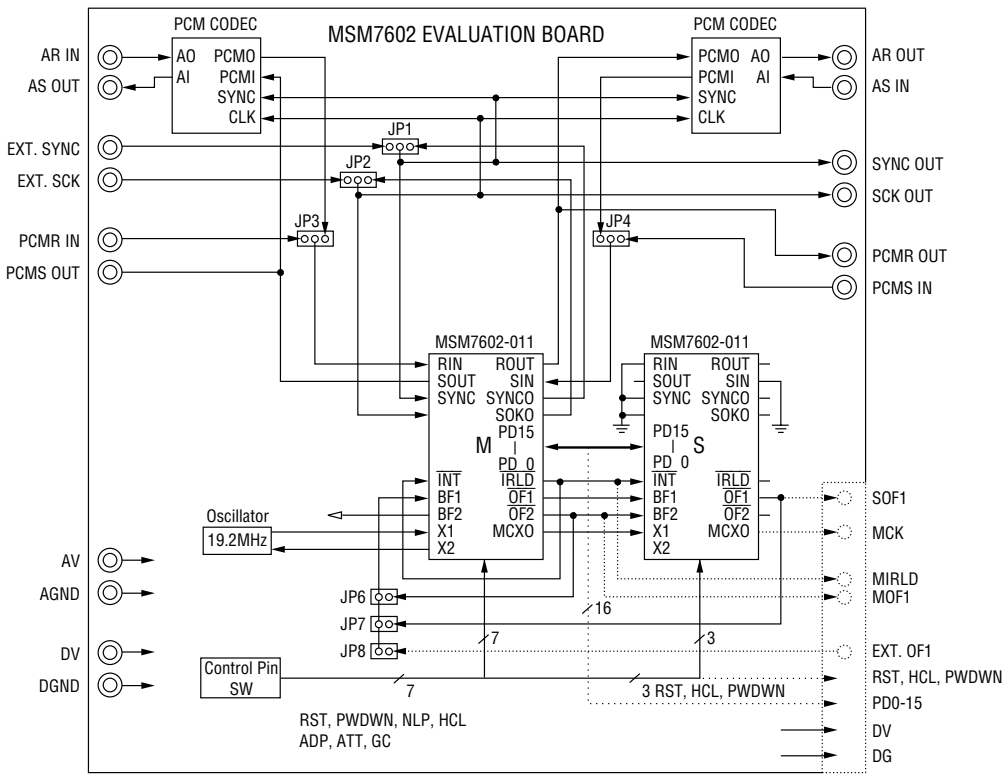
MSM7602

Evaluation Board

GENERAL DESCRIPTION

This evaluation board has been developed to evaluate the characteristics of the echo canceller MSM7602.
The MSM7602–011 (56–pin QFP) is used as this evaluation board, using a single chip or two chips (master and slave) cascade–connection.
The MSM7602–001 (28–pin SSOP) can also be used for the evaluation. However, since this MSM7602 uses a 56–pin QFP socket, special care should be taken on connecting the LSI device to the MSM7602–001.
Although the MSM7602 is available as a 28–pin SSOP and a 32–pin TSOP, in addition to the 56–pin QFP used for this evalution board, almost no difference is recognized among their characteristics as long as they are used as a single chip respectively.
If the characteristics of a 56–pin single chip are evaluated, the evaluation result can be applied to the basic characteristics of echo cancellers of both SSOP and TSOP.
The MSM7602 can support the both 3V and 5V supply voltages. This evaluation board can also support the both voltages if the PCM CODEC is replaced.
This evaluation board is provided with both analog and digital input/output interfaces, so that it can support a wide range of evaluation circuits.

BLOCK DIAGRAM

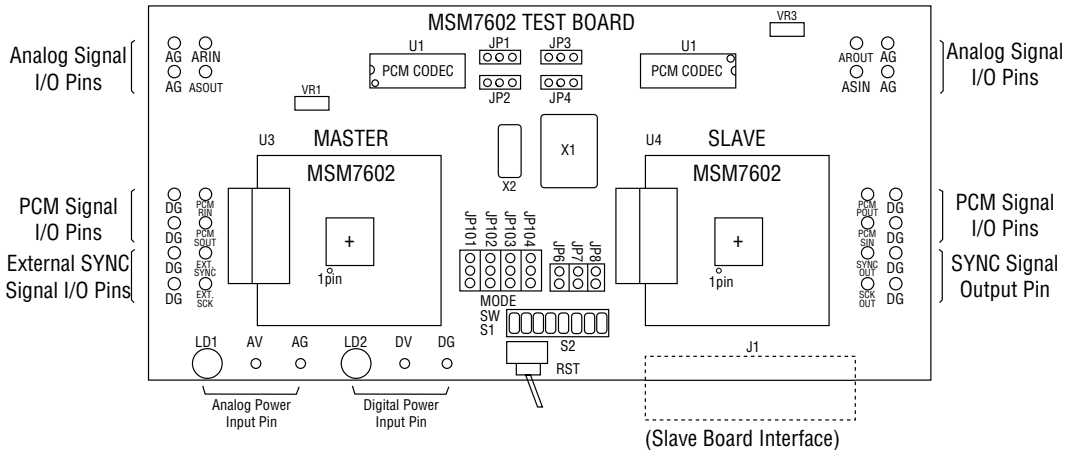


*The area enclosed with a dotted line is an optional interface for a slave board.

SPECIFICATIONS

		3V Operation	5V Operation
CODEC		**MSM7566**	**MSM7543**
Analog input block Max. input level Input impedance		1.4VP–P 600Ω	2.4VP–P 600Ω
Analog output block Output level Output impedance		2.6VP–P 600Ω	2.6VP–P 600Ω
Digital input	V_{IH} V_{IL}	1.8V to V_{DD} 0 to 0.5V	2.2V to V_{DD} 0 to 0.8V
Digital output	V_{OH} V_{OL}	2.2V to V_{DD} 0 to 0.4V	4.2V to V_{DD} 0 to 0.6V
Supply voltage		2.7V to 3.6V	4.5V to 5.5V
Operating temperature		–30 to 85°C	
Board size		18 × 11cm	
Echo canceller specification		MSM7602-011(56–pin QFP) used. Evaluation is possible with a single chip or in a 2–chip cascade connection. Use of optional slave boards enables multi–chip cascade connection in the MSM7602–011 board.	
Echo canceller characteristics Echo attenuation Cancelable delay time		30dB Input signal: White noise–10 dBm0 ERL: 6 dB(echo volume=–10 dB0–6 dB=–16 dBm0) Echo delay time: 2 ms Control mode: NLP, ATT, GC, and OFF When a single chip is used 27ms(max.) When in a 2–chip cascade connection 31ms(max.) When in a 7–chip cascade connection 213ms(max.) (Master Chip × 1 + Slave Chip × 6) Note: Slave boards(optional) are needed for multi–chip cascade connection.	
Basic clock		19.2MHz	

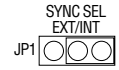
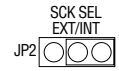
EXTERNAL VIEW/PARTS ARRANGEMENT

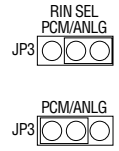
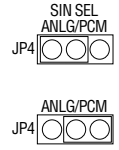
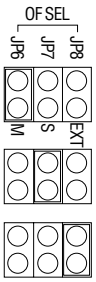
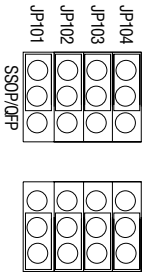


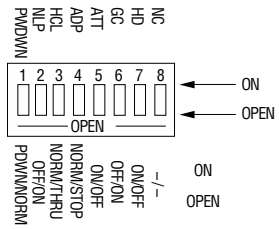
DESCRIPTION OF PINS/PARTS

Pin Name	I/O	Description
A RIN	I	Input pin for RIN signal when analog interface is used. Input analog signal is converted to μ–law PCM (A/D conversion) by U1 PCM CODEC and used as RIN signal of MSM7602. Set JP3 (RIN SEL) to ANLG when using ARIN input. (See JP3)
A ROUT	O	Output pin for ROUT signal when analog interface is used. This pin outputs analog signals D/A–converted from ROUT signal (PCM) of MSM7602 by U2 PCM CODEC. The signal level can be amplified by about 0 to +12 dB using variable resistor VR3.
A SIN	I	Input pin for SIN signal when analog interface is used, Input analog signal is converted to μ–law PCM (A/D conversion) by U2 PCM CODEC and used as SIN signal of MSM7602. Set JP4(SIN SEL) to ANLG when using ASIN input. (See JP4.)
A SOUT	O	Output pin for SOUT signl when analog interface is used. This pin outputs analog signals D/A–converted from SOUT signal (PCM) of MSM7602 by U1 PCM CODEC. This signal level can be amplified by about 0 to +12 dB using variable resistor VR1.
PCM RIN	I	Input pin for RIN signal when PCM interface is used. This input signal is used directly as RIN signal of MSM7602. Input positive phase signal to this pin. Set JP3 (RIN SEL) to PCM when using PCM RIN. (See JP3.) Use of PCM interface requires synchronization with destination. Use external synchronization (EXT.SYNC or EXT.SCK) or synchronizing signal output (SYNC OUT or SCK OUT) for the synchronization with destination.
PCM ROUT	O	Output pin for ROUT signal when PCM interface is used. This pin outputs ROUT signal (positive phase) of MSM7602 directly. Use of PCM interface requires synchronization with destination. Use external synchronization (EXT.SYNC or EXT.SCK) or synchronizing signal output (SYNC OUT or SCK OUT) for the synchronization with destination.

Pin Name	I/O	Description
PCM SIN	I	Input pin for SIN signal when PCM interface is used. This input signal is used as SIN signal of MSM7602 as is. Input positive phase signal to this pin. Set JP4 (SIN SEL) to PCM when using PCM SIN.(See JP4.) Use of PCM interface requires synchronization with destination. Use enternal synchronization (EXT.SYNC or EXT.SCK) or synchronizing signal output (SYNC OUT or SCK OUT) for the synchronization with destination.
PCM SOUT	O	Output pin for SOUT signal when PCM interface is used. This pin outputs SOUT signal of MSM7602 directly at positive phase signal. Use of PCM interface requires synchronization with destination. Use external synchronization (EXT.SYNC or EXT.SCK) or synchronizing signal output (SYNC OUT or SCK OUT) for the synchronization with destination.
EXT.SYNC	I	Input pin for EXT.SYNC signal when external synchronization is required. EXT.SYNC signal is used as synchronizing signal when PCM interface is used.(See JP1.) Input 8kHz SYNC (positive phase) to this pin.
EXT.SCK	I	Input pin for EXT.SCK signal when external when external synchronization is required. EXT.SCK signal is used as synchronizing signal when PCM interface is used. (See JP2.) Input 64 to 2048 kHz SCK (positive phase) signal to this pin.
SYNC OUT	O	Output pin for synchronizing SYNC signal. SYNC OUT signal is used as synchronizing signal when PCM interface is used. This pin outputs SYNC signal (positive phase) used for actual operations. (This pin outputs SYNC0 in internal SCK mode and EXT.SYNC when external synchronizing signal is used.) (See JP1.)
SCK OUT	O	Output pin for synchronizing SCK signal. SCK OUT signal is used as synchronizing signal when PCM interface is used. This pin outputs SCK signal (positive phase) used for actual operations. (This pin outputs SCK0 in internal SCK mode and EXT.SCK when external synchronizing signal is used.) (See JP2.)
AV	I	Power supply for analog system. Input 3V or 5V just like power supply for digital system. Select PCM CODEC (U1/U2) according to selected supply voltage. 3V operation: MSM7566 5V operation: MSM7543
AG	—	GND for analog system. Basically this GND is separated from GND for digital system.
DV	I	Power supply for digital system. Input 3V or 5V just like power supply for analog system. Select PCM CODEC (U1/U2) according to selected supply voltage. 3V operation: MSM7566 5V operation: MSM7543
DG	—	GND for digital system. Basicarry, this GND is separated from GND for analog system.

Part No./Name		Description
U1 U2	PCM CODEC	Uses μ–law CODEC is used. Select PCM CODEC (CU1/U2) according to selected supply voltage. 3V operation: MSM7566 5V operation: MSM7543 Note that U2 parts are reversely placed.
U3	MSM7602-011 IC socket MASTER	Mount MSM7602-011 (28–pin SSOP) or MSM7602-011 (56–pin QFP). When using 28–pin SSOP, be careful to set LSI device so that the pins may not be shifted. 56-pin QFP can be used as a master chip for single chip or multi-chip cascade connection. OF SEL jumpers (JP6–JP8) are used to select single chip mode or cascade mode. (See JP6 to JP8)
U5	MSM7602-011 IC socket SLAVE	Mount MSM7602-011 (56–pin QFP). This chip can be used as a slave chip in cascade connection. OF SEL jumpers (JP6–JP8) are used to select cascade mode. (See JP6 to JP8.)
X1	Crystal oscillator	19.2 MHz is used and the oscillation circuit has to be assembled. When using this oscillator (X1), remove X2 oscillator.
X2	Crystal oscillator	19.2 MHz is used, the oscillation circuit has to be assembled. C20, C21:27pF R12: 1 MΩ When using X2, either 3V to 5V can be used. When using X2, remove X1.
VR1	ASOUT volume	Variable resistor to adjust output level of ASOUT by about 0 to +12 dB.
VR3	AROUT volume	Variable resistor to adjust output level of AROUT by about 0 to +12 dB.
JP1	SYNC SEL jumper	SYNC select pin. This pin selects internal SYNC signal or external SYNC signal. Set this JP1 just like JP2 (SCK selector).  Internal SYNC mode: Uses SYNC0 signal output from U1 (MSM7602).  External SYNC mode: SYNC signal that is input from EXT.SYNC pin is used.
JP2	SCK SEL jumper	SCK select pin. This pin selects internal SCK signal or external SCK signal. Set this JP2 just like JP1 (SYNC selector).  Internal SCK mode: Uses SCK0 signal output from U1 (MSM7602).  External SCK mode: SCK signal that is input from EXT.SYNC pin is used.

Part No./Name		Description
JP3	RIN SEL jumper	RIN select pin. This pin selects signal to be input to RIN of MSM7602.  Analog input mode: PCM signal is used, which is converted (A/D conversion) by U1 (PCM CODEC) from analog signal that is input from ARIN pin. PCM input mode: PCM signal is used, which is input from RIN pin.
JP4	SIN SEL jumper	SIN select pin. This pin selects signals to be input to SIN of MSM7602.  PCM input mode: PCM signal is used, which is converted (A/D conversion) by U1(PCM CODEC) from analog signal that is input from ASIN pin. PCM input mode: PCM signal is used, which is input from RIN pin.
JP6 JP7 JP8	OF SEL jumper	OUT FLAG select pins (cascade select pins). These pins select OF (OUT FLAG) to be input to SF1 of MSM7602 MASTER(U1). When OF is selected, cascade mode is set.  Single chip mode: Inputs MASTER OF2 to SF1 of MASTER to execute single chip operation. No problem will arise even if a chip is mounted in slave socket. 2–chip cascade mode: Inputs SLAVE OF1 to SF1 of MASTER to connect 2 chips in cascade form. Multi–chip cascade mode: Multi–step cascade connection is made by using optional slave boards. Normally, this mode not used.
JP101 JP102 JP103 JP104	SSOP/QFP SEL jumper	SSOP/QFP SEL select pins. These pins select echo canceller package.  SSOP mode: Use MSM7602-001 (28–pin SSOP) in this mode. QFP mode: Use MSM7602-001 (56–pin QFP) in this mode.

Part No./Name		Description			
S1	MODE SW	Sets up control pins of MSM7602. 			
		MODE SW			Operation
		1	PDWN	ON	Sets power down mode. This switch stops MSM7602 operation to reduce power consumption.
				OPEN	Sets normal mode.
		2	NLP	ON	Turns center clip off.
				OPEN	Turns center clip on. When SOUT output is –57 dBm0 or lower, this switch outputs min. positive value(FFh) forcibly to reduce idle circuit noise.
		3	HCL	ON	Sets normal mode to cancel echo.
				OPEN	Sets through mode. Data that was input to RIN and SIN are output to ROUT and SOUT in through mode respectively.
		4	ADP	ON	Sets normal mode to update AFF coefficient.
				OPEN	Sets coefficient fix mode to stop updating of AFF coefficient and operates LSI device according to stop time coefficient.
		5	ATT	ON	Turns ATT on. Attenuator(6 dB)prepared in RIN and SOUT is inserted in MSM7602 according to input status. Refer to data sheet for operation.
				OPEN	Turns ATT off.
		6	GC	ON	Turns GC off.
				OPEN	Controls signal level to be within 0 to 8.5 dB using gain controller prepared in RIN. Level control is validated at around –24 dBm0.
		7	HD	ON	Turns HD on. This switch detects and cancels howling.
				OPEN	Turns HD off.
		8	NC	—	Not connected(reserved). This switch may be set to ON or OPEN.

Part No./Name		Description
S2	RST SW	Resets MSM7602. Be sure to reset MSM7602 after power is turned on.
J1	Connector to connect slave board	Used for multi-chip cascade connection test using optional slave boards. Normally, this is not used.
LD1	Analog power light	Goes on after analog power input.
LD2	Digital power light	Goes on after digital power input.

USING METHOD

This evaluation board is used for MSM7602 only. When evaluating the characteristics of the LSI device, check the operation of this board using the MSM7602 data sheet.

1) Set jumper pins suitable for the circuit to be connected.
   (1) Set the usable package (SSOP or QFP).
   JP101 to 104 SSOP/QFP

   (2) Set the synchronizing signal (external or internal synchronization).
   JP1 (SYNC SEL) EXT/INT
   JP2 (SCK SEL) EXT/INT

   (3) Set the input signals(PCM or analog).
   JP3 (RIN SEL) PCM/ANLG
   JP4 (SIN SEL) ANLG/PCM

   (4) Set the number of echo cancellers to be connected (single or cascade).
   JP6 single chip
   JP7 2–chip cascade
   JP8 Multi–chip cascade (Slave boards are needed.)

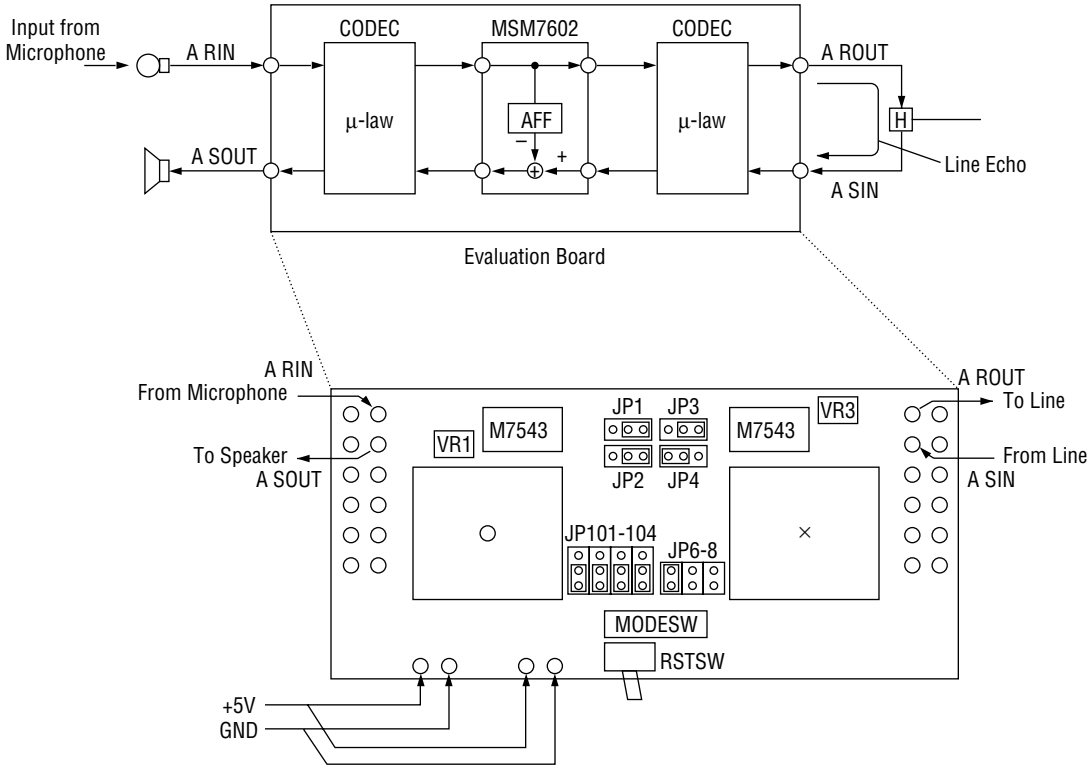
2) Adjust the analog output level.
   In this evaluation board, the analog output level can be adjusted by about 0 to +12dB using VR3 and VR1.
   3V CODEC (MSM7566) should be adjusted because input and output levels are different.
   Set input and output levels using a level meter or an oscilloscope, so that they are equal or have levels specified.

3) Connect the power supply and the ground (GND).
   In this board, basically analog and digital systems are separated from each other.
   Since the characteristics of an analog circuit affect the characteristics of an echo canceller, use an analog power supply/GND with less noise.
   A power supply/GND with less noise can be used commonly for both analog and digital systems.

4) Set the MODE switch to desired mode.
   Note: Do not turn the power on while the MODE SW1 (PWDWN SW) is on (in the power down mode).
   Power down should be made after more than 10 basic clocks are input. This is to stabilize the internal status.

5) The setting of the MSM7602 evaluation board is complete.
   Input signals from the set interface to start the test.
   Note: Be sure to reset the MSM7602 after the power is turned on.

● Use example 1: Line echo cancellation (to cancel the line echo caused by an input from a microphone)
Setups: 56–pin QFP single chip, analog interface, and internal synchronization

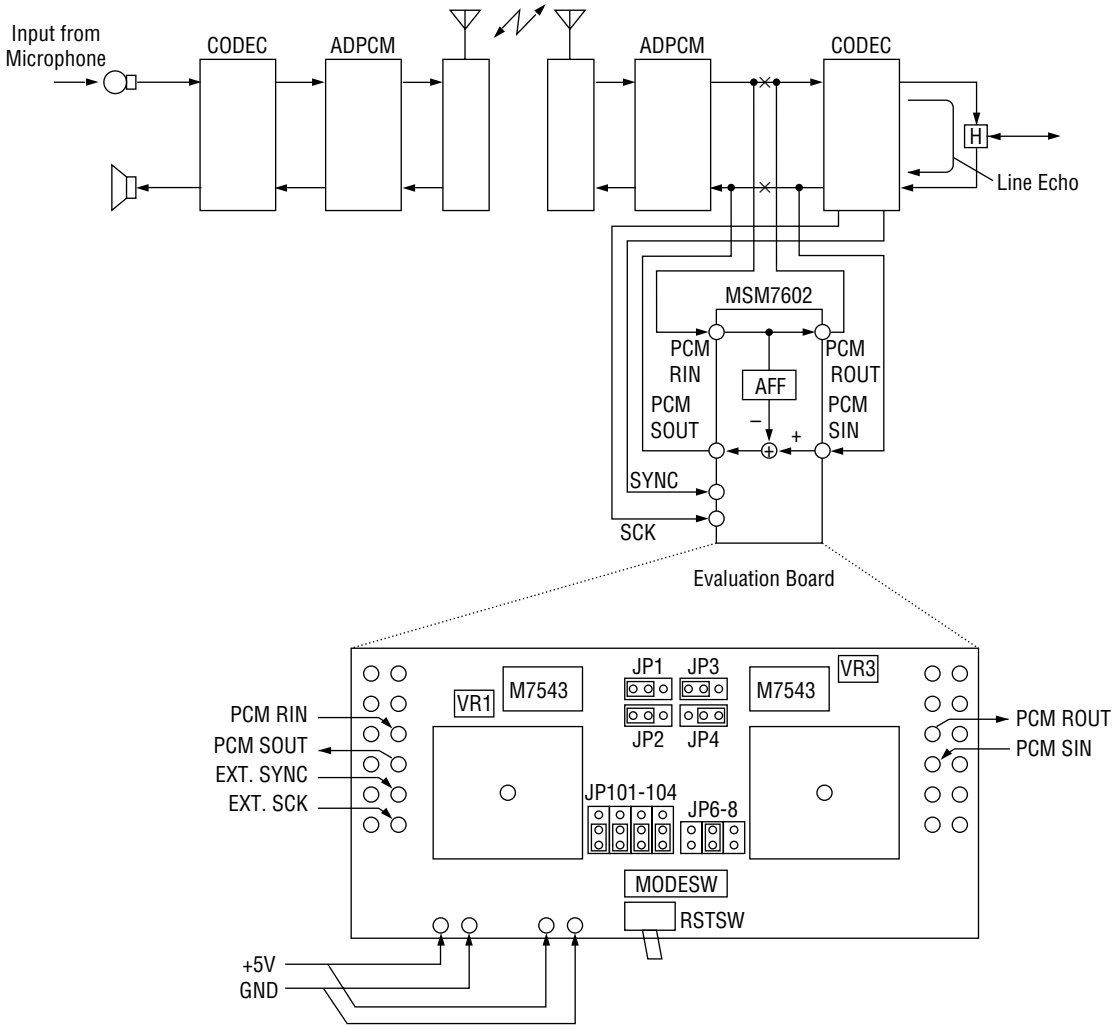


(1) Set the evaluation board as follows.
- Set JP101 to 104 to QFP to set the 56–pin QFP mode.
- Set JP1 and JP2 to INT to set the internal synchronization mode.
- Set JP3 and JP4 to ANLG to set the analog interface mode.
- Set the OF SEL jumpers(JP6 to JP8) to M(JP6) to set the single chip mode.
- Make sure the MODE switch 1(PWDWN SW) is set to OPEN.

(2) Connect the MSM7602 to a power supply and adjust the analog output level.
Reset the MSM7602 after the power is turned on.
Tone signal may be used to adjust the analog output level. In the test, however, be sure to use white noise or voice.

(3) Connect the inputs/outputs of the MSM7602 to the test system and start the test.
Reset the MSM7602 after the power is turned on.

● Use example 2: Connecting an echo cancellor to an existing PCM circuit and checking the effect of the echo canceller.
Setups: 56-pin QFP 2-chip cascade, PCM interface, and external synchronization



(1) Set the evaluation board as follows.
- Set JP101 to 104 to QFP to set the 56–pin QFP mode.
- Set JP1 and JP2 to EXT to set the external synchronization mode.
- Set JP3 and JP4 to PCM to set the PCM interface mode.
- Set the OF SEL jumpers (JP6 to JP8) to S (JP7) to set the 2–chip cascade mode.
- Make sure the MODE switch 1 (PWDWN SW) is set to OPEN.

(2) Connect the MSM7602 to a power supply and adjust the analog output level.
Reset the MSM7602 after the power is turned on.
Tone signal may be used to adjust the analog output level. In the test, however, be sure to use white noise or voice.

(3) Connect the inputs/outputs of the MSM7602 to the test system and start the test.
Reset the MSM7602 after the power is turned on.

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2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit and assembly designs.

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