

# MSM66577 Family

## 16-Bit Microcontroller

### GENERAL DESCRIPTION

The MSM66577 family of highly functional CMOS 16-bit single chip microcontrollers utilizes the nX-8/500S, Oki's proprietary CPU core.

Four channels of serial ports, consisting of two channels of synchronous serial ports with 32-byte FIFO registers and two channels of UART/synchronous serial ports, enable easy interfacing with external peripheral LSI devices such as an encoder/decoder or servocontroller.

A switching function permits selection of separate address and data lines or multiplexed lines for the external bus interface to correspond to various peripheral LSI devices.

With features such as a clock gear function, dual clock function, STOP/HALT mode, programmable pull-up ports in which individual bits can be programmed, and a small, thin package, the MSM66577 family of microprocessors is optimally suited for the system control of small-sized low power devices.

The flash ROM version (MSM66Q577LY) programmable with a single 3V power supply (3.0 to 3.6V) and flash ROM version (MSM66Q577) programmable with a single 5V power supply (4.5 to 5.5V) are also included in the family.

### APPLICATIONS

Digital Audio Control Systems  
PC Peripheral Control Systems  
Office Electronics Control Systems

### ORDERING INFORMATION

Order Code or Product Name	Package	Remark
MSM66577L-xxTB *1	100-pin plastic TQFP (TQFP 100-P-1414-0.50-K)	Low voltage mask ROM version (2.4 to 3.6 V)
MSM66577-xxTB *1		5 V mask ROM version (4.5 to 5.5 V)
MSM66Q577LY-NTB *2		MSM66577L flash ROM version (3.0 to 3.6V)
MSM66Q577-NTB *2		MSM66577 flash ROM version (4.5 to 5.5 V)

\*1 : The "xx" of "-xx" stands for the code number.

\*2 : The "N" of "-N" stands for the flash ROM blank version.

When OKI programs and ship the flash ROM, the part number is changed from "-N" to "-XX" (code number) , for example, MSM66Q577-999TB.

## FEATURES

Name	MSM66577L	MSM66577
Operating temperature	-30°C to +70°C	
Power supply voltage/ maximum frequency	$V_{DD} = 2.4$ to $3.6$ V/ $f = 14$ MHz	$V_{DD} = 4.5$ to $5.5$ V/ $f = 30$ MHz
Minimum instruction execution time	143 ns at 14 MHz	67 ns at 30 MHz
	61 $\mu$ s at 32.768 kHz	
Internal ROM size (max. external)	128 KB (1 MB)	
Internal RAM size (max. external)	4 KB (1 MB)	
I/O ports	74 I/O pins (with programmable pull-up resistors) 8 input-only pins	
Timers	16-bit free running timer $\times$ 1ch	
	Compare output/capture input $\times$ 2ch	
	16-bit auto reload timer (event input/timer out) $\times$ 1ch	
	8-bit auto reload timer $\times$ 2ch (can also be used as 16-bit timer $\times$ 1ch)	
	8-bit auto reload timer $\times$ 1ch	
	8-bit auto reload timer $\times$ 3ch (also functions as serial communication baud rate generator)	
	8-bit auto reload timer $\times$ 1ch (also functions as watchdog timer)	
	Watch timer (Real-time counter) $\times$ 1ch	
	8-bit PWM $\times$ 4ch (can also be used as 16-bit PWM $\times$ 2ch)	
Serial port	Synchronous, with 32-byte FIFO $\times$ 2ch	
	UART/Synchronous $\times$ 2ch	
A/D converter	10-bit A/D converter $\times$ 8ch	
D/A converter	8-bit D/A converter $\times$ 2ch	
External interrupt	Non-maskable $\times$ 1ch	
	Maskable $\times$ 8ch	
Interrupt priority	3 levels	
Others	External bus interface (Separate address and data busses / multiplexed address and data busses)	
	Bus release function	
	Dual clocks function	
	Clock gear function	
Flash ROM version	MSM66Q577LY ( $V_{DD}=3.0$ to $3.6$ V)	MSM66Q577

## SPECIAL FEATURES

### 1. High-performance CPU

The family includes the high-performance CPU, powerful bit manipulation instruction set, full symmetrical addressing mode, and ROM WINDOW function, and also provides the best optimized C compiler support.

### 2. A variety of power saving modes

Attaching a 32.768-kHz crystal produces a real-time clock signal from the internal clock timer. Use of a single clock in place of dual clocks is possible.

The clock gear function allows a  $1/2 \times$  or  $1/4 \times$  main clock to be selected for the CPU operating clock.

Switching the CPU clock to 32.768-kHz signal,  $1/2 \times$  main clock, or  $1/4 \times$  main clock, then produces operation in a low power consumption mode.

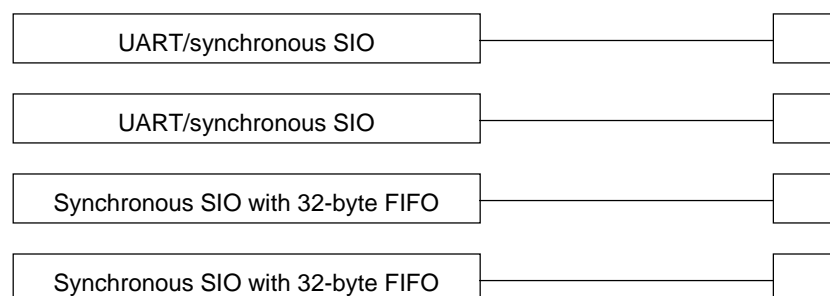
The family provides a wide range of standby control functions. In addition to the usual STOP mode that stops the oscillator, there are the quick restart STOP mode that shuts down the CPU and peripherals but leaves the oscillator running, and the HALT mode that shuts down the CPU but leaves the peripherals running.

### 3. Variety of multifunctional serial ports

The family includes two channels of built-in synchronous serial ports with 32-byte FIFO implementing an auto transfer function.

The family allows multi-byte 1-frame information which consists of address, command, and data to be easily and efficiently transmitted to or received from a serial interface type peripheral LSI device. The family also allows multi-byte character information to be easily and efficiently transmitted to or received from an LCD module.

In addition, the family has two channels of combined UART/synchronous serial ports, and provides four channels of serial interfaces.



### 4. MSM66Q577LY and MSM66Q577 with flash memory programmable with single power supply

In addition to the regular mask ROM version, the family includes these versions with 128KB of flash memory that can be programmed using a single power supply.

For the MSM66Q577LY, an internal booster circuit derives the necessary program voltage from the device's low (3.0 to 3.6V) power supply, and the program voltage for the MSM66Q577 is provided with a single 5 V power supply (4.5 to 5.5 V).

### 5. High-precision A/D and D/A converters

The family includes a high-precision 10-bit analog-to-digital converter with eight channels and 8-bit digital-to-analog converter with two channels.

## **6. Multifunction PWM**

The family supports both 8- and 16-bit PWM operation.

Choosing between the time-base counter output or overflow from an 8-bit auto-reload timer as the PWM counter clock source provides a wide number of possibilities over a broad frequency range. The 16-bit PWM configuration supports a high-speed synchronization mode that generates a high-precision output signal with less ripple suitable for digital-to-analog control applications.

## **7. Programmable pull-up resistors**

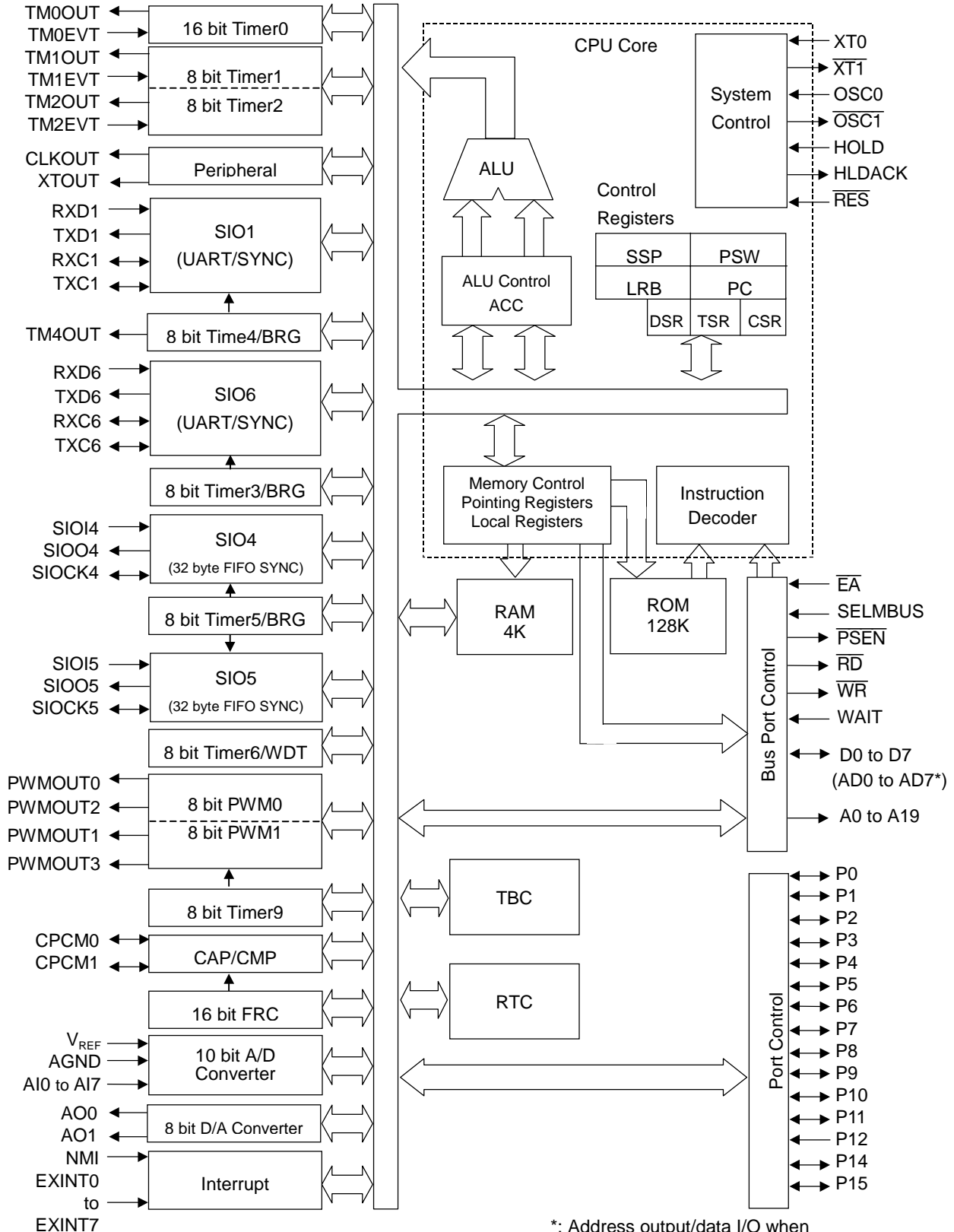
Building the pull-up resistors into the chip contributes to overall design compactness.

Making them programmable on a per-bit basis allows complete flexibility in circuit board layout and system design. These programmable pull-up resistors are available for all I/O pins not already assigned specific functions (such as the oscillator connection pins).

## **8. Wide support for external interrupts**

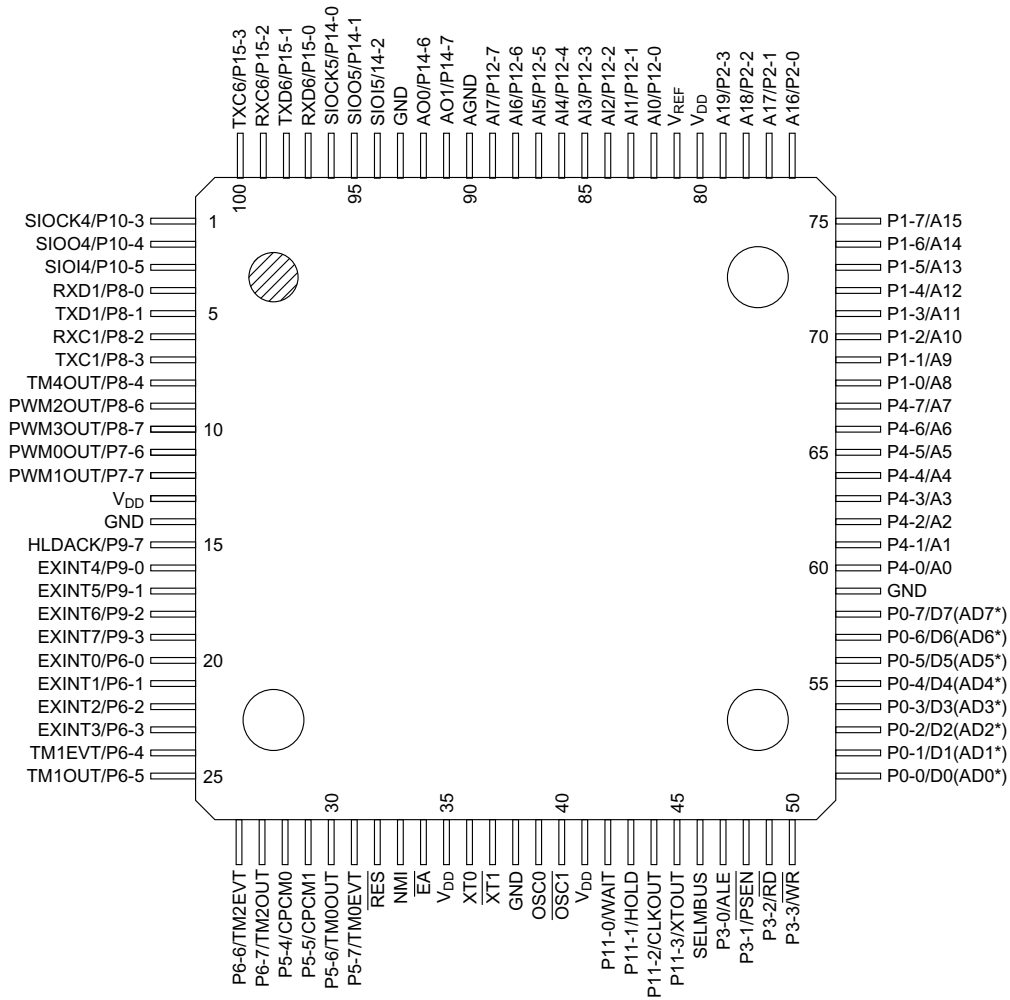
There are a total of nine interrupt channels for use in communicating with external devices: eight for maskable interrupts and one for non-maskable interrupts.

**BLOCK DIAGRAM**



\*: Address output/data I/O when selecting multiplexed bus type.

**PIN CONFIGURATION (TOP VIEW)**



**100-pin Plastic TQFP**

\*: Address output/data I/O when selecting multiplexed bus type.

## PIN DESCRIPTIONS

In the Type column, “I” indicates an input pin, “O” indicates an output pin, and “I/O” indicates an I/O pin.

Function	Symbol	Description			
		Type	Primary function	Type	Secondary function
Port	P0_0/D0 (AD0) to P0_7/D7 (AD7)	I/O	8-bit I/O port 10 mA sink capability Pull-up resistors can be specified for each individual bit	I/O	External memory access Data I/O port (Address output/data I/O port when selecting a multiplexed bus)
	P1_0/A8 to P1_7/A15	I/O	8-bit I/O port Pull-up resistors can be specified for each individual bit	O	External memory access Address output port
	P2_0/A16 to P2_3/A19	I/O	4-bit I/O port Pull-up resistors can be specified for each individual bit	O	External memory access Address output port
	P3_0/ALE	I/O	4-bit I/O port 10 mA sink capability Pull-up resistors can be specified for each individual bit	O	External memory access Address latch enable signal output pin
	P3_1/ $\overline{\text{PSEN}}$			O	External program memory access Read strobe output pin
	P3_2/ $\overline{\text{RD}}$			O	External data memory access Read strobe output pin
	P3_3/ $\overline{\text{WR}}$			O	External data memory access Write strobe output pin
	P4_0/A0 to P4_7/A7	I/O	8-bit I/O port Pull-up resistors can be specified for each individual bit	O	External memory access Address output port (When selecting a separate bus type)
	P5_4/CPCM0	I/O	4-bit I/O port Pull-up resistors can be specified for each individual bit	I/O	Capture 0 input / Compare 0 output pin
	P5_5/CPCM1			I/O	Capture 1 input / Compare 1 output pin
	P5_6/TM0OUT			O	Timer 0 timer output pin
	P5_7/TM0EVT			I	Timer 0 external event input pin
	P6_0/EXINT0	I/O	8-bit I/O port Pull-up resistors can be specified for each individual bit	I	External interrupt 0 input pin
	P6_1/EXINT1			I	External interrupt 1 input pin
	P6_2/EXINT2			I	External interrupt 2 input pin
	P6_3/EXINT3			I	External interrupt 3 input pin
	P6_4/TM1EVT			I	Timer1 external event input pin
	P6_5/TM1OUT			O	Timer 1 timer output pin
	P6_6/TM2EVT			I	Timer 2 external event input pin
	P6_7/TM2OUT			O	Timer 2 timer output pin

Function	Symbol	Description			
		Type	Primary function	Type	Secondary function
Port	P7_6/PWM0OUT	I/O	2-bit I/O port	O	PWM0 output pin
	P7_7/PWM1OUT		Pull-up resistors can be specified for each individual bit	O	PWM1 output pin
	P8_0/RXD1	I/O	7-bit I/O port	I	SIO1 receive data input pin
	P8_1/TXD1		Pull-up resistors can be specified for each individual bit	O	SIO1 transmit data output pin
	P8_2/RXC1		I/O	SIO1 receive clock I/O pin	
	P8_3/TXC1		I/O	SIO1 transmit clock I/O pin	
	P8_4/TM4OUT		O	Timer 4 timer output pin	
	P8_6/PWM2OUT		O	PWM2 output pin	
	P8_7/PWM3OUT		O	PWM3 output pin	
	P9_0/EXINT4		I/O	5-bit I/O port	I
	P9_1/EXINT5	Pull-up resistors can be specified for each individual bit		I	External Interrupt 5 input pin
	P9_2/EXINT6	I		External Interrupt 6 input pin	
	P9_3/EXINT7	I		External Interrupt 7 input pin	
	P9_7/HLDACK	O		HOLD mode output pin	
	P10_3/SIOCK4	I/O	3-bit I/O port	I/O	SIO4 transmit-receive clock I/O pin
	P10_4/SIOO4		Pull-up resistors can be specified for each individual bit	I	SIO4 receive data input pin
	P10_5/SIOI4		O	SIO4 transmit data output pin	
	P11_0/WAIT	I/O	4-bit I/O port 10 mA sink capability	I	External data memory access wait input pin
	P11_1/HOLD		Pull-up resistors can be specified for each individual bit	I	HOLD mode request input pin
	P11_2/CLKOUT		O	Main clock pulse output pin	
	P11_3/XTOUT		O	Sub clock pulse output pin	
	P12_0/AI0 to P12_7/AI7	I	8-bit input port	I	A/D converter analog input port
	P14_0/SIOCK5	I/O	5-bit I/O port	I/O	SIO5 transmit-receive clock I/O pin
	P14_1/SIOO5		Pull-up resistors can be specified for each individual bit	O	SIO5 transmit data output pin
	P14_2/SIOI5		I	SIO5 receive data input pin	
	P14_6/AO0		O	D/A converter analog output port	
	P14_7/AO1		O	D/A converter analog output port	
	P15_0/RXD6	I/O	4-bit I/O port	I	SIO6 receive data input pin
	P15_1/TXD6		Pull-up resistors can be specified for each individual bit	O	SIO6 transmit data output pin
	P15_2/RXC6		I/O	SIO6 receive clock I/O pin	
P15_3/TXC6	I/O		SIO6 transmit clock I/O pin		



Function	Symbol	Type	Description
Power supply	$V_{DD}$	I	Power supply pin Connect all $V_{DD}$ pins to the power supply.*
	GND	I	GND pin Connect all GND pins to GND.*
	$V_{REF}$	I	Analog reference voltage pin (Connect to the $V_{DD}$ pin when A/D converter is not used.)
	AGND	I	Analog GND pin (Connect to the GND pin when A/D converter is not used.)
Oscillation	XT0	I	Sub clock oscillation input pin Connect to a crystal oscillator of $f = 32.768$ kHz.
	$\overline{XT1}$	O	Sub clock oscillation output pin Connect to a crystal oscillator of $f = 32.768$ kHz. The clock output is opposite in phase to XT0.
	OSC0	I	Main clock oscillation input pin Connect to a crystal or ceramic oscillator. Or, input an external clock.
	$\overline{OSC1}$	O	Main clock oscillation output pin Connect to a crystal or ceramic oscillator. The clock output is opposite in phase to OSC0. Leave this pin unconnected when an external clock is used.
Reset	$\overline{RES}$	I	Reset input pin
Other	NMI	I	Non-maskable interrupt input pin
	$\overline{EA}$	I	External program memory access input pin If the $\overline{EA}$ pin is enabled (low level), the internal program memory is masked and the CPU executes the program code in external program memory through all address space.
	SELMBUS	I	External bus interface selection input pin SELMBUS = H: Address/data separate bus type SELMBUS = L: Multiplexed bus type

\* Each of the family devices has unique pattern routes for the internal power and ground. Connect the power supply voltage to all  $V_{DD}$  pins and the ground potential to all GND pins. If a device may have one or more  $V_{DD}$  or GND pins to which the power supply voltage or the ground potential is not connected, it can not be guaranteed for normal operation.

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Condition		Rated value	Unit
Digital power supply voltage	$V_{DD}$	GND = AGND = 0 V Ta = 25°C	MSM66577/Q577	-0.3 to +7.0	V
			MSM66577L/Q577LY	-0.3 to +4.6	V
Input voltage	$V_I$		—	-0.3 to $V_{DD} + 0.3$	V
Output voltage	$V_O$		—	-0.3 to $V_{DD} + 0.3$	V
Analog reference voltage	$V_{REF}$	—	-0.3 to $V_{DD} + 0.3$	V	
Analog input voltage	$V_{AI}$	—	-0.3 to $V_{REF}$	V	
Power dissipation	$P_D$	Ta = 70°C per package	100-pin TQFP	650	mW
Storage Temperature	$T_{STG}$	—		-50 to +150	°C

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Condition		Rated value	Unit
Digital power supply voltage	$V_{DD}$	MSM66577	$f_{OSC} \leq 30$ MHz	4.5 to 5.5	V
		MSM66Q577	$f_{OSC} \leq 30$ MHz	4.5 to 5.5	
		MSM66577L	$f_{OSC} \leq 14$ MHz	2.4 to 3.6	
		MSM66Q577LY	$f_{OSC} \leq 14$ MHz	3.0 to 3.6	
Analog reference voltage	$V_{REF}$	—		$V_{DD} - 0.3$ to $V_{DD}$	V
Analog input voltage	$V_{AI}$	—		AGND to $V_{REF}$	V
Memory hold voltage	$V_{DDH}$	MSM66577	$f_{OSC} = 0$ Hz	2.0 to 5.5	V
		MSM66Q577			
		MSM66577L		2.0 to 3.6	
		MSM66Q577LY			
Operating frequency	$f_{OSC}$	MSM66577	$V_{DD} = 4.5$ to 5.5 V	2 to 30	MHz
		MSM66Q577	$V_{DD} = 4.5$ to 5.5 V	2 to 30	
		MSM66577L	$V_{DD} = 2.4$ to 3.6 V	2 to 14	
		MSM66Q577LY	$V_{DD} = 3.0$ to 3.6V	2 to 14	
	$f_{XT}$	—		32.768	kHz
Ambient temperature	Ta	—		-30 to +70	°C
Fan out	N	MOS load		20	—
		TTL load	P0, P3, P11	6	—
			P1, P2, P4, P5, P6, P7, P8, P9, P10, P14, P15	1	—

**ALLOWABLE OUTPUT CURRENT VALUES**MSM66577/Q577 ( $V_{DD} = 4.5$  to  $5.5$  V,  $T_a = -30$  to  $+70^\circ\text{C}$ )MSM66577L ( $V_{DD} = 2.4$  to  $3.6$  V,  $T_a = -30$  to  $+70^\circ\text{C}$ )MSM66Q577LY ( $V_{DD} = 3.0$  to  $3.6$  V,  $T_a = -30$  to  $+70^\circ\text{C}$ )

Parameter	Pin	Symbol	Min.	Typ.	Max.	Unit
"H" output pin (1 pin)	All output pins	$I_{OH}$	—	—	-2	mA
"H" output pins (sum total)	Sum total of all output pins	$\Sigma I_{OH}$	—	—	-40	
"L" output pin (1 pin)	P0, P3, P11	$I_{OL}$	—	—	10	
	Other ports				5	
"L" output pins (sum total)	Sum total of P0, P3, P11	$\Sigma I_{OL}$	—	—	80	
	Sum total of P1, P2, P4				50	
	Sum total of P5, P6, P9					
	Sum total of P7, P8, P10, P14, P15					
	Sum total of all output pins					

**[Note]**

Each of the family devices has unique pattern routes for the internal power and ground. Connect the power supply voltage to all  $V_{DD}$  pins and the ground potential to all GND pins. If a device may have one or more  $V_{DD}$  or GND pins to which the power supply voltage or the ground potential is not connected, it can not be guaranteed for normal operation.

**INTERNAL FLASH ROM PROGRAMMING CONDITIONS**

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	$V_{DD}$	MSM66Q577	4.5 to 5.5	V
		MSM66Q577LY	3.0 to 3.6	
Ambient Temperature	$T_a$	During Read	-30 to +70	$^\circ\text{C}$
		During Programming	+0 to +50	
Endurance	CEP	—	100	Cycles
Blocks size	—	—	128	bytes

## ELECTRICAL CHARACTERISTICS

DC Characteristics 1 ( $V_{DD} = 4.5$  to  $5.5$  V)MSM66577/Q577 ( $V_{DD} = 4.5$  to  $5.5$  V,  $T_a = -30$  to  $+70^\circ\text{C}$ )

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage *1	$V_{IH}$	—	$0.44V_{DD}$	—	$V_{DD}+0.3$	V
"H" input voltage *2,*3,*4,*5,*6			$0.80V_{DD}$	—	$V_{DD}+0.3$	
"L" input voltage *1	$V_{IL}$	—	-0.3	—	$0.16V_{DD}$	
"L" input voltage *2,*3,*4,*5,*6			-0.3	—	$0.20V_{DD}$	
"H" output voltage *1, *4	$V_{OH}$	$I_O = -400 \mu\text{A}$	$V_{DD}-0.4$	—	—	
		$I_O = -2.0 \text{ mA}$	$V_{DD}-0.6$	—	—	
$I_O = -200 \mu\text{A}$		$V_{DD}-0.4$	—	—		
$I_O = -1.0 \text{ mA}$		$V_{DD}-0.6$	—	—		
"L" output voltage *1, *4	$V_{OL}$	$I_O = 3.2 \text{ mA}$	—	—	0.4	
		$I_O = 10.0 \text{ mA}$	—	—	0.8	
$I_O = 1.6 \text{ mA}$		—	—	0.4		
$I_O = 5.0 \text{ mA}$		—	—	0.8		
Input leakage current *3	$I_{IH}/I_{IL}$	$V_I = V_{DD}/0 \text{ V}$	—	—	1/-1	$\mu\text{A}$
Input current *5			—	—	1/-250	
Input current *6			—	—	15/-15	
Output leakage current *1, *2, *4	$I_{LO}$	$V_O = V_{DD}/0 \text{ V}$	—	—	$\pm 10$	$\mu\text{A}$
Pull-up resistance	$R_{pull}$	$V_I = 0 \text{ V}$	25	50	100	$k\Omega$
Input capacitance	$C_I$	$f_{OSC} = 1 \text{ MHz}, T_a = 25^\circ\text{C}$	—	5	—	$\text{pF}$
Output capacitance	$C_O$		—	7	—	
Analog reference supply current	$I_{REF}$	During A/D operation	—	—	4	$\text{mA}$
		When A/D is stopped	—	—	10	$\mu\text{A}$

\*1: Applicable to P0

\*2: Applicable to P1, P2, P4, P5, P6, P7, P8, P9, P10, P14, P15

\*3: Applicable to P12, SELMBUS,  $\overline{\text{EA}}$ , NMI

\*4: Applicable to P3, P11

\*5: Applicable to  $\overline{\text{RES}}$ 

\*6: Applicable to OSC0

Supply current ( $V_{DD}=4.5$  to  $5.5$  V)MSM66577/Q577 ( $V_{DD}=4.5$  to  $5.5$  V,  $T_a=-30$  to  $+70^\circ\text{C}$ )

Mode	Symbol	Condition	Min.	Typ.	Max.	Unit	
CPU operation mode *1	$I_{DD}$	$f_{OSC} = 30 \text{ MHz}$	—	60	80	$\text{mA}$	
		$f_{XT} = 32.768 \text{ kHz}$	MSM66577	—	80	180	$\mu\text{A}$
			MSM66Q577	—	500	800	$\mu\text{A}$
HALT mode *2	$I_{DDH}$	$f_{OSC} = 30 \text{ MHz}$	—	40	60	$\text{mA}$	
STOP mode *3	$I_{DDs}$	OSC is stopped	XT is used	—	5	110	$\mu\text{A}$
			XT is not used	—	1	100	
		OSC is stopped, XT is not used $V_{DD}=2 \text{ V}, T_a=25^\circ\text{C}$	—	0.2	10		

[Note] Ports used as inputs are at  $V_{DD}$  or 0 V. Other ports are unloaded.

\*1. CPU and all the peripheral functions (timer, PWM, A/D, etc.) are activated.

\*2. CPU is stopped, and all the peripheral functions (timer, PWM, A/D, etc.) are activated.

\*3. CPU and all the peripheral functions are deactivated (The clock timer is being activated when the XT is used).

DC Characteristics 2 ( $V_{DD} = 2.4$  to  $3.6$  V)MSM66577L ( $V_{DD} = 2.4$  to  $3.6$  V,  $T_a = -30$  to  $+70^\circ\text{C}$ )MSM66Q577LY ( $V_{DD} = 3.0$  to  $3.6$  V,  $T_a = -30$  to  $+70^\circ\text{C}$ )

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage *1	$V_{IH}$	—	$0.55V_{DD}$	—	$V_{DD}+0.3$	V
"H" input voltage *2,*3,*4,*5,*6		—	$0.80V_{DD}$	—	$V_{DD}+0.3$	
"L" input voltage *1	$V_{IL}$	—	-0.3	—	$0.16V_{DD}$	
"L" input voltage *2,*3,*4,*5,*6		—	-0.3	—	$0.20V_{DD}$	
"H" output voltage *1, *4	$V_{OH}$	$I_O = -400 \mu\text{A}$	$V_{DD}-0.4$	—	—	
"H" output voltage *2		$I_O = -2.0 \text{ mA}$	$V_{DD}-0.8$	—	—	
		$I_O = -200 \mu\text{A}$	$V_{DD}-0.4$	—	—	
		$I_O = -1.0 \text{ mA}$	$V_{DD}-0.8$	—	—	
"L" output voltage *1, *4	$V_{OL}$	$I_O = 3.2 \text{ mA}$	—	—	0.5	
"L" output voltage *2		$I_O = 5.0 \text{ mA}$	—	—	0.9	
		$I_O = 1.6 \text{ mA}$	—	—	0.5	
		$I_O = 2.5 \text{ mA}$	—	—	0.9	
Input leakage current *3	$I_{IH}/I_{IL}$	$V_I = V_{DD}/0 \text{ V}$	—	—	1/-1	$\mu\text{A}$
Input current *5			—	—	1/-250	
Input current *6			—	—	15/-15	
Output leakage current *1, *2, *4	$I_{LO}$	$V_O = V_{DD}/0 \text{ V}$	—	—	$\pm 10$	$\mu\text{A}$
Pull-up resistance	$R_{pull}$	$V_I = 0 \text{ V}$	40	100	200	$\text{k}\Omega$
Input capacitance	$C_i$	$f_{osc} = 1 \text{ MHz}, T_a = 25^\circ\text{C}$	—	5	—	$\text{pF}$
Output capacitance	$C_o$		—	7	—	
Analog reference supply current	$I_{REF}$	During A/D operation	—	—	2	$\text{mA}$
		When A/D is stopped	—	—	5	$\mu\text{A}$

\*1: Applicable to P0

\*2: Applicable to P1, P2, P4, P5, P6, P7, P8, P9, P10, P14, P15

\*3: Applicable to P12, SELMBUS,  $\overline{\text{EA}}$ , NMI

\*4: Applicable to P3, P11

\*5: Applicable to  $\overline{\text{RES}}$ 

\*6: Applicable to OSC0

Supply current ( $V_{DD}=2.4$  to  $3.6$  V)MSM66577L ( $V_{DD} = 2.4$  to  $3.6$  V,  $T_a = -30$  to  $+70^\circ\text{C}$ )MSM66Q577LY ( $V_{DD} = 3.0$  to  $3.6$  V,  $T_a = -30$  to  $+70^\circ\text{C}$ )

Mode	Symbol	Condition	Min.	Typ.	Max.	Unit	
CPU operation mode *1	$I_{DD}$	$f_{osc} = 14 \text{ MHz}$	—	15	25	$\text{mA}$	
		$f_{XT} = 32.768 \text{ kHz}$	MSM66577L	—	50	150	$\mu\text{A}$
			MSM66Q577LY	—	300	600	$\mu\text{A}$
HALT mode *2	$I_{DDH}$	$f_{osc} = 14 \text{ MHz}$	—	10	17	$\text{mA}$	
STOP mode *3	$I_{DDS}$	OSC is stopped	XT is used*	—	3	110	$\mu\text{A}$
			XT is not used*	—	1	100	
		OSC is stopped, XT is not used $V_{DD}=2 \text{ V}, T_a=25^\circ\text{C}$ *	—	0.2	10		

[Note] Ports used as inputs are at  $V_{DD}$  or 0 V. Other ports are unloaded.

\*1. CPU and all the peripheral functions (timer, PWM, A/D, etc.) are activated.

\*2. CPU is stopped, and all the peripheral functions (timer, PWM, A/D, etc.) are activated.

\*3. CPU and all the peripheral functions are deactivated (The clock timer is being activated when the XT is used).

AC Characteristics 1 ( $V_{DD} = 4.5$  to  $5.5$  V)

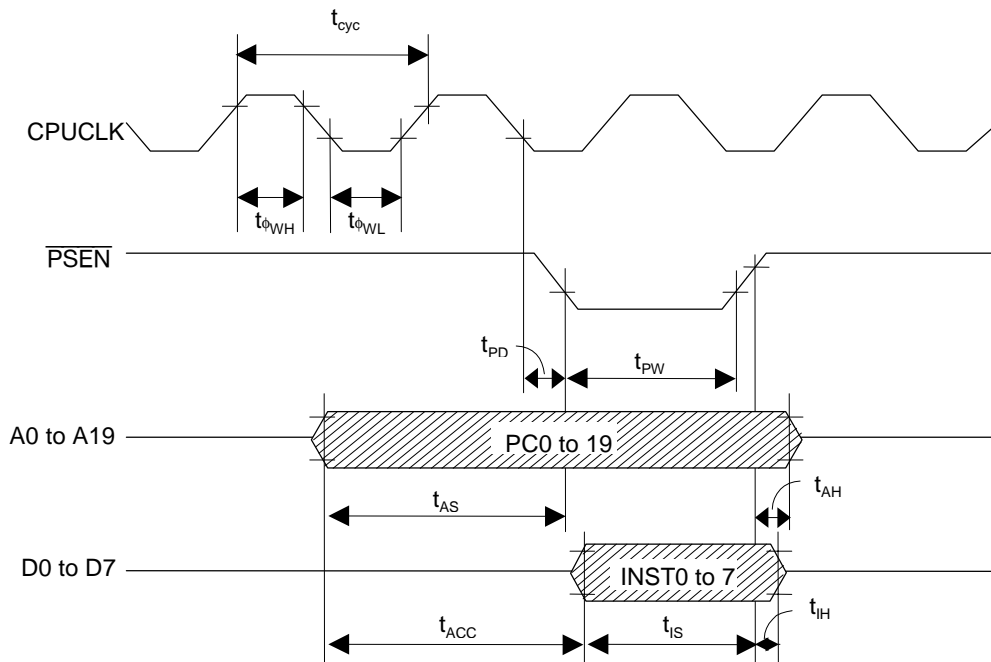
(1) Separate Bus Type

External program memory control

MSM66577/Q577 ( $V_{DD} = 4.5$  to  $5.5$  V,  $T_a = -30$  to  $+70^\circ\text{C}$ )

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	$t_{cyc}$	$f_{OSC} = 30$ MHz	33.3	—	ns
Clock pulse width (HIGH level)	$t_{\phi WH}$	$C_L = 50$ pF	13	—	
Clock pulse width (LOW level)	$t_{\phi WL}$		13	—	
$\overline{\text{PSEN}}$ pulse width	$t_{PW}$		$2 t\phi - 15$	—	
$\overline{\text{PSEN}}$ pulse delay time	$t_{PD}$		—	45	
Address setup time	$t_{AS}$		$t\phi - 25$	—	
Address hold time	$t_{AH}$		0	—	
Instruction setup time	$t_{IS}$		25	—	
Instruction hold time	$t_{IH}$		0	—	
Read data access time	$t_{ACC}$		—	—	

Note:  $t\phi = t_{cyc}/2$



Bus timing during no wait cycle time

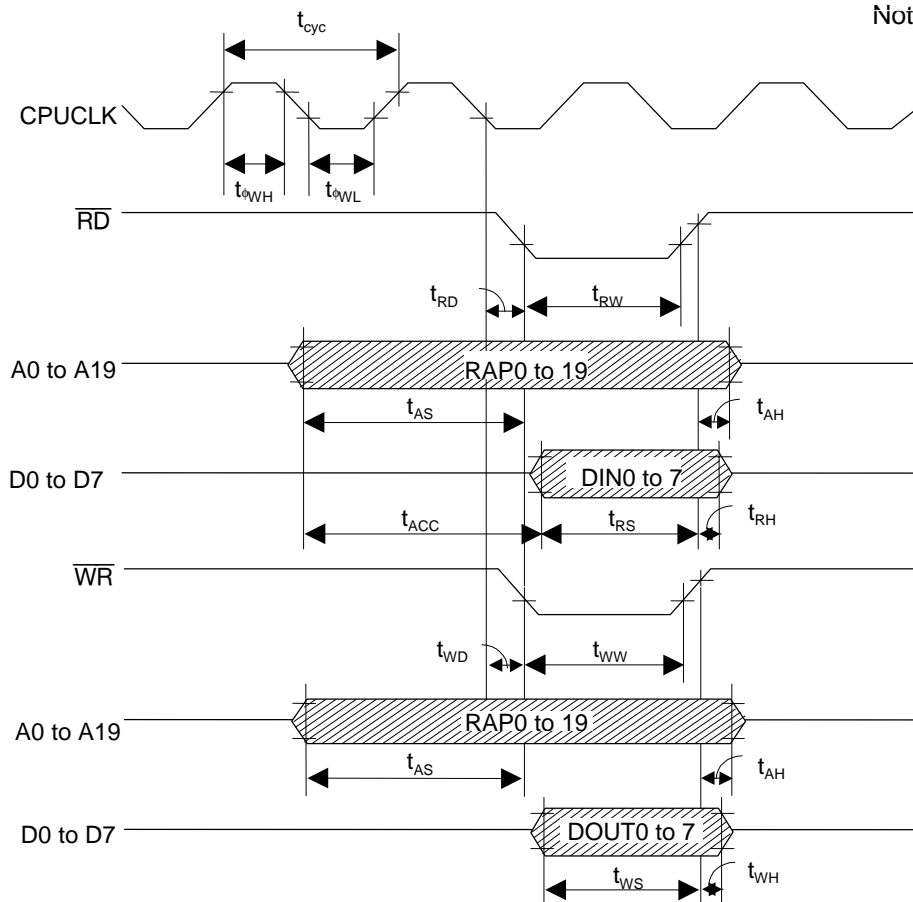
\*1: The read data access time ( $t_{ACC}$ ) is  $(3+2n) t\phi - 65$  when  $n$  wait cycles are inserted.

External data memory control

MSM66577/Q577 ( $V_{DD} = 4.5$  to  $5.5$  V,  $T_a = -30$  to  $+70^\circ\text{C}$ )

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	$t_{cyc}$	$f_{OSC} = 30$ MHz	33.3	—	ns
Clock pulse width (HIGH level)	$t_{\phi WH}$	$C_L = 50$ pF	13	—	
Clock pulse width (LOW level)	$t_{\phi WL}$		13	—	
$\overline{RD}$ pulse width	$t_{RW}$		$2\phi - 15$	—	
$\overline{WR}$ pulse width	$t_{WW}$		$2\phi - 15$	—	
$\overline{RD}$ pulse delay time	$t_{RD}$		—	45	
$\overline{WR}$ pulse delay time	$t_{WD}$		—	45	
Address setup time	$t_{AS}$		$t\phi - 25$	—	
Address hold time	$t_{AH}$		$t\phi - 3$	—	
Read data setup time	$t_{RS}$		25	—	
Read data hold time	$t_{RH}$		0	—	
Read data access time	$t_{ACC}$		—	$3t\phi - 65^*1$	
Write data setup time	$t_{WS}$		$2t\phi - 30$	—	
Write data hold time	$t_{WH}$		$t\phi - 3$	—	

Note:  $t\phi = t_{cyc}/2$



Bus timing during no wait cycle time

\*1: The read data access time ( $t_{ACC}$ ) is  $(3+2n)t\phi - 65$  when  $n$  wait cycles are inserted.

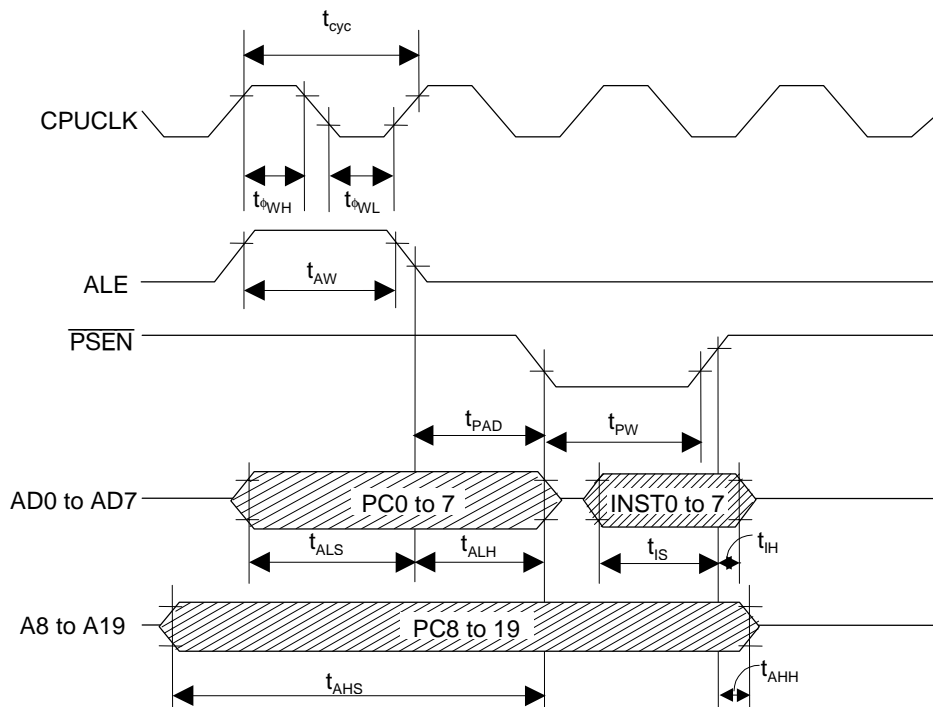
(2) Multiplexed bus type

External program memory control

MSM66577/Q577 ( $V_{DD} = 4.5$  to  $5.5$  V,  $T_a = -30$  to  $+70^\circ\text{C}$ )

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	$t_{cyc}$	$f_{OSC} = 30$ MHz	33.3	—	ns
Clock pulse width (HIGH level)	$t_{\phi WH}$	$C_L = 50$ pF	13	—	
Clock pulse width (LOW level)	$t_{\phi WL}$		13	—	
ALE pulse width	$t_{AW}$		$2\phi - 10$	—	
$\overline{\text{PSEN}}$ pulse width	$t_{PW}$		$2\phi - 15$	—	
$\overline{\text{PSEN}}$ pulse delay time	$t_{PAD}$		$\phi - 3$	—	
Low address setup time	$t_{ALS}$		$2\phi - 15$	—	
Low address hold time	$t_{ALH}$		$\phi - 3$	—	
High address setup time	$t_{AHS}$		$3\phi - 25$	—	
High address hold time	$t_{AHH}$		0	—	
Instruction setup time	$t_{IS}$		25	—	
Instruction hold time	$t_{IH}$		0	$\phi - 3$	

Note:  $t\phi = t_{cyc}/2$



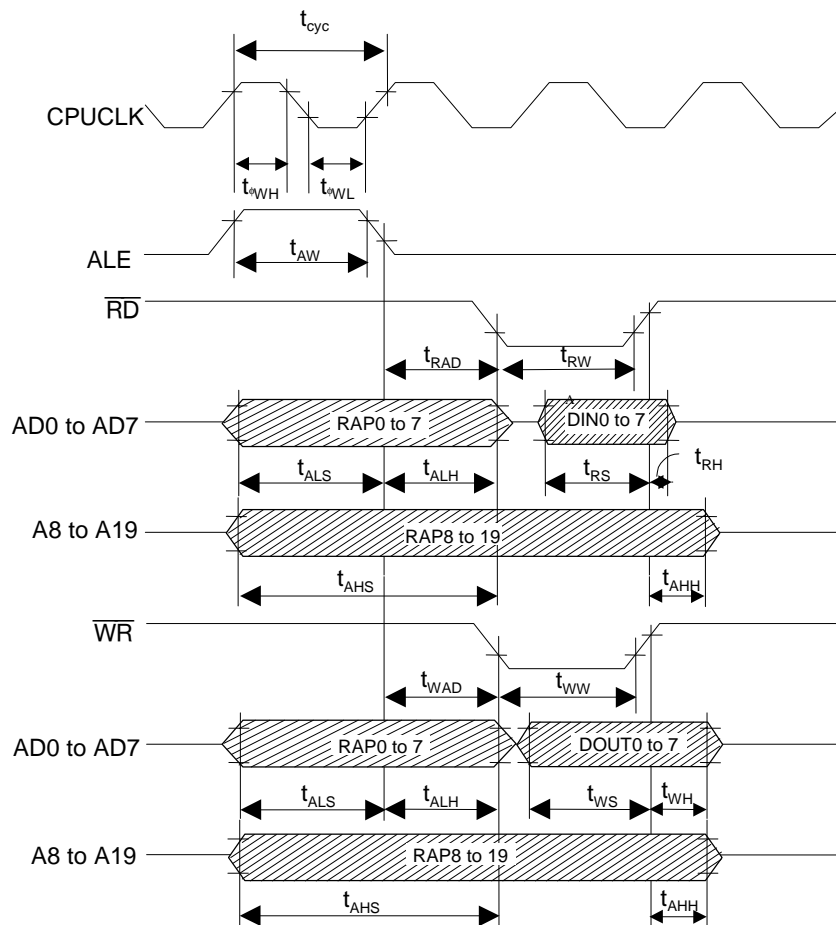
Bus timing during no wait cycle time



External data memory control

MSM66577/Q577 ( $V_{DD} = 4.5$  to  $5.5$  V,  $T_a = -30$  to  $+70^\circ\text{C}$ )

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	$t_{cyc}$	$f_{OSC} = 30$ MHz	33.3	—	ns
Clock pulse width (HIGH level)	$t_{\phi WH}$	$C_L = 50$ pF	13	—	
Clock pulse width (LOW level)	$t_{\phi WL}$		13	—	
ALE pulse width	$t_{AW}$		$2\phi - 10$	—	
$\overline{RD}$ pulse width	$t_{RW}$		$2\phi - 15$	—	
$\overline{WR}$ pulse width	$t_{WW}$		$2\phi - 15$	—	
$\overline{RD}$ pulse delay time	$t_{RAD}$		$\phi - 3$	—	
$\overline{WR}$ pulse delay time	$t_{WAD}$		$\phi - 3$	—	
Low address setup time	$t_{ALS}$		$2\phi - 15$	—	
Low address hold time	$t_{ALH}$		$\phi - 3$	—	
High address setup time	$t_{AHS}$		$3\phi - 25$	—	
High address hold time	$t_{AHH}$		$\phi - 3$	—	
Read data setup time	$t_{RS}$		25	—	
Read data hold time	$t_{RH}$		0	$\phi - 3$	
Write data setup time	$t_{WS}$		$2\phi - 30$	—	
Write data hold time	$t_{WH}$		$\phi - 3$	—	



Note:  $t_{\phi} = t_{cyc}/2$

Bus timing during no wait cycle time

(3) Serial port control

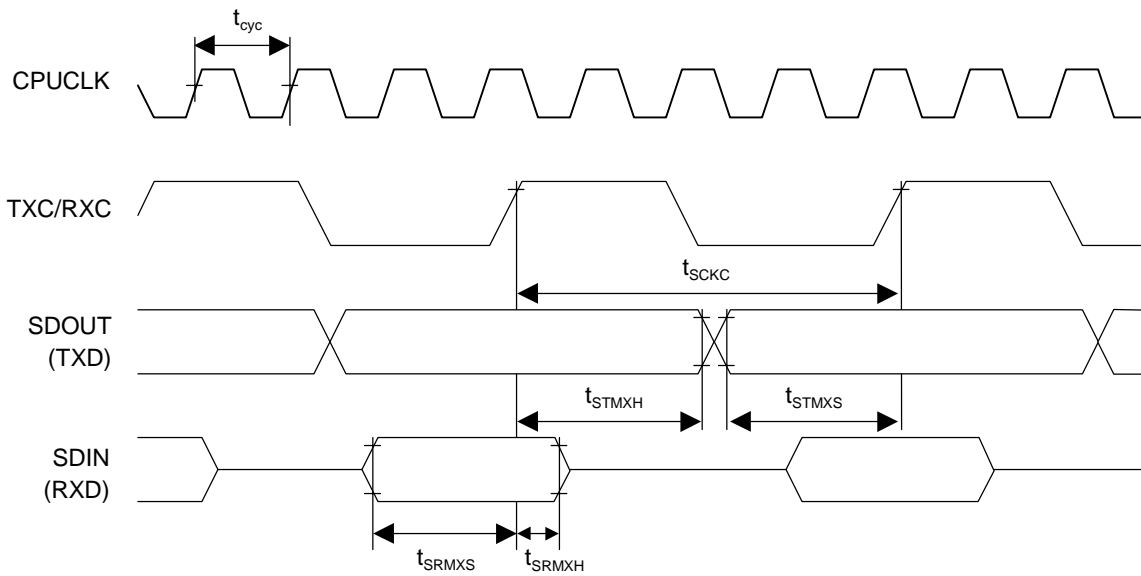
Serial ports 1 and 6 (SIO1 and 6)

Master mode (Clock synchronous serial port)

MSM66577/Q577 ( $V_{DD} = 4.5$  to  $5.5$  V,  $T_a = -30$  to  $+70^\circ\text{C}$ )

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	$t_{cyc}$	$f_{OSC} = 30$ MHz	33.3	—	ns
Serial clock cycle time	$t_{SCKC}$	$C_L = 50$ pF	$4 t_{cyc}$	—	
Output data setup time	$t_{STMXS}$		$2 t\phi - 5$	—	
Output data hold time	$t_{STMXH}$		$5 t\phi - 10$	—	
Input data setup time	$t_{SRMXS}$		13	—	
Input data hold time	$t_{SRMXH}$		0	—	

Note:  $t\phi = t_{cyc}/2$

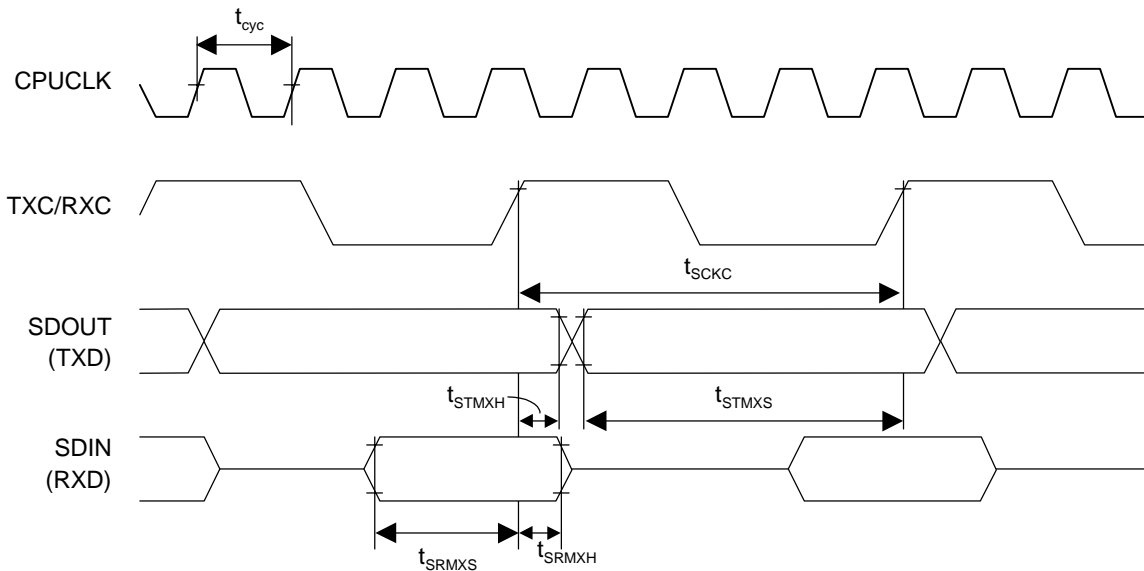


Slave mode (Clock synchronous serial port)

MSM66577/Q577 ( $V_{DD} = 4.5$  to  $5.5$  V,  $T_a = -30$  to  $+70^\circ\text{C}$ )

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	$t_{cyc}$	$f_{OSC} = 30$ MHz	33.3	—	ns
Serial clock cycle time	$t_{SCKC}$	$C_L = 50$ pF	$4 t_{cyc}$	—	
Output data setup time	$t_{STMXS}$		$2 t\phi - 15$	—	
Output data hold time	$t_{STMXH}$		$4 t\phi - 10$	—	
Input data setup time	$t_{SRMXS}$		13	—	
Input data hold time	$t_{SRMXH}$		3	—	

Note:  $t\phi = t_{cyc}/2$



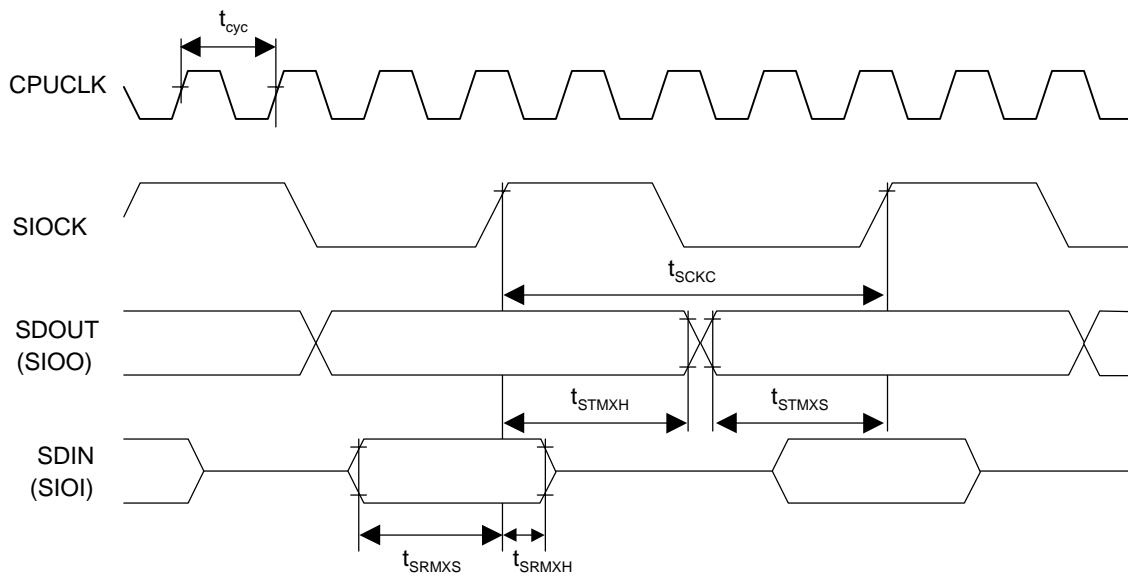
Serial ports 4 and 5 (SIO4 and 5)

Master mode (Clock synchronous serial port)

MSM66577/Q577 ( $V_{DD} = 4.5$  to  $5.5$  V,  $T_a = -30$  to  $+70^\circ\text{C}$ )

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	$t_{cyc}$	$f_{OSC} = 30$ MHz	33.3	—	ns
Serial clock cycle time	$t_{SCKC}$	$C_L = 50$ pF	200	—	
Output data setup time	$t_{STMXS}$		$6 t\phi - 5$	—	
Output data hold time	$t_{STMXH}$		$4.5 t\phi - 10$	—	
Input data setup time	$t_{SRMXS}$		13	—	
Input data hold time	$t_{SRMXH}$		0	—	

Note:  $t\phi = t_{cyc}/2$

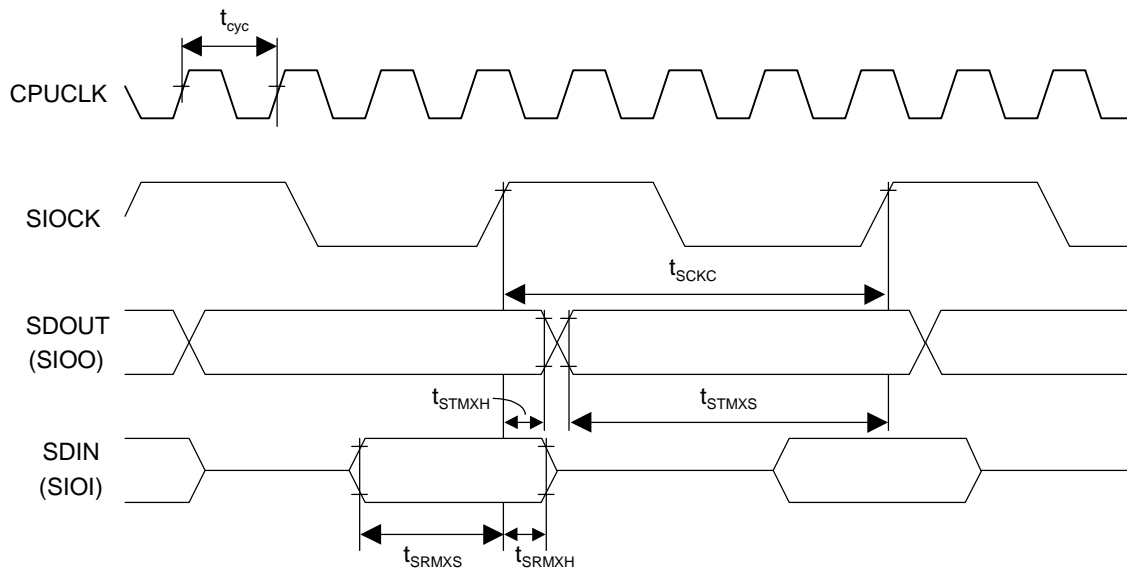


Slave mode (Clock synchronous serial port)

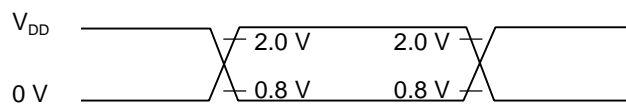
MSM66577/Q577 ( $V_{DD} = 4.5$  to  $5.5$  V,  $T_a = -30$  to  $+70^\circ\text{C}$ )

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	$t_{cyc}$	$f_{OSC} = 30$ MHz	33.3	—	ns
Serial clock cycle time	$t_{SCKC}$	$C_L = 50$ pF	200	—	
Output data setup time	$t_{STMXS}$		$3 t\phi - 15$	—	
Output data hold time	$t_{STMXH}$		$6 t\phi - 10$	—	
Input data setup time	$t_{SRMXS}$		13	—	
Input data hold time	$t_{SRMXH}$		3	—	

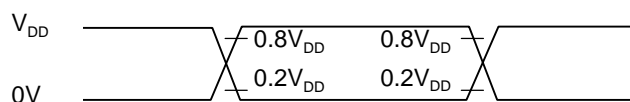
Note:  $t\phi = t_{cyc}/2$



Measurement points for AC timing (except the serial port)



Measurement points for AC timing (the serial port)



AC Characteristics 2 ( $V_{DD} = 2.4$  to  $3.6$  V)

(1) Separate Bus Type

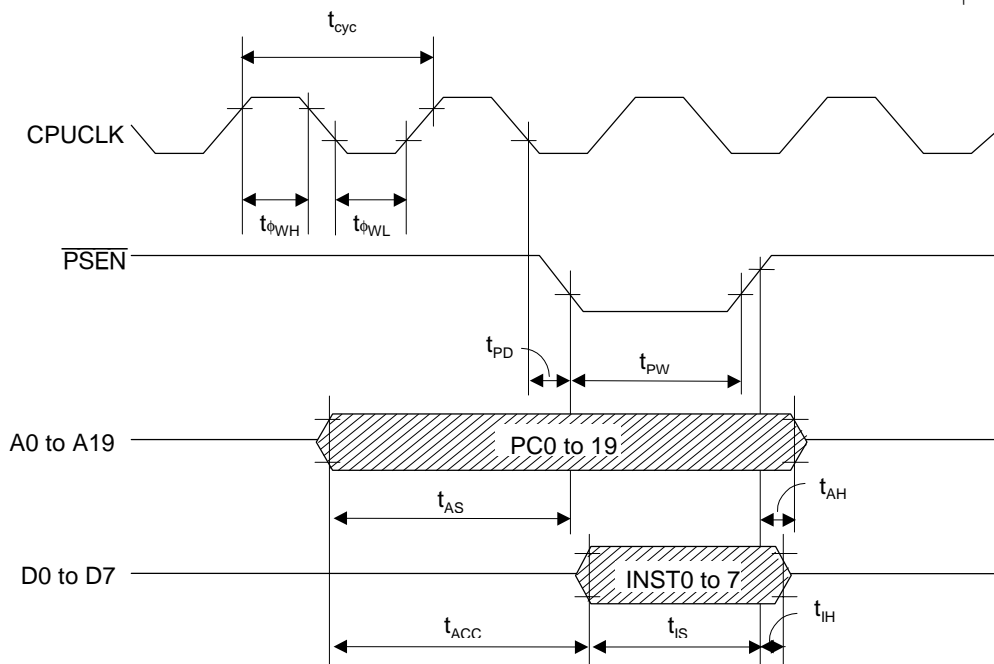
External program memory control

MSM66577L ( $V_{DD} = 2.4$  to  $3.6$  V,  $T_a = -30$  to  $+70^\circ\text{C}$ )

MSM66Q577LY ( $V_{DD} = 3.0$  to  $3.6$  V,  $T_a = -30$  to  $+70^\circ\text{C}$ )

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	$t_{cyc}$	$f_{OSC} = 14$ MHz	71.4	—	ns
Clock pulse width (HIGH level)	$t_{\phi WH}$	$C_L = 50$ pF	28	—	
Clock pulse width (LOW level)	$t_{\phi WL}$		28	—	
$\overline{\text{PSEN}}$ pulse width	$t_{PW}$		$2\phi - 40$	—	
$\overline{\text{PSEN}}$ pulse delay time	$t_{PD}$		—	95	
Address setup time	$t_{AS}$		$t\phi - 45$	—	
Address hold time	$t_{AH}$		0	—	
Instruction setup time	$t_{IS}$		75	—	
Instruction hold time	$t_{IH}$		0	—	
Read data access time	$t_{ACC}$		—	$3\phi - 120^{*1}$	

Note:  $t\phi = t_{cyc}/2$



Bus timing during no wait cycle time

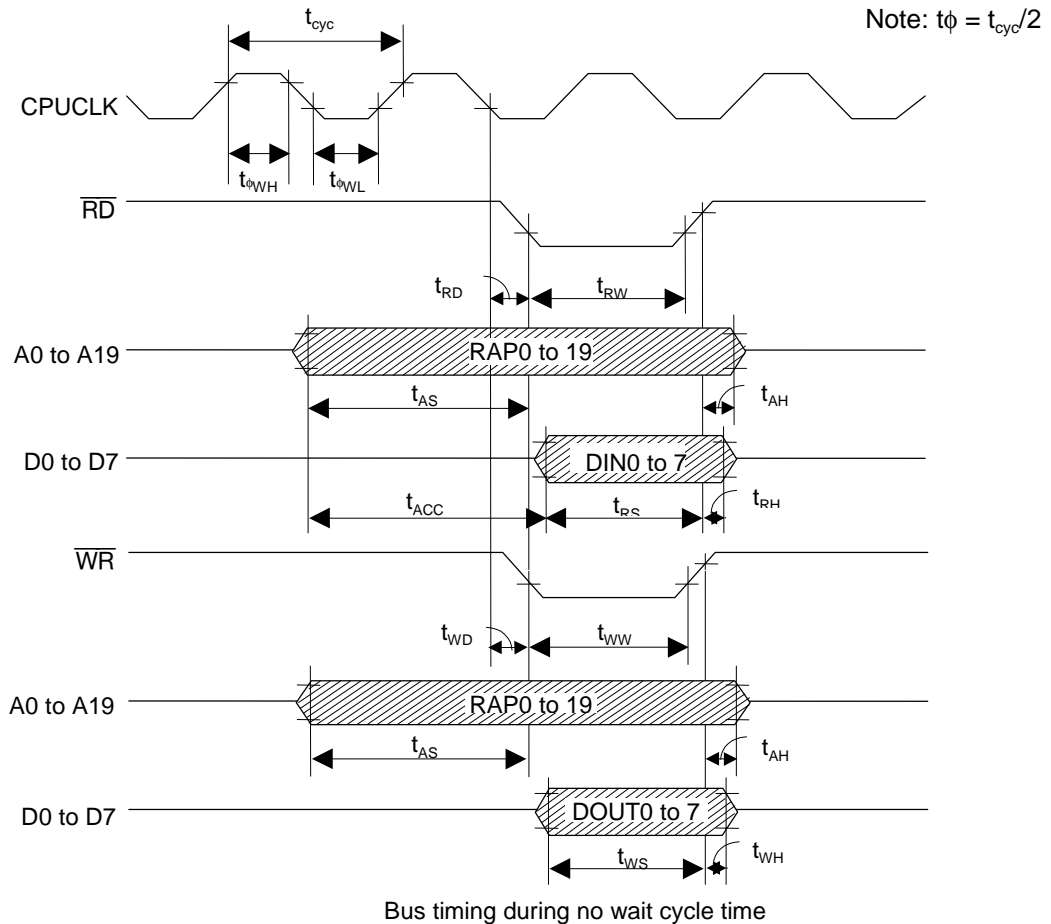
\*1: The read data access time ( $t_{ACC}$ ) is  $(3+2n)\phi - 120$  when  $n$  wait cycles are inserted.

External data memory control

MSM66577L ( $V_{DD} = 2.4$  to  $3.6$  V,  $T_a = -30$  to  $+70^\circ\text{C}$ )

MSM66Q577LY ( $V_{DD} = 3.0$  to  $3.6$  V,  $T_a = -30$  to  $+70^\circ\text{C}$ )

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	$t_{cyc}$	$f_{OSC} = 14$ MHz	71.4	—	ns
Clock pulse width (HIGH level)	$t_{\phi WH}$	$C_L = 50$ pF	28	—	
Clock pulse width (LOW level)	$t_{\phi WL}$		28	—	
$\overline{RD}$ pulse width	$t_{RW}$		$2\phi - 40$	—	
$\overline{WR}$ pulse width	$t_{WW}$		$2\phi - 40$	—	
$\overline{RD}$ pulse delay time	$t_{RD}$		—	95	
$\overline{WR}$ pulse delay time	$t_{WD}$		—	95	
Address setup time	$t_{AS}$		$\phi - 45$	—	
Address hold time	$t_{AH}$		$\phi - 6$	—	
Read data setup time	$t_{RS}$		75	—	
Read data hold time	$t_{RH}$		0	—	
Read data access time	$t_{ACC}$		—	$3\phi - 120^*1$	
Write data setup time	$t_{WS}$		$2\phi - 55$	—	
Write data hold time	$t_{WH}$		$\phi - 6$	—	



\*1: The read data access time ( $t_{ACC}$ ) is  $(3+2n)\phi - 120$  when  $n$  wait cycles are inserted.

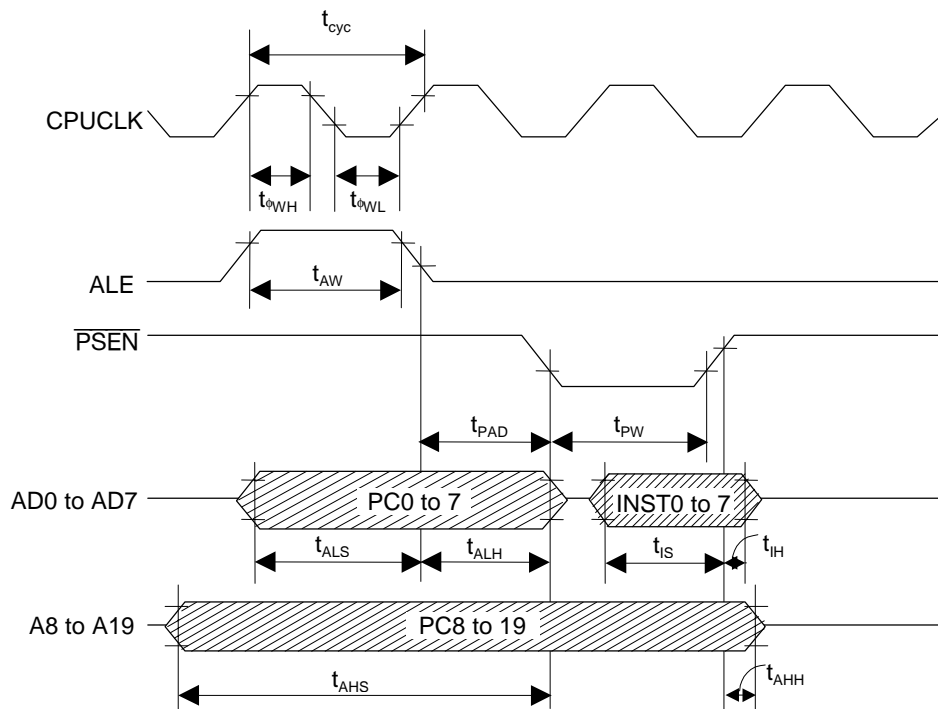
(2) Multiplexed bus type

External program memory control

MSM66577L ( $V_{DD} = 2.4$  to  $3.6$  V,  $T_a = -30$  to  $+70^\circ\text{C}$ )  
 MSM66Q577LY ( $V_{DD} = 3.0$  to  $3.6$  V,  $T_a = -30$  to  $+70^\circ\text{C}$ )

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	$t_{cyc}$	$f_{OSC} = 14$ MHz	71.4	—	ns
Clock pulse width (HIGH level)	$t_{\phi WH}$	$C_L = 50$ pF	28	—	
Clock pulse width (LOW level)	$t_{\phi WL}$		28	—	
ALE pulse width	$t_{AW}$		$2\phi - 15$	—	
$\overline{\text{PSEN}}$ pulse width	$t_{PW}$		$2\phi - 40$	—	
$\overline{\text{PSEN}}$ pulse delay time	$t_{PAD}$		$\phi - 6$	—	
Low address setup time	$t_{ALS}$		$2\phi - 25$	—	
Low address hold time	$t_{ALH}$		$\phi - 6$	—	
High address setup time	$t_{AHS}$		$3\phi - 45$	—	
High address hold time	$t_{AHH}$		0	—	
Instruction setup time	$t_{IS}$		75	—	
Instruction hold time	$t_{IH}$		0	$\phi - 6$	

Note:  $\phi = t_{cyc}/2$



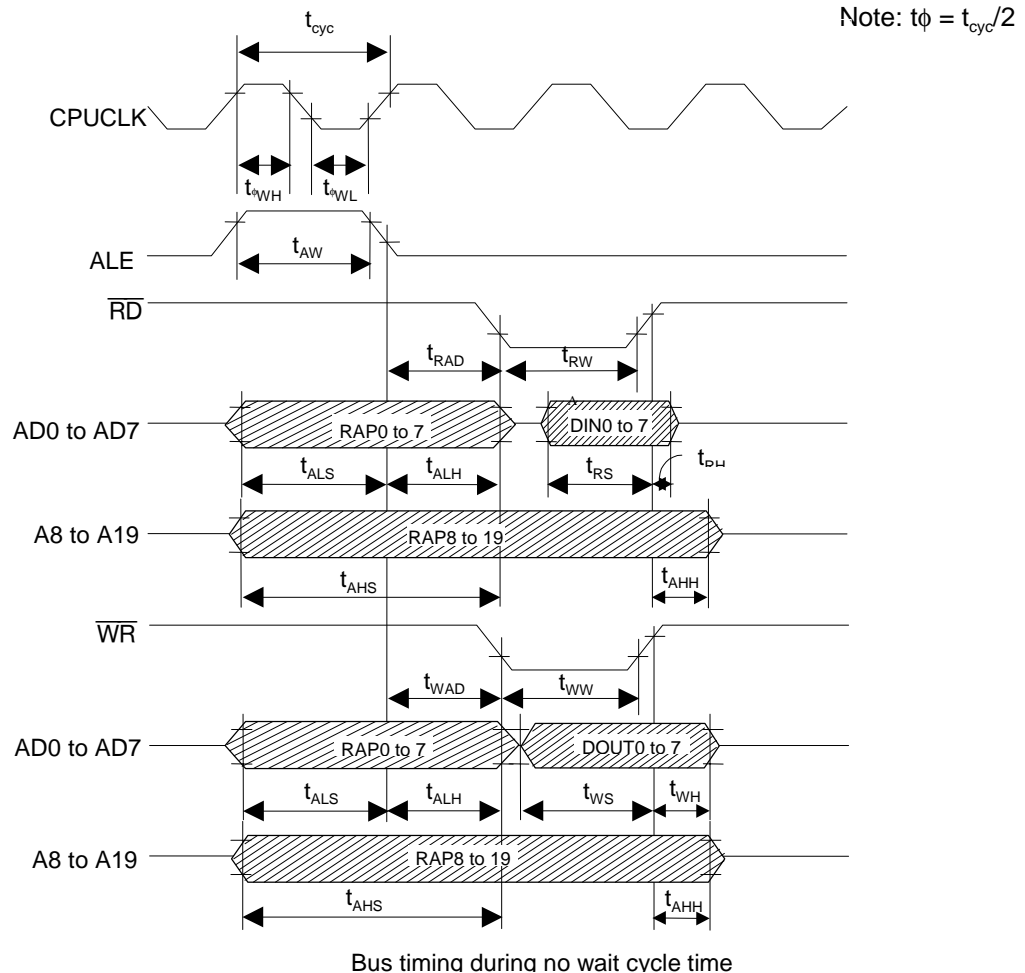


External data memory control

MSM66577L ( $V_{DD} = 2.4$  to  $3.6$  V,  $T_a = -30$  to  $+70^\circ\text{C}$ )

MSM66Q577LY ( $V_{DD} = 3.0$  to  $3.6$  V,  $T_a = -30$  to  $+70^\circ\text{C}$ )

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	$t_{cyc}$	$f_{OSC} = 14$ MHz	71.4	—	ns
Clock pulse width (HIGH level)	$t_{\phi WH}$	$C_L = 50$ pF	28	—	
Clock pulse width (LOW level)	$t_{\phi WL}$		28	—	
ALE pulse width	$t_{AW}$		$2\phi - 15$	—	
$\overline{RD}$ pulse width	$t_{RW}$		$2\phi - 40$	—	
$\overline{WR}$ pulse width	$t_{WW}$		$2\phi - 40$	—	
$\overline{RD}$ pulse delay time	$t_{RAD}$		$\phi - 6$	—	
$\overline{WR}$ pulse delay time	$t_{WAD}$		$\phi - 6$	—	
Low address setup time	$t_{ALS}$		$2\phi - 25$	—	
Low address hold time	$t_{ALH}$		$\phi - 6$	—	
High address setup time	$t_{AHS}$		$3\phi - 45$	—	
High address hold time	$t_{AHH}$		$\phi - 6$	—	
Read data setup time	$t_{RS}$		75	—	
Read data hold time	$t_{RH}$		0	$\phi - 6$	
Write data setup time	$t_{WS}$		$2\phi - 55$	—	
Write data hold time	$t_{WH}$		$\phi - 6$	—	



Bus timina during no wait cycle time

(3) Serial port control

Serial ports 1 and 6 (SIO1 and 6)

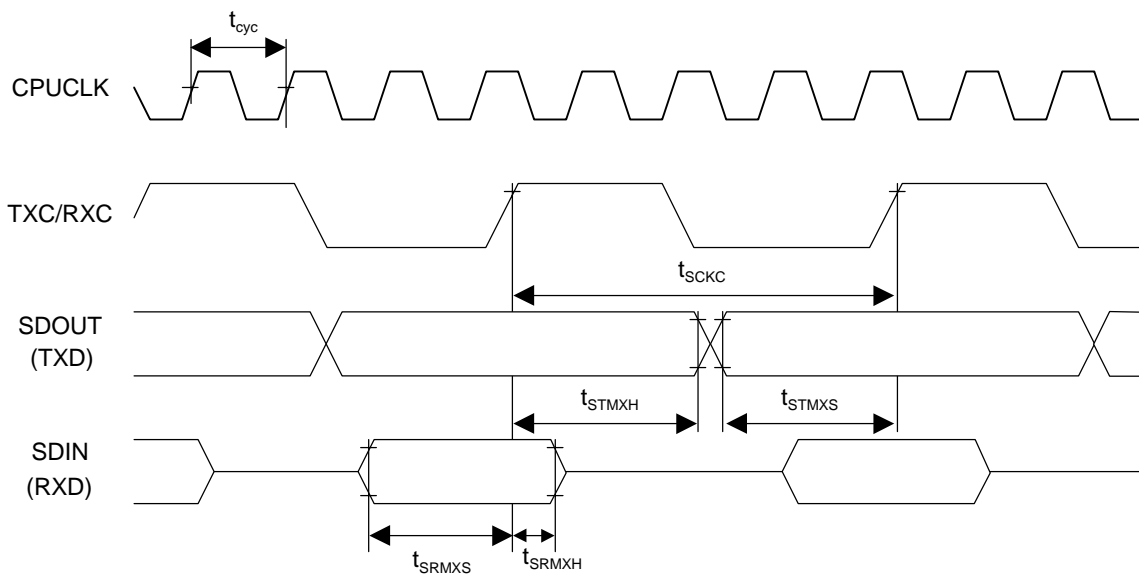
Master mode (Clock synchronous serial port)

MSM66577L ( $V_{DD} = 2.4$  to  $3.6$  V,  $T_a = -30$  to  $+70^\circ\text{C}$ )

MSM66Q577LY ( $V_{DD} = 3.0$  to  $3.6$  V,  $T_a = -30$  to  $+70^\circ\text{C}$ )

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	$t_{cyc}$	$f_{OSC} = 14$ MHz	71.4	—	ns
Serial clock cycle time	$t_{SCKC}$	$C_L = 50$ pF	$4 t_{cyc}$	—	
Output data setup time	$t_{STMXS}$		$2 \phi - 10$	—	
Output data hold time	$t_{STMXH}$		$5 \phi - 20$	—	
Input data setup time	$t_{SRMXS}$		21	—	
Input data hold time	$t_{SRMXH}$		0	—	

Note:  $\phi = t_{cyc}/2$



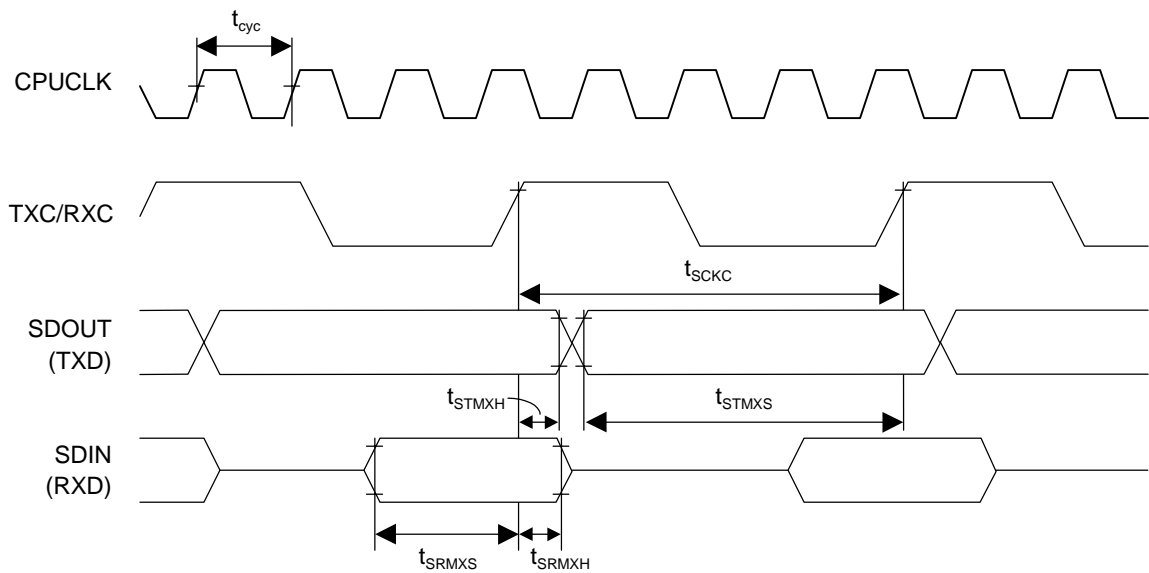
Slave mode (Clock synchronous serial port)

MSM66577L ( $V_{DD} = 2.4$  to  $3.6$  V,  $T_a = -30$  to  $+70^\circ\text{C}$ )

MSM66Q577LY ( $V_{DD} = 3.0$  to  $3.6$  V,  $T_a = -30$  to  $+70^\circ\text{C}$ )

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	$t_{cyc}$	$f_{OSC} = 14$ MHz	71.4	—	ns
Serial clock cycle time	$t_{SCKC}$	$C_L = 50$ pF	$4 t_{cyc}$	—	
Output data setup time	$t_{STMXS}$		$2 t\phi - 30$	—	
Output data hold time	$t_{STMXH}$		$4 t\phi - 20$	—	
Input data setup time	$t_{SRMXS}$		21	—	
Input data hold time	$t_{SRMXH}$		7	—	

Note:  $t\phi = t_{cyc}/2$



Serial ports 4 and 5 (SIO4 and 5)

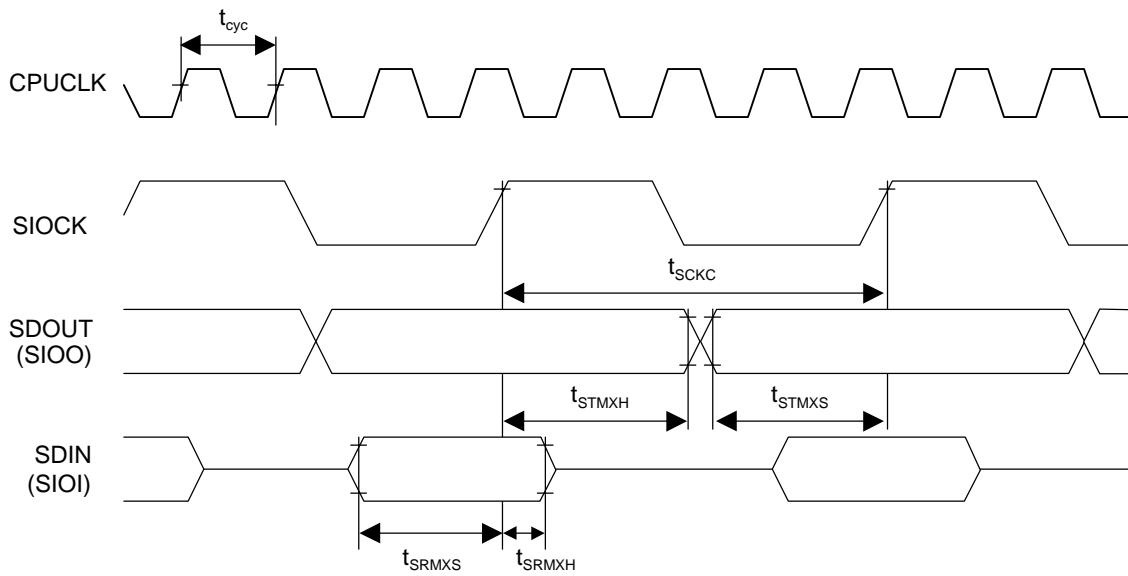
Master mode (Clock synchronous serial port)

MSM66577L ( $V_{DD} = 2.4$  to  $3.6$  V,  $T_a = -30$  to  $+70^\circ\text{C}$ )

MSM66Q577LY ( $V_{DD} = 3.0$  to  $3.6$  V,  $T_a = -30$  to  $+70^\circ\text{C}$ )

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	$t_{cyc}$	$f_{OSC} = 14$ MHz	71.4	—	ns
Serial clock cycle time	$t_{SCKC}$	$C_L = 50$ pF	400	—	
Output data setup time	$t_{STMXS}$		$5.6 t\phi - 10$	—	
Output data hold time	$t_{STMXH}$		$4.2 t\phi - 20$	—	
Input data setup time	$t_{SRMXS}$		21	—	
Input data hold time	$t_{SRMXH}$		0	—	

Note:  $t\phi = t_{cyc}/2$



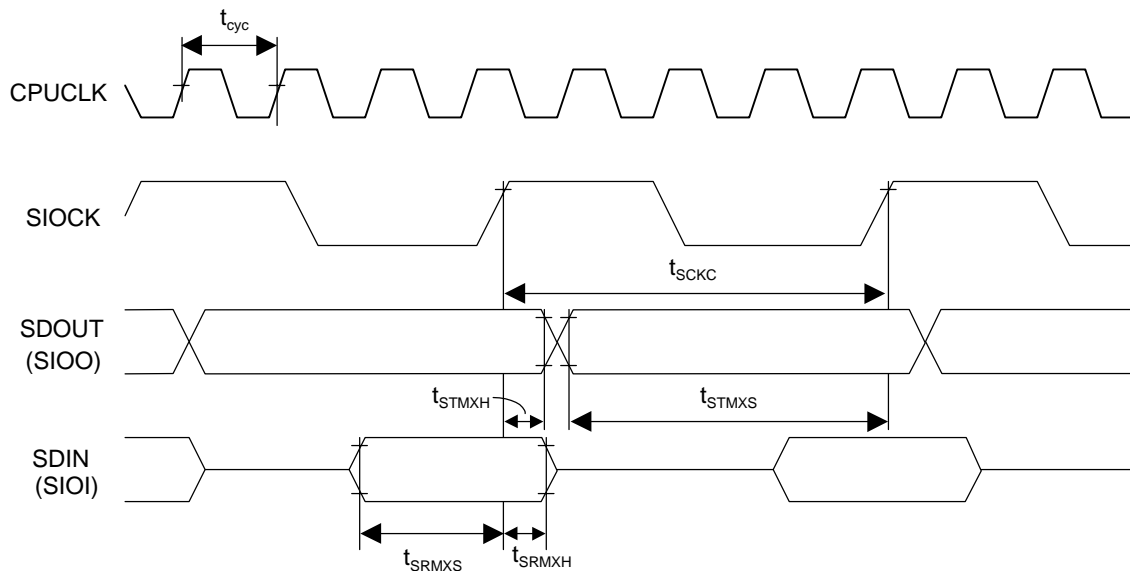
Slave mode (Clock synchronous serial port)

MSM66577L ( $V_{DD} = 2.4$  to  $3.6$  V,  $T_a = -30$  to  $+70^\circ\text{C}$ )

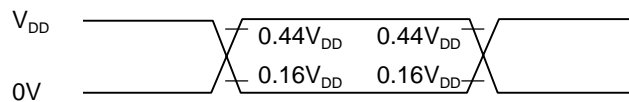
MSM66Q577LY ( $V_{DD} = 3.0$  to  $3.6$  V,  $T_a = -30$  to  $+70^\circ\text{C}$ )

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	$t_{cyc}$	$f_{OSC} = 14$ MHz	71.4	—	ns
Serial clock cycle time	$t_{SCKC}$	$C_L = 50$ pF	400	—	
Output data setup time	$t_{STMXS}$		$2.8 t\phi - 30$	—	
Output data hold time	$t_{STMXH}$		$5.6 t\phi - 20$	—	
Input data setup time	$t_{SRMXS}$		21	—	
Input data hold time	$t_{SRMXH}$		7	—	

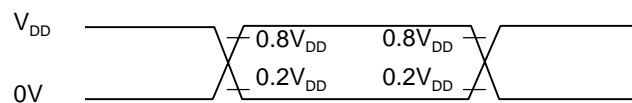
Note:  $t\phi = t_{cyc}/2$



Measurement points for AC timing (except the serial port)



Measurement points for AC timing (the serial port)

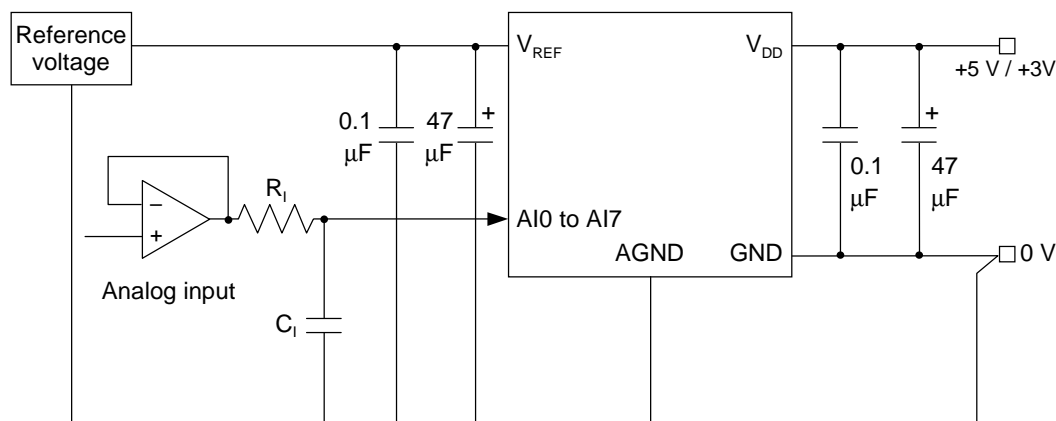


**A/D Converter Characteristics 1 ( $V_{DD} = 4.5$  to  $5.5$  V)**MSM66577/Q577 ( $T_a = -30$  to  $70^\circ\text{C}$ ,  $V_{DD} = V_{REF} = 4.5$  to  $5.5$  V,  $AGND = GND = 0$  V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	Refer to measurement circuit 1 Analog input source impedance $R_i \leq 5$ k $\Omega$ $t_{conv} = 8.5$ $\mu$ s	—	10	—	Bit
Linearity error	$E_L$		—	—	$\pm 3$	LSB
Differential linearity error	$E_D$		—	—	$\pm 2$	
Zero scale error	$E_{ZS}$		—	—	+3	
Full-scale error	$E_{FS}$		—	—	-3	
Cross talk	$E_{CT}$	Refer to measurement circuit 2	—	—	$\pm 1$	
Conversion time	$t_{CONV}$	Set according to ADTM set data	8.5	—	3906.3	$\mu$ s/ch

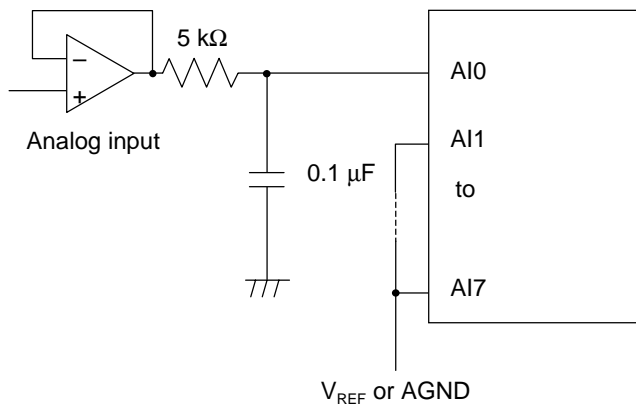
**A/D Converter Characteristics 2 ( $V_{DD} = 2.4$  to  $3.6$  V)**MSM66577L ( $T_a = -30$  to  $70^\circ\text{C}$ ,  $V_{DD} = V_{REF} = 2.4$  to  $3.6$  V,  $AGND = GND = 0$  V)MSM66Q577LY ( $T_a = -30$  to  $70^\circ\text{C}$ ,  $V_{DD} = V_{REF} = 3.0$  to  $3.6$  V,  $AGND = GND = 0$  V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	Refer to measurement circuit 1 Analog input source impedance $R_i \leq 5$ k $\Omega$ $t_{conv} = 27.4$ $\mu$ s	—	10	—	Bit
Linearity error	$E_L$		—	—	$\pm 4$	LSB
Differential linearity error	$E_D$		—	—	$\pm 3$	
Zero scale error	$E_{ZS}$		—	—	+4	
Full-scale error	$E_{FS}$		—	—	-4	
Cross talk	$E_{CT}$	Refer to measurement circuit 2	—	—	$\pm 2$	
Conversion time	$t_{CONV}$	Set according to ADTM set data	27.4	—	3906.3	$\mu$ s/ch



$R_1$  (impedance of analog input source)  $\leq 5$  k $\Omega$   
 $C_1 \approx 0.1 \mu\text{F}$

**Measurement Circuit 1**



Cross talk is the difference between the A/D conversion results when the same analog input is applied to AI0 through AI7 and the A/D conversion results of the circuit to the left.

**Measurement Circuit 2**

#### Definition of Terminology

##### 1. Resolution

Resolution is the value of minimum discernible analog input.

With 10 bits, since  $2^{10} = 1024$ , resolution of  $(V_{REF} - AGND) \div 1024$  is possible.

##### 2. Linearity error

Linearity error is the difference between ideal conversion characteristics and actual conversion characteristics of a 10-bit A/D converter (not including quantization error).

Ideal conversion characteristics can be obtained by dividing the voltage between  $V_{REF}$  and AGND into 1024 equal steps.

##### 3. Differential linearity error

Differential linearity error indicates the smoothness of conversion characteristics. Ideally, the range of analog input voltage that corresponds to 1 converted bit of digital output is  $1\text{LSB} = (V_{REF} - AGND) \div 1024$ . Differential error is the difference between this ideal bit size and bit size of an arbitrary point in the conversion range.

##### 4. Zero scale error

Zero scale error is the difference between ideal conversion characteristics and actual conversion characteristics at the point where the digital output changes from 000H to 001H.

##### 5. Full-scale error

Full-scale error is the difference between ideal conversion characteristics and actual conversion characteristics at the point where the digital output changes from 3FEH to 3FFH.

**D/A Converter Characteristics**MSM66577/Q577 ( $V_{DD} = 4.5$  to  $5.5$  V,  $T_a = -30$  to  $+70^\circ\text{C}$ )MSM66577L ( $V_{DD} = 2.4$  to  $3.6$  V,  $T_a = -30$  to  $+70^\circ\text{C}$ )MSM66Q577LY ( $V_{DD} = 3.0$  to  $3.6$  V,  $T_a = -30$  to  $+70^\circ\text{C}$ )

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	—	—	—	8	Bit
Linearity error	$E_L$		—	—	$\pm 1$	LSB
Absolute precision	—		—	—	$\pm 2$	
Conversion time	$t_{CONV}$	$C_L = 50$ pF	—	20	50	$\mu\text{s}$
Analog output impedance	—	—	—	10	40	k $\Omega$

## Definition of Terminology

## 1. Resolution

Resolution is the value of minimum discernible analog output.

With 8 bits, since  $2^8 = 256$ , resolution of  $(V_{DD} - \text{GND}) \div 256$  is possible.

## 2. Linearity error

Linearity error is the difference between ideal conversion characteristics and actual conversion characteristics of an 8-bit D/A converter.

Ideal conversion characteristics can be obtained by dividing the voltage between  $V_{DD}$  and GND into 256 equal steps.

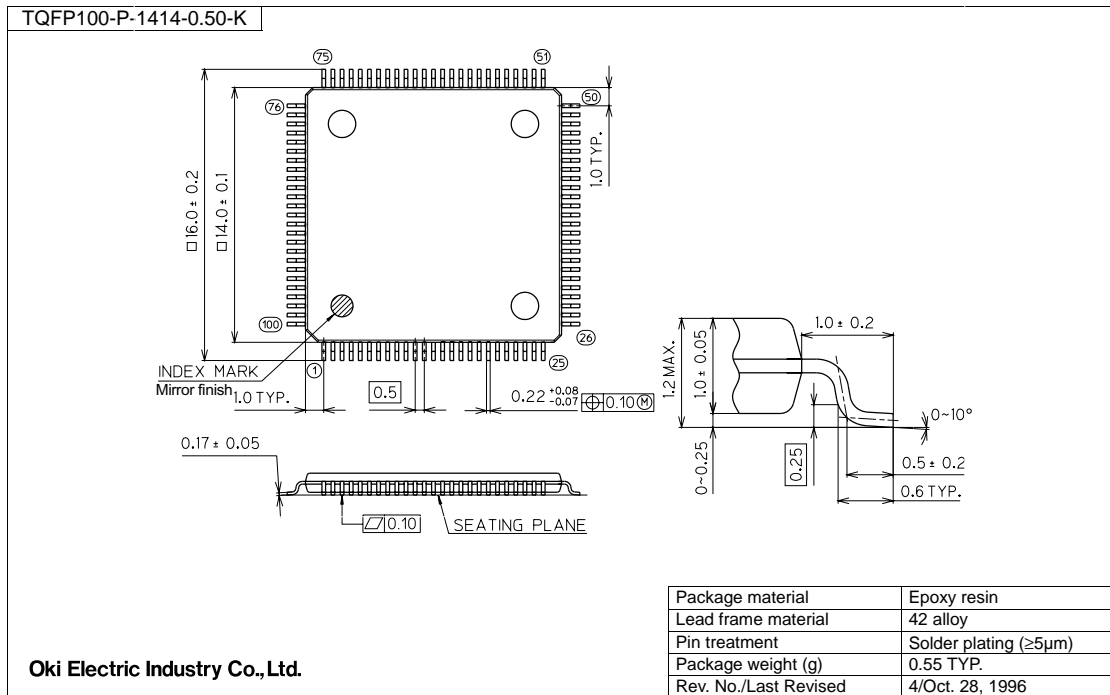
## 3. Absolute precision

Absolute precision is a gross error including a linearity error and the effect of noise.



**PACKAGE DIMENSIONS**

(Unit: mm)



**Notes for Mounting the Surface Mount Type Packages**

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.

Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

**REVISION HISTORY**

Date	Changes compared to previous version
Apr. 2000	-
Oct. 2000	<ul style="list-style-type: none"> <li>- Modified the contents of ORDERING INFORMATION “*2: comment” on P-1.</li> <li>- Modified the contents of PIN DESCRIPTIONS “P3_2/<math>\overline{RD}</math> and P3_3/<math>\overline{WR}</math> Secondary function” on P-7.</li> <li>- Added the contents of PIN DESCRIPTIONS “V<sub>REF</sub>, AGND, and SELMBUS Description” on P-9.</li> <li>- Changed the contents of RECOMMENDED OPERATING CONDITIONS “Memory hold voltage Condition and Rated value” on P-10.</li> <li>- Changed the contents of DC Characteristics 1 “H output voltage Condition and Min. value” on P-12.</li> <li>- Changed the contents of Supply current “CPU operation mode Max. value” on P-12.</li> <li>- Changed the contents of DC Characteristics 2 “H input voltage Condition and Min. value” on P-13.</li> <li>- Modified the contents of DC Characteristics 2 “*3: and *4: comment” on P-13.</li> <li>- Changed the contents of Supply current “CPU operation and HALT mode Max. value” on P13.</li> <li>- Added the contents of AC Characteristics 1 and 2 “*1: comment” on P-14, P-15, P-22, and P-23.</li> <li>- Changed the contents of A/D Converter Characteristics 1 and 2 “Conversion time Min. and Max. value” on P-30.</li> <li>- Changed the contents of “Definition of Terminology” on P-32.</li> </ul>
Feb. 2001	<ul style="list-style-type: none"> <li>- Deleted the character of “Preliminary” on P-1.</li> <li>- Changed the contents of Supply current 1 “CPU operation mode f<sub>XT</sub> =32.768 kHz “ on P-12.</li> <li>- Changed the contents of Supply current 2 “CPU operation mode f<sub>XT</sub> =32.768 kHz “ on P-13.</li> <li>- Modified the mark of “f” to “f<sub>XT</sub>” and “f<sub>OSC</sub>” on P-12 and P13.</li> <li>- Modified the “Serial clock cycle time Min. value” on P-20 and P-21.</li> <li>- Modified the “Serial clock cycle time Min. value” on P-28 and P-29.</li> </ul>

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2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.
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