

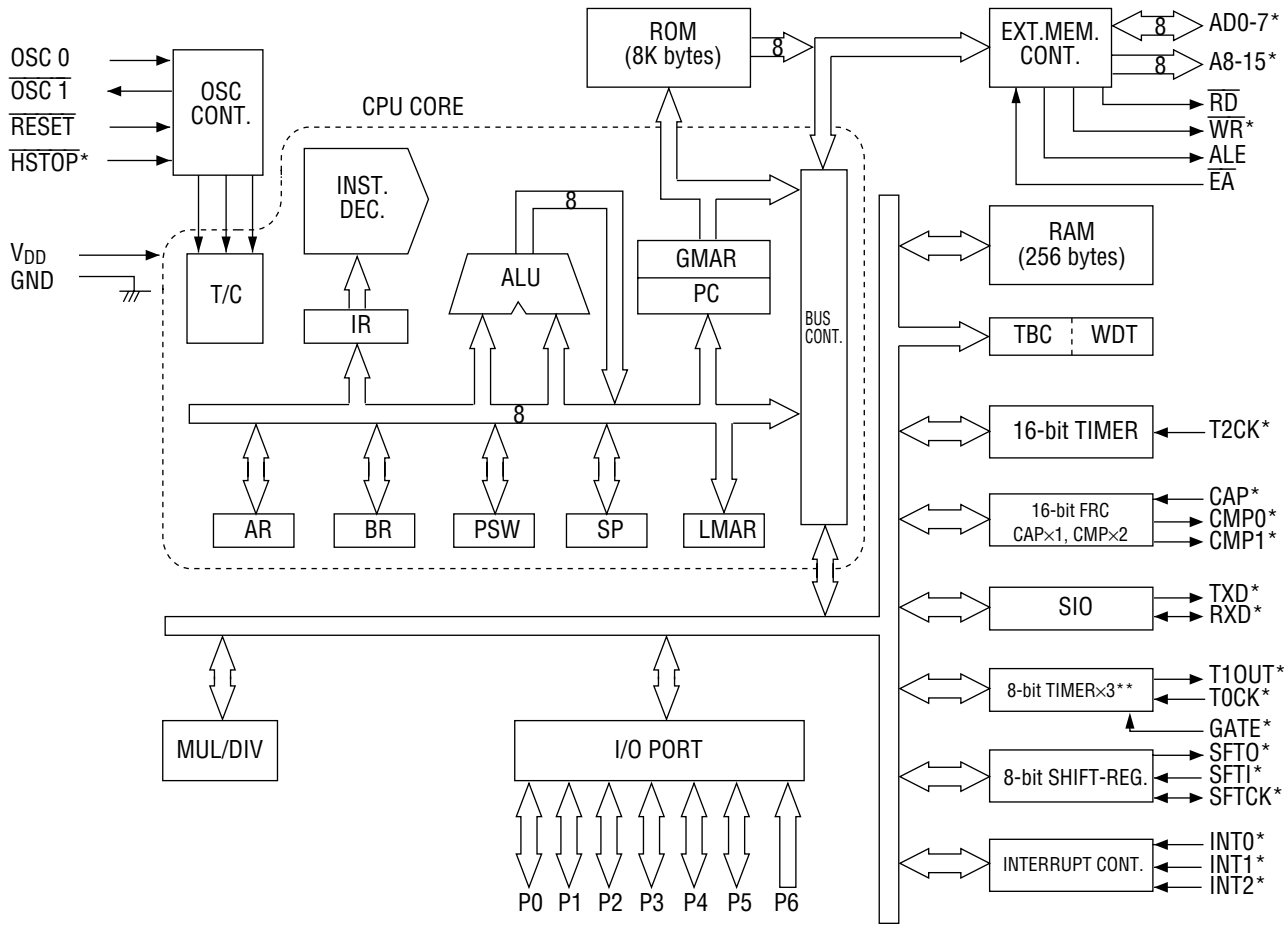
**MSM65513/65P513****High Performance 8-Bit Microcontroller****GENERAL DESCRIPTION**

The MSM65513 is a high-performance 8-bit microcontroller that employs OKI original nX-8/50 CPU core. With a minimum instruction execution time of 400 ns (10MHz clock), the MSM65513 is capable of high-speed processing, and includes 8K bytes of program memory, 256 bytes of data memory, timers and serial ports. Also available are the MSM65P513, which replaces the MSM65513's built-in program memory with one-time PROM, and the MSM65X513, which uses external program memory.

**FEATURES**

- Operating range
    - Operating frequency : 0 to 10MHz ( $V_{DD}=4.5$  to 5.5V)  
0 to 5MHz ( $V_{DD}=2.7$  to 5.5V)
    - Operating voltage : 2.7 to 5.5V
    - Operating temperature :  $-40$  to  $+85^{\circ}\text{C}$
  - Memory space : 64K bytes
    - Internal program memory : 8K bytes
    - Internal data memory : 256 bytes
  - Minimum instruction execution time : 400ns @ 10 MHz
  - Powerful instruction set : 83 basic instructions  
8/16-bit operation instructions  
Bit manipulation instructions  
Compound function instructions
  - Abundant addressing modes
  - Multiplication/division operation functions :  $8 \times 8 \rightarrow 16$   
 $16/8 \rightarrow 16 \dots 8$
  - I/O port
    - Input-output port : 6 ports  $\times$  8 bits
    - input port : 1 port  $\times$  8 bits
  - Timers : 8-bit auto-reload timer  $\times$  2  
16-bit auto-reload timer  $\times$  1  
Watchdog timer  $\times$  1
  - Counters : Time base counter  $\times$  1  
16-bit free-running counter  $\times$  1
  - Capture input : 1 channel
  - Compare output : 2 channels
  - Serial ports : Shift register  $\times$  1  
Serial port with baud rate generator  
(UART/synchronous)  $\times$  1
  - External interrupts : 3
  - Interrupt sources : 15
  - Package
    - 64-pin plastic shrink DIP (SDIP64-P-750-1.78) : (MSM65513-xxxSS, MSM65P513-xxxSS)
    - 64-pin plastic QFP (QFP64-P-1414-0.80-BK) : (MSM65513-xxxGS-BK,  
MSM65P513-xxxGS-BK)
    - 68-pin plastic QFJ (PLCC) (QFJ68-P-S950-1.27) : (MSM65513-xxxJS, MSM65P513-xxxJS)
- xxx indicates the code number.

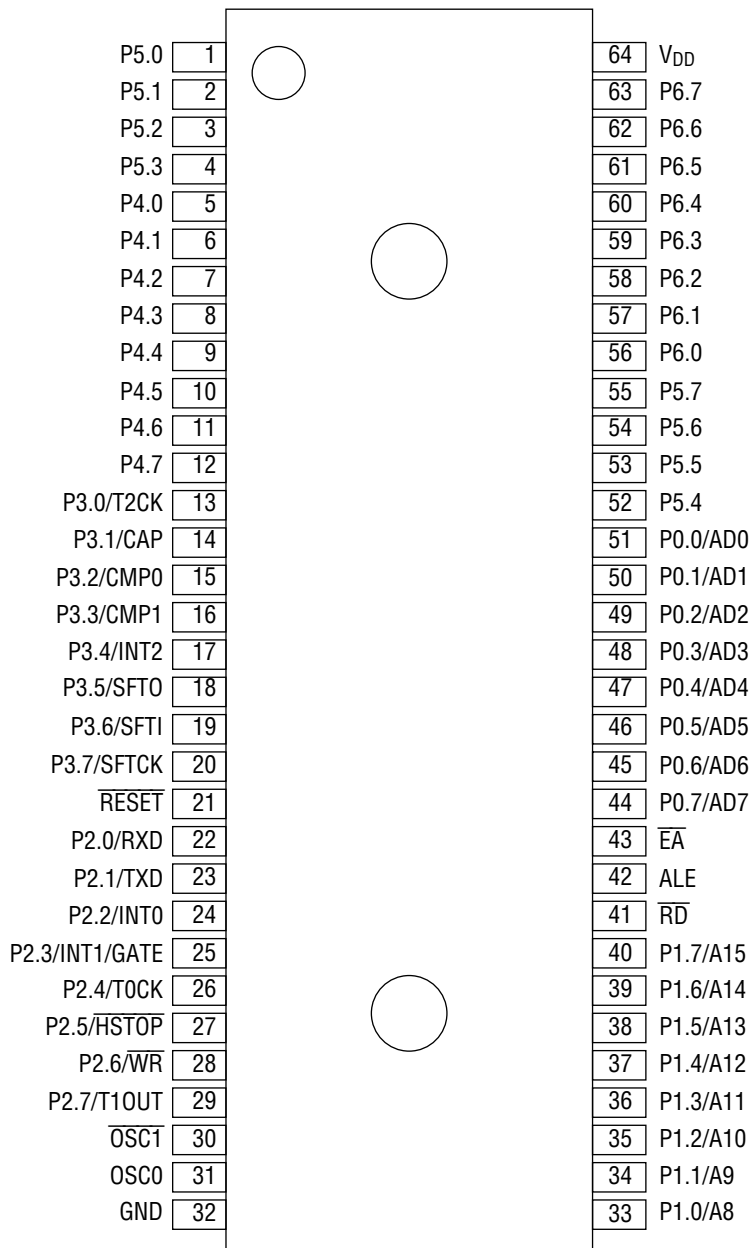
**BLOCK DIAGRAM**



\* Secondary functions of ports

\*\* One timer is used for the SIO baud rate generator.

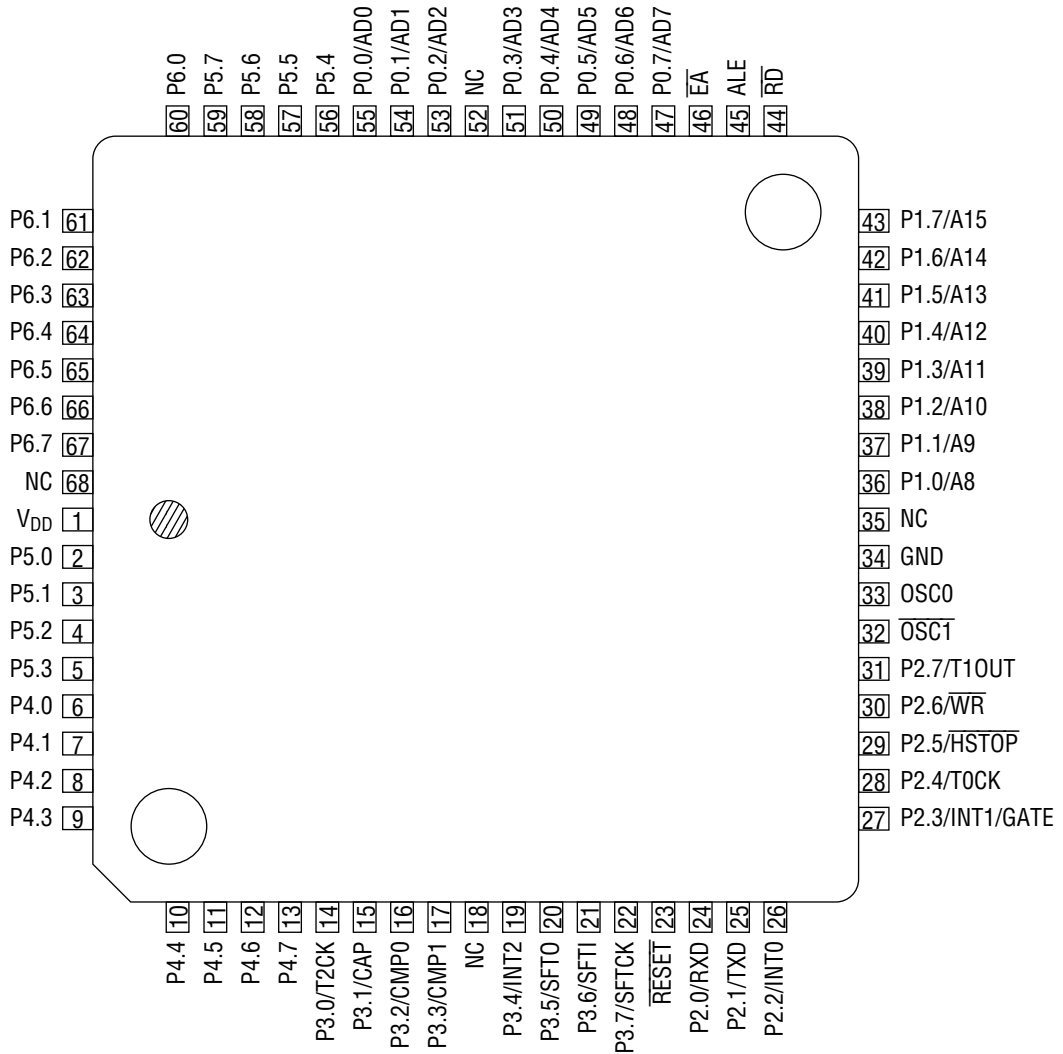
**PIN CONFIGURATION (TOP VIEW)**



**64-Pin Plastic Shrink DIP**



**PIN CONFIGURATION (TOP VIEW) (Continued)**



NC: No-connection pin

**68-Pin Plastic QFJ (PLCC)**

## PIN DESCRIPTION

### Basic Functions

Function	Symbol	Type	Description
Power Supply	V <sub>DD</sub>	—	+5V power supply
	GND	—	0V digital ground
Oscillation	OSC0	I	Crystal oscillation input/external clock input.
	OSC1	O	Crystal oscillation output
Control	RESET	I	System reset input (program starts from address 0040H); internal pull-up resistor
	EA	I	Program memory select input pin. "L" level input for external program memory; "H" level input for internal program memory.
	RD	O	Read strobe signal during external memory access
	ALE	O	Address latch signal during external memory access
Port	PORT 0	I/O	8-bit Input-output port During external memory access, becomes address/data bus for address output, instruction fetch or data read/write along with ALE, RD and WR pins
	PORT 1	I/O	8-bit Input-output port Address bus during external memory access
	PORT 2 PORT 3 PORT 4 PORT 5	I/O	8-bit Input-output port × 4. Secondary functions shown in following table are added for ports 2 and 3.
	PORT 6	I	8-bit Input port.

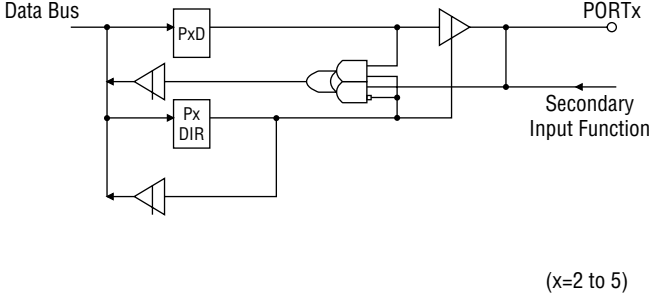

## Secondary Functions

Symbol	Type	Description
RXD	I/O	P2.0 secondary functions UART: Input pin for serial port receive data. Synchronous: Input/output pin for serial port transmit/receive data.
TXD	O	P2.1 secondary functions UART: Output pin for serial port transmit data. Synchronous: Output pin for serial port synchronizing clock.
INT0	I	P2.2 secondary function External interrupt 0 input pin.
INT1/GATE	I	P2.3 secondary functions External interrupt 1 input pin. Also used as input pin for gate signal for timer 0 count enable/disable.
T0CK	I	P2.4 secondary function Timer 0 external clock input pin.
HSTOP	I	P2.5 secondary function Hard stop mode input pin; stops system clock oscillation with "L" level input.
WR	O	P2.6 secondary function Write strobe signal output pin during external data memory access.
T1OUT	O	P2.7 secondary function Output pin for signal obtained by dividing timer 1 overflow by 2.
T2CK	I	P3.0 secondary function Timer 2 external clock input pin.
CAP	I	P3.1 secondary function Capture trigger input pin.
CMP0	O	P3.2 secondary function Compare output channel 0 output pin.
CMP1	O	P3.3 secondary function Compare output channel 1 output pin.
INT2	I	P3.4 secondary function External interrupt 2 input pin.
SFTO	O	P3.5 secondary function Shift register data output pin.
SFTI	I	P3.6 secondary function Shift register data input pin.
SFTCK	I/O	P3.7 secondary function Shift register synchronizing clock input/output pin.

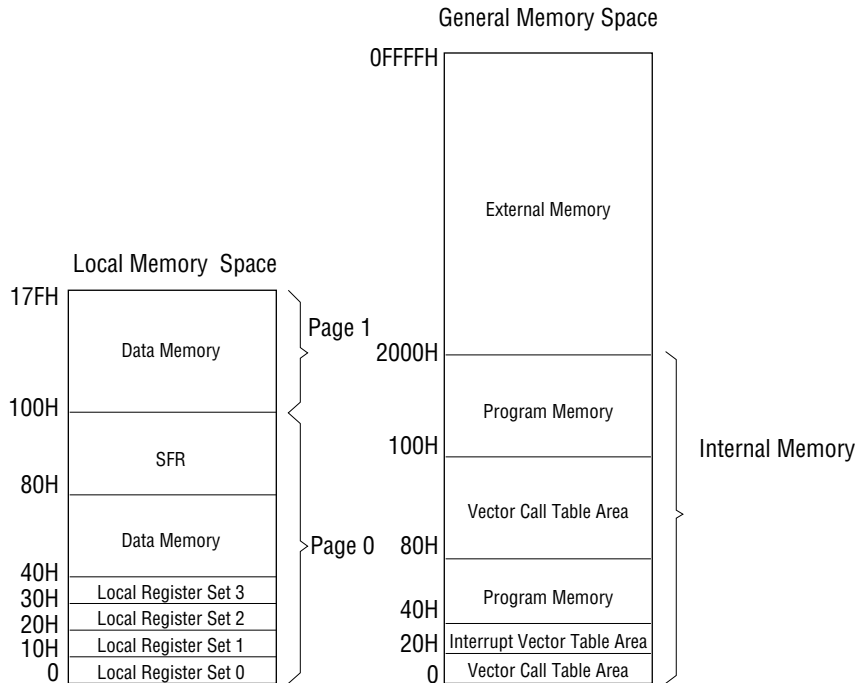




Port Circuit Configuration (Continued)

Type	Port	Circuit Configuration	Electrical Characteristics (V <sub>DD</sub> =5V)
4	P2.2/INT0, P2.3/INT1/GATE, P2.4/T0CK, P2.5/HSTOP, P3.0/T2CK, P3.1/CAP, P3.4/INT2, P3.6/SFTI, P4.0-P4.7, P5.0-P5.7	 <p style="text-align: right;">(x=2 to 5)</p>	<p>"H" Input Voltage:</p> <ul style="list-style-type: none"> <li>• V<sub>IH</sub>=2.4V</li> </ul> <p>"L" Input Voltage:</p> <ul style="list-style-type: none"> <li>• V<sub>IL</sub>=0.8V</li> </ul> <p>"H" Output Voltage:</p> <ul style="list-style-type: none"> <li>• V<sub>OH</sub>=3.75V</li> <li>• I<sub>OH</sub>=-200μA</li> </ul> <p>"L" Output Voltage:</p> <ul style="list-style-type: none"> <li>• V<sub>OL</sub>=0.4V</li> <li>• I<sub>OL</sub>=1.6mA</li> </ul>
5	P6.0-P6.7		<p>"H" Input Voltage:</p> <ul style="list-style-type: none"> <li>• V<sub>IH</sub>=2.4V</li> </ul> <p>"L" Input Voltage:</p> <ul style="list-style-type: none"> <li>• V<sub>IL</sub>=0.8V</li> </ul>

**MEMORY MAPS**



**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	V <sub>DD</sub>	Ta=25°C	-0.3 to 7.0	V
Input Voltage	V <sub>I</sub>		-0.3 to V <sub>DD</sub> +0.3	
Output Voltage	V <sub>O</sub>		-0.3 to V <sub>DD</sub> +0.3	
Power Dissipation	P <sub>D</sub>	Ta=25°C per package	400	mW
		Ta=25°C per output	50	
Storage Temperature	T <sub>STG</sub>	—	-55 to +150	°C

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Condition	Range	Unit
Supply Voltage	V <sub>DD</sub>	Refer to Figure 1	2.7 to 5.5	V
Memory Hold Voltage	V <sub>DDMH</sub>	f <sub>OSC</sub> =0 Hz	2.0 to 5.5	
Oscillation Operating Frequency *1	f <sub>OSC</sub>	Refer to Figure 1	1 to 10	MHz
External Clock Operating Frequency	f <sub>EXTCLK</sub>	Refer to Figure 1	0 to 10	MHz
Operating Temperature	T <sub>OP</sub>	—	-40 to +85	°C

\*1 This is due to the standard of a crystal oscillator or resonator.

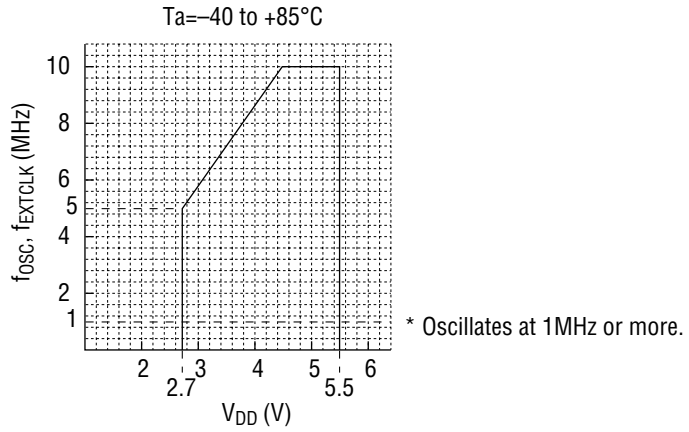


Figure 1. Operating Frequency vs Power Supply Voltage

**ELECTRICAL CHARACTERISTICS**

**DC Characteristics 1 (V<sub>DD</sub>=4.5 to 5.5V)**

(GND=0V, T<sub>a</sub>=-40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage 1 *1	V <sub>IH1</sub>	—	2.4	—	V <sub>DD</sub> +0.3	V
"H" Input Voltage 2 *2	V <sub>IH2</sub>	—	0.7V <sub>DD</sub>	—	V <sub>DD</sub> +0.3	
"L" Input Voltage	V <sub>IL</sub>	—	-0.3	—	0.8	
"H" Output Voltage 1 *3	V <sub>OH1</sub>	I <sub>OH</sub> =-200μA	0.75V <sub>DD</sub>	—	—	
"H" Output Voltage 2 *4	V <sub>OH2</sub>	I <sub>OH</sub> =-400μA	0.75V <sub>DD</sub>	—	—	
"L" Output Voltage 1 *3	V <sub>OL1</sub>	I <sub>OL</sub> =1.6mA	—	—	0.4	
"L" Output Voltage 2 *4	V <sub>OL2</sub>	I <sub>OL</sub> =3.2mA	—	—	0.4	
Input Leak Current 1 *5	I <sub>LI1</sub>	V <sub>I</sub> =V <sub>DD</sub> /0V	—	—	±1	μA
Input Leak Current 2 *6	I <sub>LI2</sub>	V <sub>I</sub> =V <sub>DD</sub> /0V	—	—	±10	
"L" Input Current *7	I <sub>IL</sub>	V <sub>I</sub> =0V	-40	-200	-400	
Input Capacity	C <sub>I</sub>	f=1MHz, T <sub>a</sub> =25°C	—	5	—	pF
Still Current Consumption	I <sub>DDS</sub>	5V, Stop mode *8	—	—	50	μA
Operating Current Consumption	I <sub>DD</sub>	10MHz, 5V, no load Refer to Fig.2	—	20	40	mA

\*1 Excluding OSC0 and  $\overline{\text{RESET}}$

\*2 OSC0 and  $\overline{\text{RESET}}$

\*3 Excluding P0, ALE,  $\overline{\text{RD}}$ , P2.6/ $\overline{\text{WR}}$

\*4 P0, ALE,  $\overline{\text{RD}}$ , P2.6/ $\overline{\text{WR}}$

\*5  $\overline{\text{EA}}$ , P6

\*6 Excluding  $\overline{\text{RESET}}$ ,  $\overline{\text{EA}}$ , P6

\*7  $\overline{\text{RESET}}$

\*8 The ports configured as inputs should be coupled to V<sub>DD</sub> or 0V. Other ports should not be loaded.

**DC Characteristics 2 (2.7≤V<sub>DD</sub><4.5V)**

(GND=0V, Ta=-40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage 1 *1	V <sub>IH1</sub>	—	0.5V <sub>DD</sub> +0.2	—	V <sub>DD</sub> +0.3	V
"H" Input Voltage 2 *2	V <sub>IH2</sub>	—	0.6V <sub>DD</sub> +0.4	—	V <sub>DD</sub> +0.3	
"L" Input Voltage	V <sub>IL</sub>	—	-0.3	—	0.15V <sub>DD</sub> +0.1	
"H" Output Voltage 1 *3	V <sub>OH1</sub>	I <sub>OH</sub> =-10μA	0.75V <sub>DD</sub>	—	—	
"H" Output Voltage 2 *4	V <sub>OH2</sub>	I <sub>OH</sub> =-20μA	0.75V <sub>DD</sub>	—	—	
"L" Output Voltage 1 *3	V <sub>OL1</sub>	I <sub>OL</sub> =10μA	—	—	0.1	
"L" Output Voltage 2 *4	V <sub>OL2</sub>	I <sub>OL</sub> =20μA	—	—	0.1	
Input Lack Current 1 *5	I <sub>LI1</sub>	V <sub>I</sub> =V <sub>DD</sub> /0V	—	—	±1	
Input Lack Current 2 *6	I <sub>LI2</sub>	V <sub>I</sub> =V <sub>DD</sub> /0V	—	—	±10	
"L" Input Current *7	I <sub>IL</sub>	V <sub>DD</sub> =2.7 to 3.3V, V <sub>I</sub> =0V	-40	-120	-240	
Input Capacity	C <sub>I</sub>	f=1MHz, Ta=25°C	—	5	—	pF
Still Current Consumption	I <sub>DDS</sub>	3V, Stop mode *8	—	—	25	μA
Operating Current Consumption	I <sub>DD</sub>	5MHz, 3V, no load Refer to Fig.2	—	6	15	mA

\*1 Excluding OSC0 and  $\overline{\text{RESET}}$

\*2 OSC0 and  $\overline{\text{RESET}}$

\*3 Excluding P0, ALE,  $\overline{\text{RD}}$ , P2.6/ $\overline{\text{WR}}$

\*4 P0, ALE,  $\overline{\text{RD}}$ , P2.6/ $\overline{\text{WR}}$

\*5  $\overline{\text{EA}}$ , P6

\*6 Excluding  $\overline{\text{RESET}}$ ,  $\overline{\text{EA}}$ , P6

\*7  $\overline{\text{RESET}}$

\*8 The ports configured as input should be coupled to V<sub>DD</sub> or 0V. Ports other than those should not be loaded.

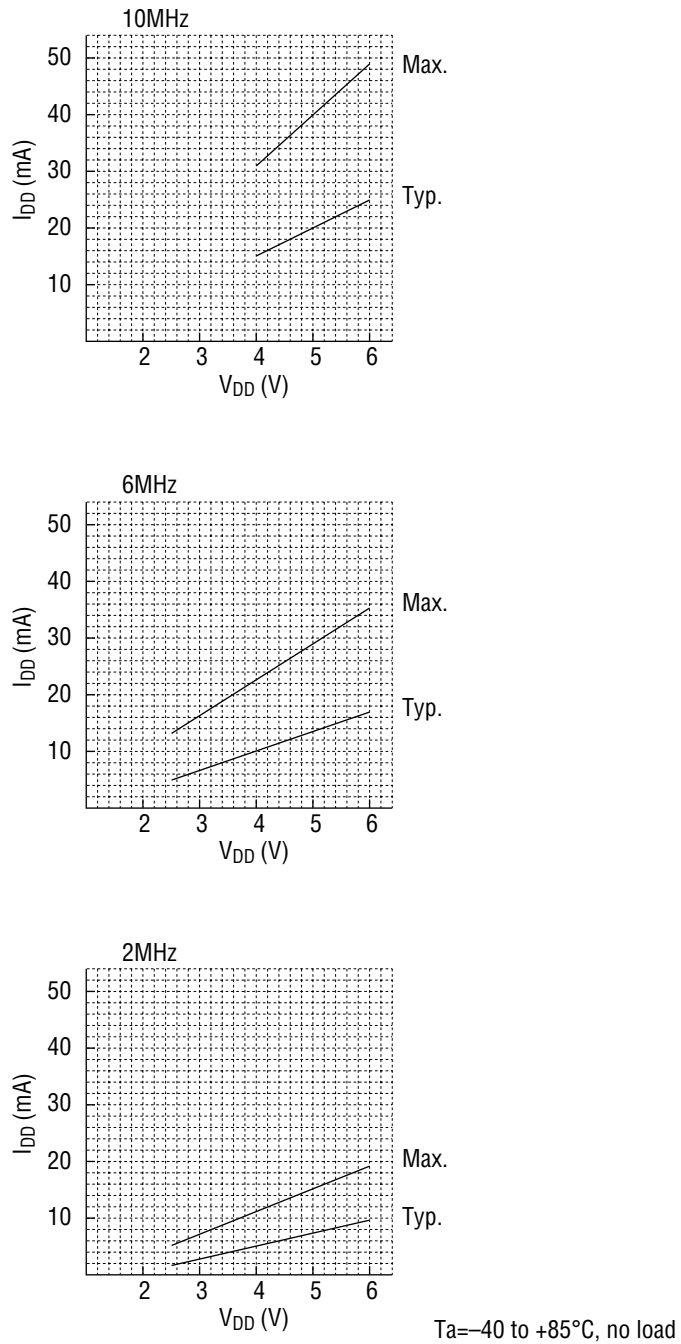


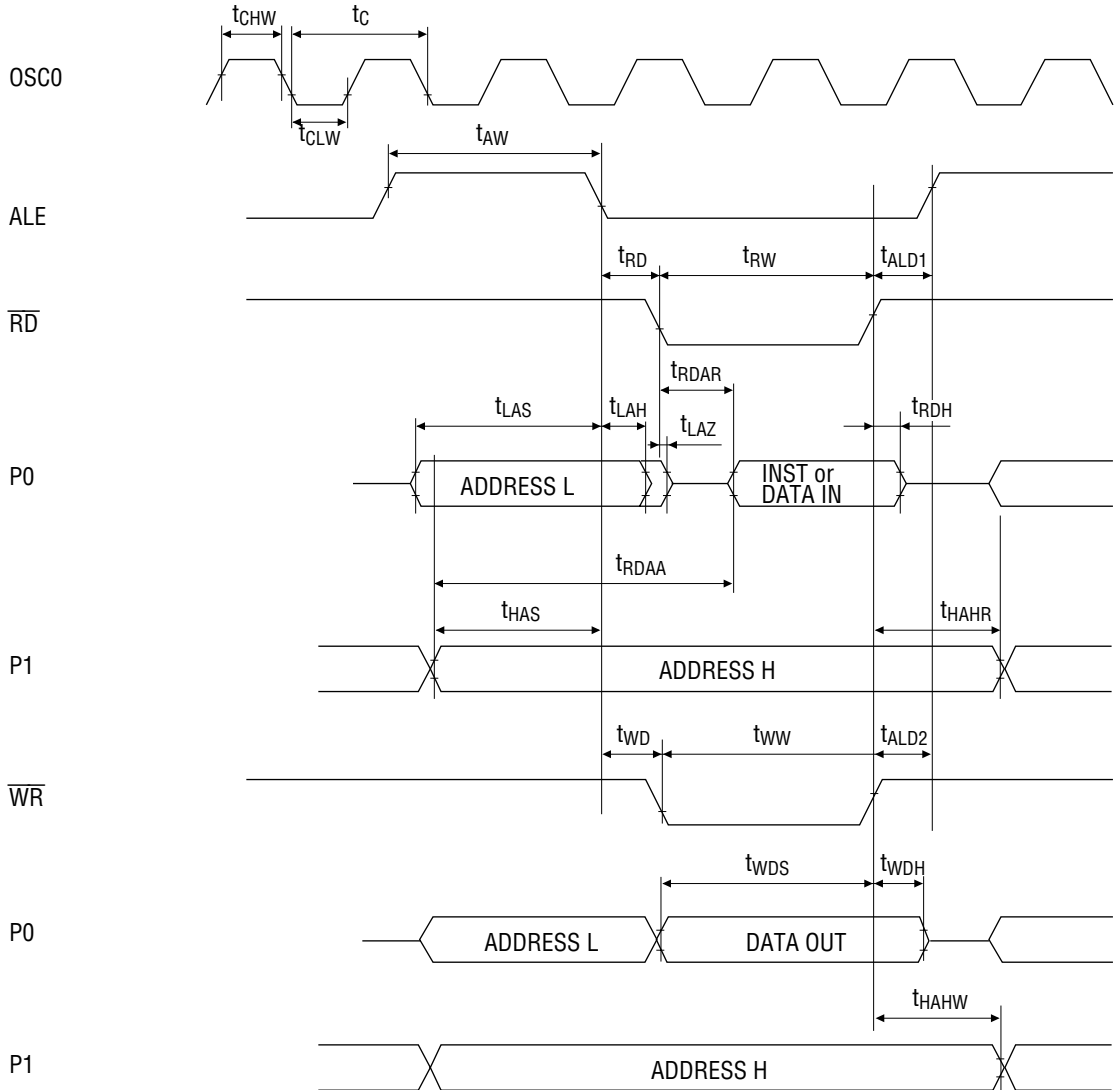
Figure 2. Operating Current Consumption vs. Power Supply Voltage

**AC Characteristics**

• **External memory control**

(V<sub>DD</sub>=2.7 to 5.5V, GND=0V, Ta=-40 to +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Clock Cycle	t <sub>C</sub>	V <sub>DD</sub> =4.5 to 5.5V	100	—	ns
"L" Clock Pulse Width	t <sub>CLW</sub>		45	—	
"H" Clock Pulse Width	t <sub>CHW</sub>		45	—	
Clock Cycle	t <sub>C</sub>	V <sub>DD</sub> =2.7 to 5.5V	200	—	
"L" Clock Pulse Width	t <sub>CLW</sub>		90	—	
"H" Clock Pulse Width	t <sub>CHW</sub>		90	—	
ALE Pulse Width	t <sub>AW</sub>	C <sub>L</sub> =100pF	t <sub>C</sub> +t <sub>CHW</sub> -20	—	
ALE Pulse Delay Time 1	t <sub>ALD1</sub>		t <sub>CLW</sub> -20	—	
ALE Pulse Delay Time 2	t <sub>ALD2</sub>		t <sub>CLW</sub> -20	—	
$\overline{RD}$ Pulse Width	t <sub>RW</sub>		t <sub>C</sub> +t <sub>CHW</sub> -20	—	
$\overline{RD}$ Pulse Delay Time	t <sub>RD</sub>		t <sub>CLW</sub> -40	t <sub>CLW</sub> +20	
$\overline{WR}$ Pulse Width	t <sub>WW</sub>		t <sub>C</sub> +t <sub>CHW</sub> -40	—	
$\overline{WR}$ Pulse Delay Time	t <sub>WD</sub>		t <sub>CLW</sub> -20	t <sub>CLW</sub> +40	
"L" Address Setup Time	t <sub>LAS</sub>		t <sub>C</sub> -40	—	
"H" Address Setup Time	t <sub>HAS</sub>		t <sub>C</sub> -40	—	
"L" Address Hold Time	t <sub>LAH</sub>		t <sub>CLW</sub> -20	—	
Bus Float Time	t <sub>LAZ</sub>		—	20	
"H" Address Hold Time	t <sub>HAHR</sub>		t <sub>C</sub> -20	—	
"H" Address Hold Time	t <sub>HAHW</sub>		t <sub>C</sub> -20	—	
Read Data Access Time	t <sub>RDAA</sub>		—	t <sub>C</sub> +t <sub>CLW</sub> -15	
Read Data Access Time	t <sub>RDAR</sub>		—	t <sub>CHW</sub> +10	
Read Data Hold Time	t <sub>RDH</sub>		0	—	
Write Data Setup Time	t <sub>WDS</sub>		t <sub>C</sub> +t <sub>CLH</sub> -40	—	
Write Data Hold Time	t <sub>WDH</sub>		t <sub>CLW</sub> -20	—	





• CPU control

( $V_{DD}=2.7$  to  $5.5V$ ,  $GND=0V$ ,  $T_a=-40$  to  $+85^{\circ}C$ )

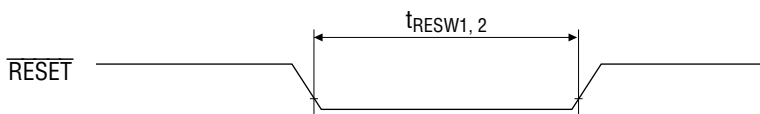
Parameter	Symbol	Condition	Min.	Max.	Unit
$\overline{RESET}$ Pulse Width *1	$t_{RESW1}$	—	20	—	ns
$\overline{RESET}$ Pulse Width *2	$t_{RESW2}$	—	*3	—	—

\*1 Excluding power ON, stop mode and hard stop mode.

\*2 In power ON, stop mode and hard stop mode.

\*3 Oscillation stabilization time depends on resonator.

$\overline{RESET}$  pulse width

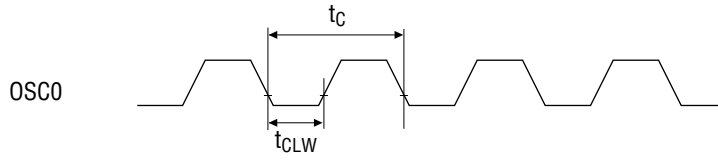


• Peripheral control 1

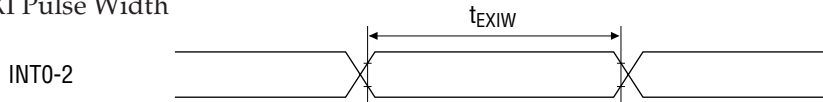
( $V_{DD}=2.7$  to  $5.5V$ ,  $GND=0V$ ,  $T_a=-40$  to  $+85^{\circ}C$ )

Parameter	Symbol	Condition	Min.	Max.	Unit	
OSC	Clock Cycle	$t_C$	$V_{DD}=4.5$ to $5.5V$	100	—	ns
		$t_C$	$V_{DD}=2.7$ to $5.5V$	200	—	
EXI	External Interrupt Pulse Width	$t_{EXIW}$	—	$4 t_C$	—	
T0	External Clock Pulse Width	$t_{T0CW}$	—	$4 t_C$	—	
	GATE Pulse Width	$t_{T0GW}$	—	$1 t_{TOCLK}^*$	—	
T2	External Clock Pulse Width	$t_{T2CW}$	—	$4 t_C$	—	
CAP	CAP Pulse Width	$t_{CAPW}$	—	$12 t_C$	—	

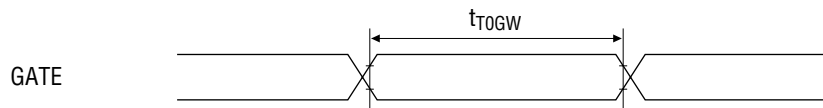
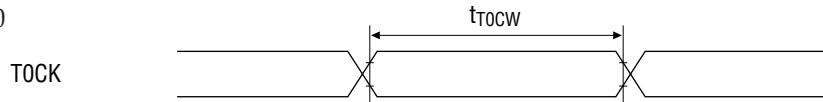
\*  $t_{TOCLK}$  : Timer 0 count clock cycle selected by T0CON.



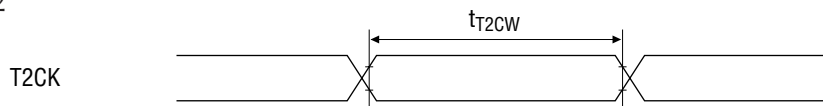
1) EXI Pulse Width



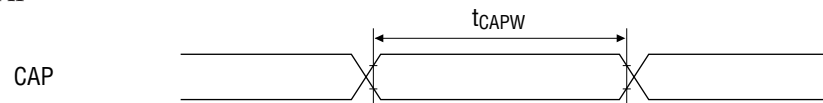
2) T0



3) T2



4) CAP

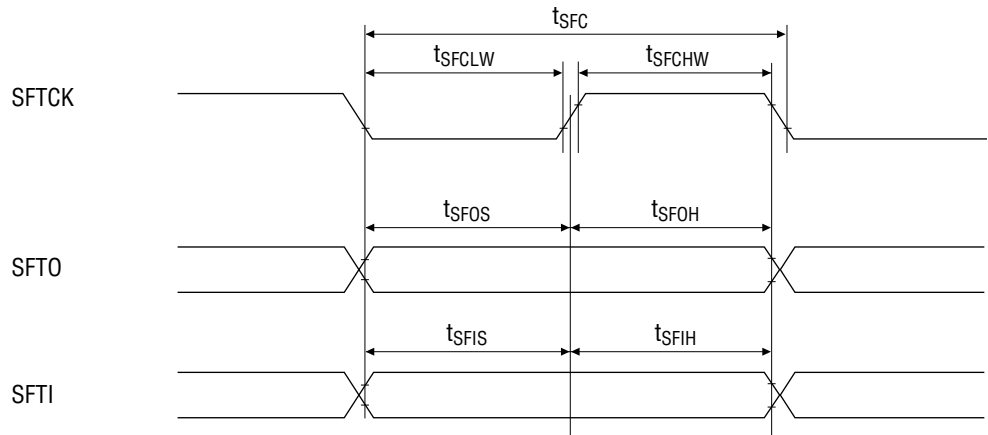


• Peripheral control 2

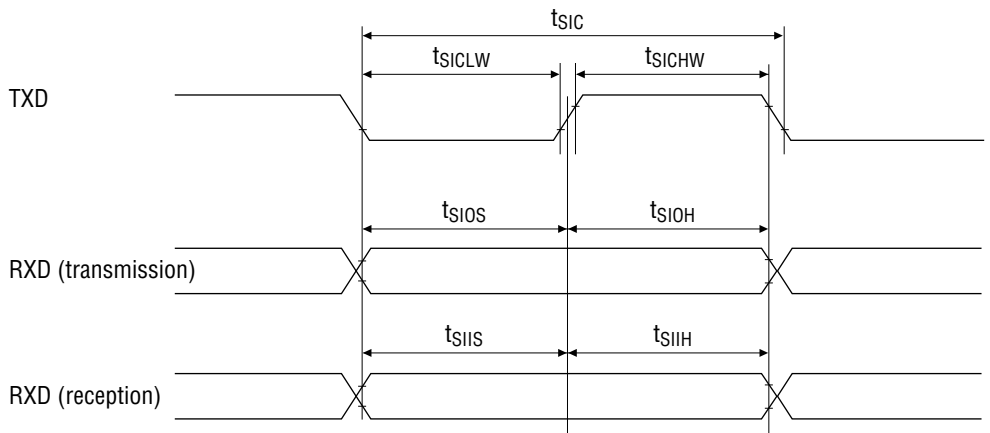
(V<sub>DD</sub>=2.7 to 5.5V, GND=0V, Ta=-40 to +85°C)

Parameter		Symbol	Condition	Min.	Max.	Unit
OSC	Clock Cycle	t <sub>c</sub>	V <sub>DD</sub> =4.5 to 5.5V	100	—	ns
			V <sub>DD</sub> =2.7 to 5.5V	200	—	
SFT	SFTCK Period	t <sub>SFC</sub>	C <sub>L</sub> =100pF	8 t <sub>c</sub>	—	
	SFTCK "L" Pulse Width	t <sub>SFCLW</sub>		4 t <sub>c</sub> -20	—	
	SFTCK "H" Pulse Width	t <sub>SFCHW</sub>		4 t <sub>c</sub> -20	—	
	SFTCK Setup Time	t <sub>SFOS</sub>		t <sub>SFCLW</sub> -100	—	
	SFTO Hold Time	t <sub>SFOH</sub>		t <sub>SFCHW</sub> -100	—	
	SFTI Setup Time	t <sub>SFIS</sub>		100	—	
	SFTI Hold Time	t <sub>SFIH</sub>		100	—	
SIO (Clock Synchronous Mode)	Synchronous Clock Cycle	t <sub>SIC</sub>	C <sub>L</sub> =100pF	8 t <sub>c</sub>	—	
	Synchronous Clock "L" Pulse Width	t <sub>SICLW</sub>		4 t <sub>c</sub> -20	—	
	Synchronous Clock "H" Pulse Width	t <sub>SICHW</sub>		4 t <sub>c</sub> -20	—	
	Output Data Setup Time	t <sub>SIOS</sub>		6 t <sub>c</sub> -100	—	
	Output Data Hold Time	t <sub>SIOH</sub>		2 t <sub>c</sub> -100	—	
	Input Data Setup Time	t <sub>SIS</sub>		t <sub>c</sub> +t <sub>CLW</sub> +100	—	
	Input Data Hold Time	t <sub>SIH</sub>		0	—	

1) SFT

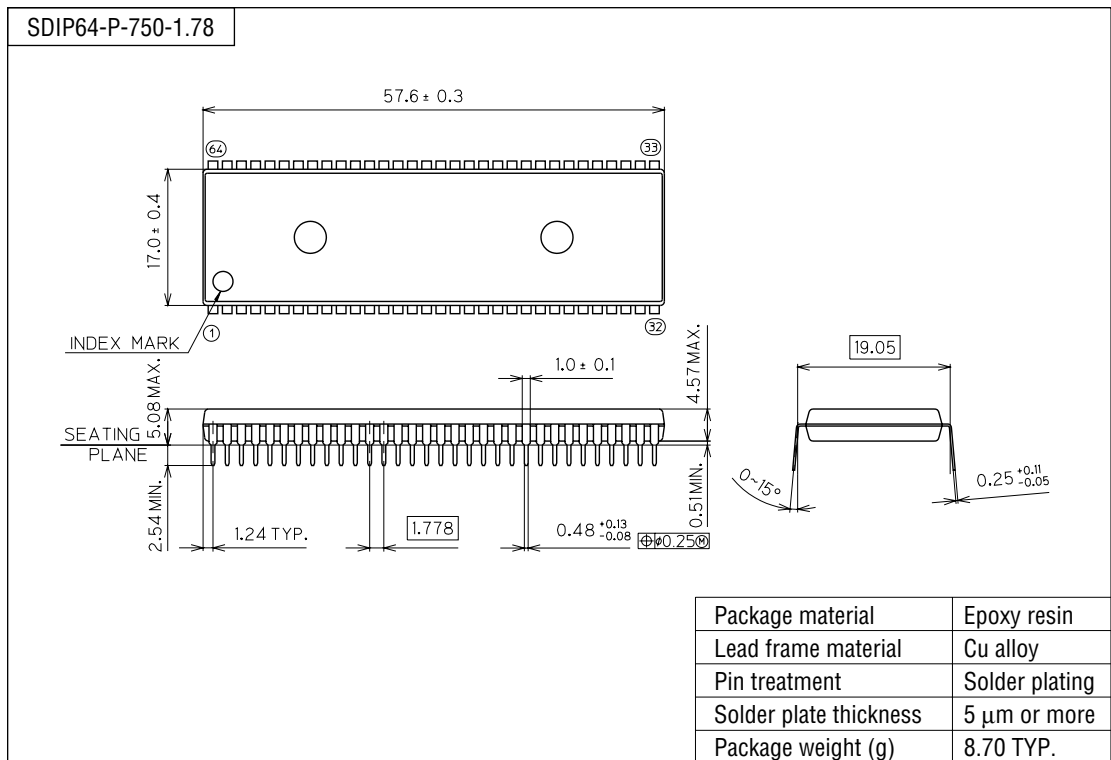


2) SIO  
(Clock synchronous mode)



**PACKAGE DIMENSIONS**

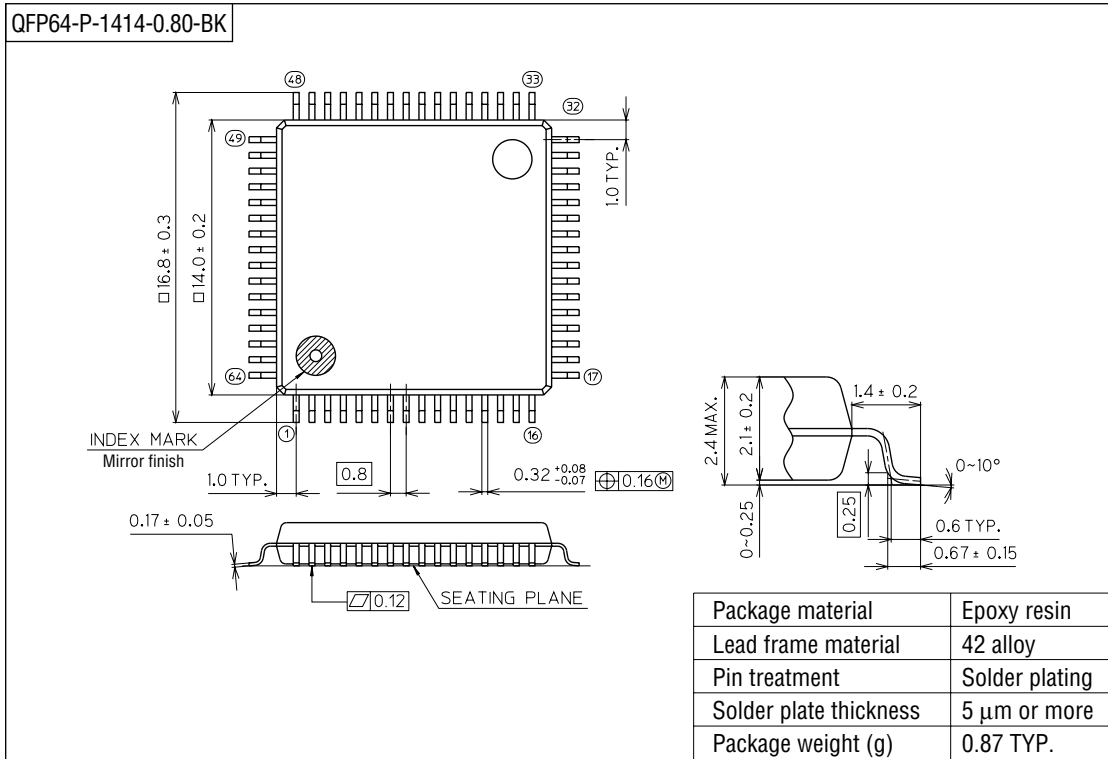
(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

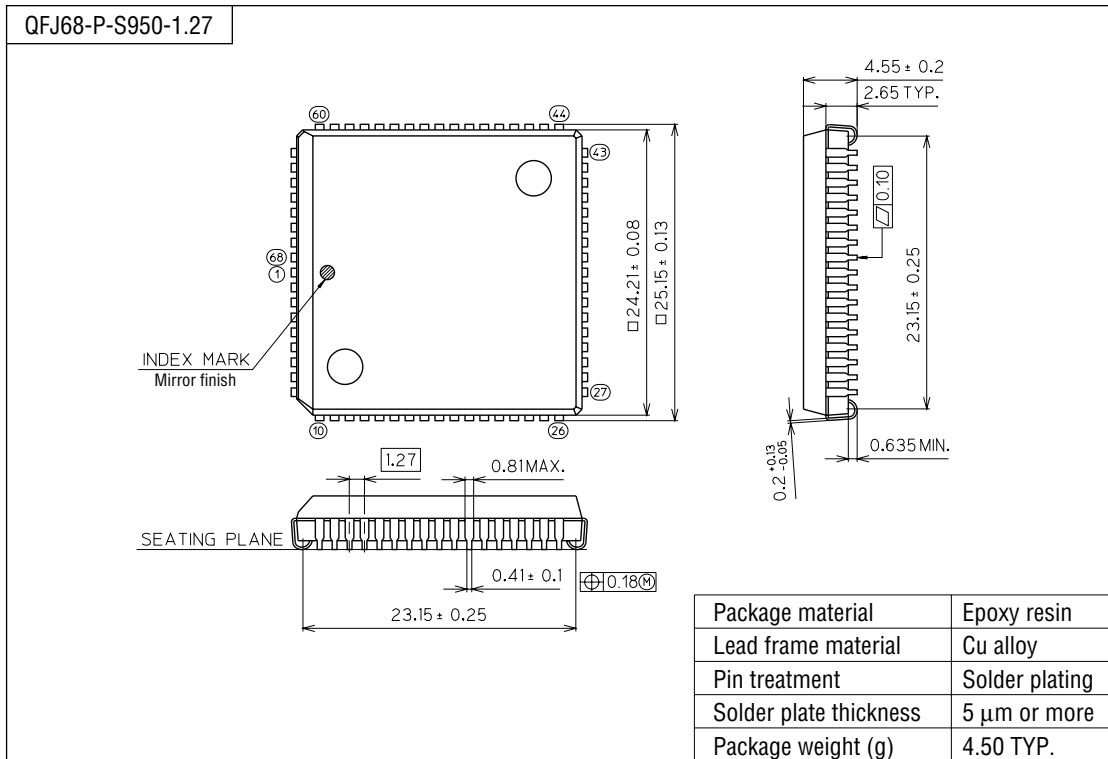
(Unit : mm)



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(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).