OKI Semiconductor

This version: Nov. 1997
Previous version: Mar. 1996

MSM5238

32-DOT LCD COMMON DRIVER

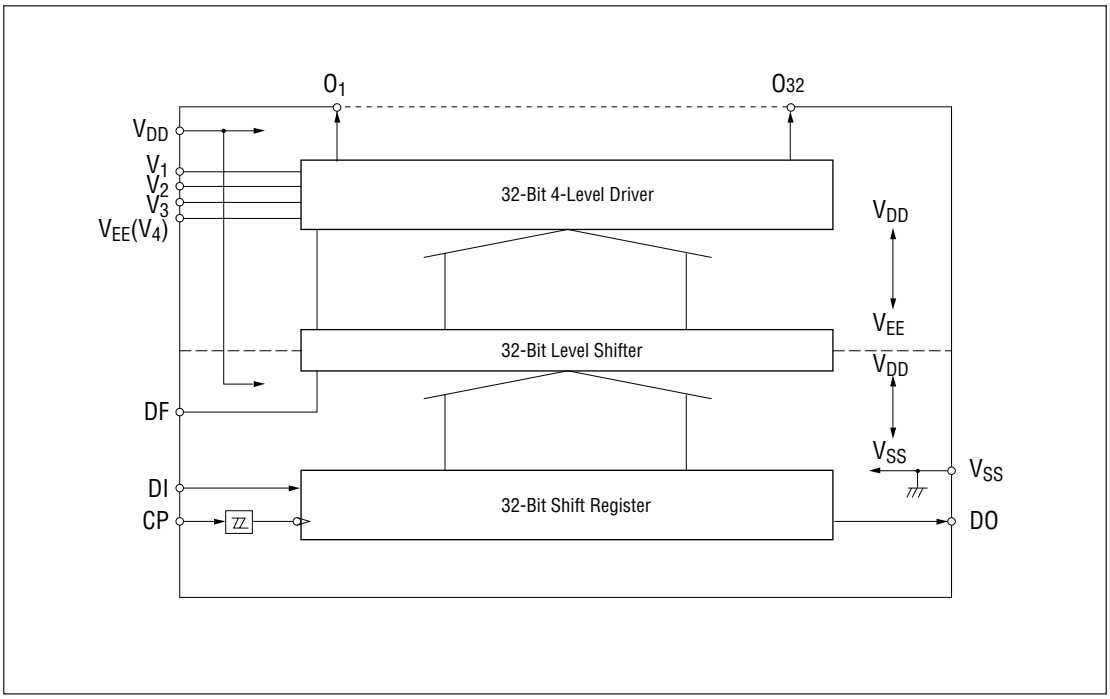
GENERAL DESCRIPTION

The MSM5238 is a dot matrix LCD common driver LSI which is fabricated using low power CMOS metal gate technology. The scanning signal in one matrix display frame can be divided into up to 1/32 duty. This LSI consists of 32-bit shift register, 32-bit level shifter and 32-bit 4-level driver.
This LSI can drive a variety of LCD panels because the bias voltage, which determines the LCD driving voltage, can be optionally supplied from an external source.

FEATURES

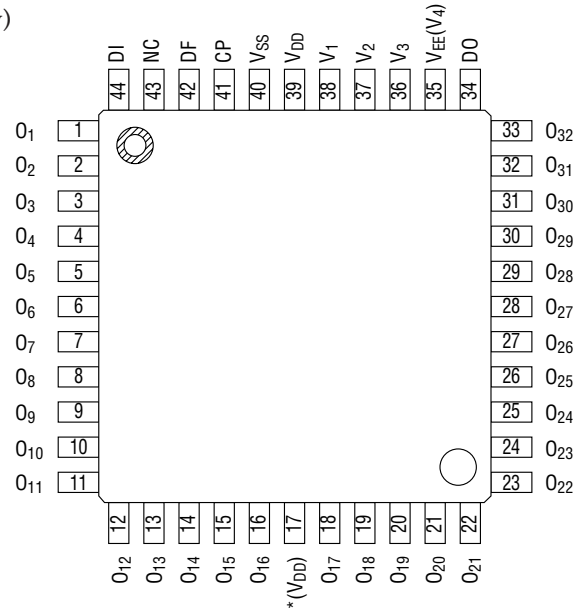
- Supply voltage : 3 to 7V
- LCD driving voltage : 3 to 16V
- Applicable LCD duty : 1/32 to 1/64
  (1/64 duty is available when MSM5238s are cascade-connected)
- Bias voltage can be supplied externally.
- Applicable segment driver: MSM5839B/C (40 outputs)
- Package options:
  44-pin plastic QFP (QFP44-P-910-0.80-K) (Product name: MSM5238GS-K)
  44-pin plastic QFP (QFP44-P-910-0.80-L2) (Product name: MSM5238GS-L2)
  44-pin plastic QFP (QFP44-P-910-0.80-2K) (Product name: MSM5238GS-2K)

BLOCK DIAGRAM



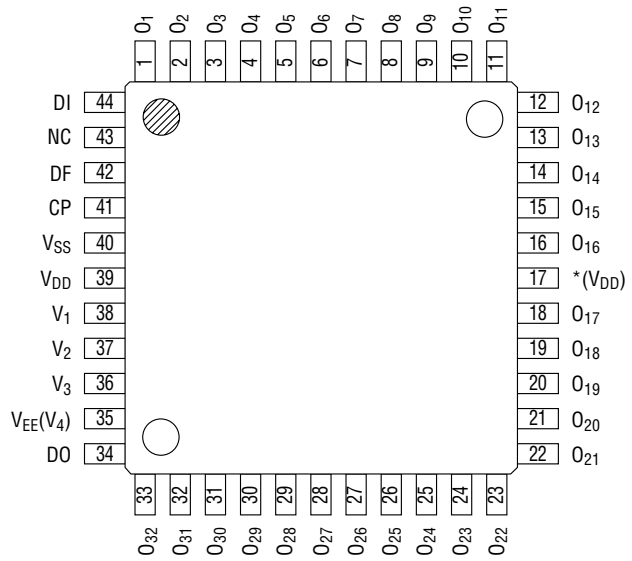
PIN CONFIGURATION (TOP VIEW)

(Top view)



NC: No connection

44-Pin Plastic QFP (Type K)



NC: No connection

44-Pin Plastic QFP (Type L)

* Pin 17 is an auxiliary pin. It must be connected to the power supply or left open.

Note : The figure for Type L shows the configuration viewed from the reverse side of the package. Pay attention to the difference in pin arrangement.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DD}	Ta = 25°C	–0.3 to +7	V
Supply Voltage	V_{LCD}	Ta = 25°C, V_{DD}–V_{EE}	0 to 16.5	V
Input Voltage	V_I	Ta = 25°C	–0.3 to V_{DD}	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Supply Voltage	V_{DD}	—	3 to 7	V
Supply Voltage	V_{LCD}	V_{DD}–V_{EE} *	3 to 16	V
Operating Temperature	T_{op}	—	–40 to +85	°C
Fan-Out	N	MOS load	5	—

* $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_{EE}$ (V_4)

ELECTRICAL CHARACTERISTICS

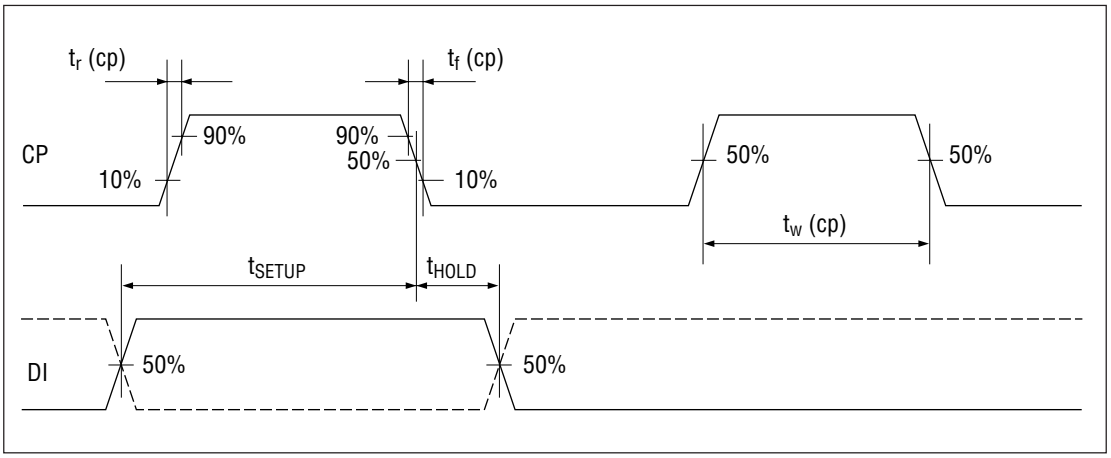
DC Characteristics

Parameter	Symbol	V_{DD} (V)	V_{SS} (V)	V_{EE} (V)	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH1}/V_{IH2} *1	5	0	0 to –9	—	3.6/4.2	—	—	V
		7	0	0 to –7	—	5.2/6.0	—	—	
"L" Input Voltage	V_{IL1}/V_{IL2} *1	5	0	0 to –9	—	—	—	0.8/0.4	V
		7	0	0 to –7	—	—	—	1.1/0.5	
Input Current	I_{IH}	7	0	–7	V_I = 7V	—	—	1	µA
	I_{IL}	7	0	–7	V_I = 0V	—	—	–1	
"H" Output Voltage	V_{OH} *2	5	0	0 to –9	I_O = –40µA	4.2	—	—	V
		7	0	0 to –7	I_O = –56µA	5.8	—	—	
"L" Output Voltage	V_{OL} *2	5	0	0 to –9	I_O = 0.2mA	—	—	0.4	V
		7	0	0 to –7	I_O = 0.3mA	—	—	0.4	
ON Resistance	R_{ON} (V_1, $V_{EE}(V_4)$)	5	0	0	V_O: DRV output $V_O - V_1$ = 0.25V $V_1 = V_{EE}$ to (V_{DD} – 0.25V) $V_O - V_4$ = 0.25V V_4 (V_{EE}): 0V MAX	—	500	2000	Ω
			0	–5		—	250	1000	
		7	0	0		—	350	1400	
			0	–7		—	200	800	
	R_{ON} (V_2, V_3)	5	0	0	$V_N = V_2$ or V_3 V_O = DRV output $V_O - V_N$ = 0.25V $V_N = V_{EE}$ to (V_{DD} – 0.25V)	—	800	3200	Ω
			0	–5		—	450	1800	
		7	0	0		—	550	2200	
			0	–7		—	350	1400	
OFF Leakage Current	I_{OFF}	5	0	–9	—	—	—	±5	µA
		7	0	–7	—	—	—	±5	
Supply Current	I_{DD}	5	0	–9	—	—	—	0.5	mA
		7	0	–7	—	—	—	1.0	
Input Capacitance	C_I	—	—	—	—	–	5	—	pF

*1 V_{IH1} and V_{IL1} are input pins for DI and DF, while V_{IH2} and V_{IL2} are input pins for CP.
*2 V_{OH} and V_{OL} are output pins for DO.

Switching Characteristics

Parameter	Symbol	V_{DD} (V)	Condition	Min.	Typ.	Max.	Unit
Clock Frequency	$f_{(cp)}$	5	—	—	—	400	kHz
		7	—	—	—	550	
Clock Pulse Width	$t_{w(cp)}$	5	—	400	—	—	ns
		7	—	300	—	—	
Data Setup Time (DATAIN → CP)	t_{SETUP}	5	—	100	—	—	ns
		7	—	50	—	—	
Data Hold Time (DATAIN → CP)	t_{HOLD}	5	—	800	—	—	ns
		7	—	500	—	—	
Clock Pulse Rise/Fall Time	$t_{r(cp)}$	5	—	—	—	0.5	ms
	$t_{f(cp)}$	7	—	—	—	0.1	



FUNCTIONAL DESCRIPTION

Pin Functional Description

- **DI**
  Shift register data input pin which inputs the data on scanning lines in synchronization with a clock (positive logic). This LSI can optionally divide the scanning signal up to 1/32 duty LCD panel because it consists of the 32-bit shift register.

- **CP**
  Clock pulse input pin for the 32-bit shift register. The data is shifted to the 32-bit shift register at the falling edge of the clock pulse. A data set up time (t_{SETUP}) and data hold time (t_{HOLD}) are required between DI and CP. (Refer to Switching Characteristics.) A Schmitt circuit is included in the CP input circuit.

- **DF**
  Synchronous signal input pin for alternate signal for LCD driving.

- **V_{DD}, V_{SS}**
  V_{DD} is a power supply pin, which is normally from 3.0V to 7.0V. V_{SS} is a ground pin, which is 0V.

- **O_1 - O_{32}**
  Display data output pins which correspond to each data bit in the latch. One of V_1, V_2, V_3 and V_{EE} (V_4) is selected as a display driving voltage source based on the combination of latched data level and DF signal. Refer to the Truth Table. O_1 - O_{32} are connected to the common side of the LCD panel.

- **V_1, V_2, V_3, V_{EE} (V_4)**
  Bias supply voltage pins to drive the LCD. Use an external bias voltage supply for driving the LCD.

- **DO**
  Shift register output pin. The data which was input from DI is output from DO with 32 bits delay, synchronized with the clock pulse. The MSM5238 is used at 1/32 duty and also at 1/64 duty through cascade connection. Refer to Figure 1 below.

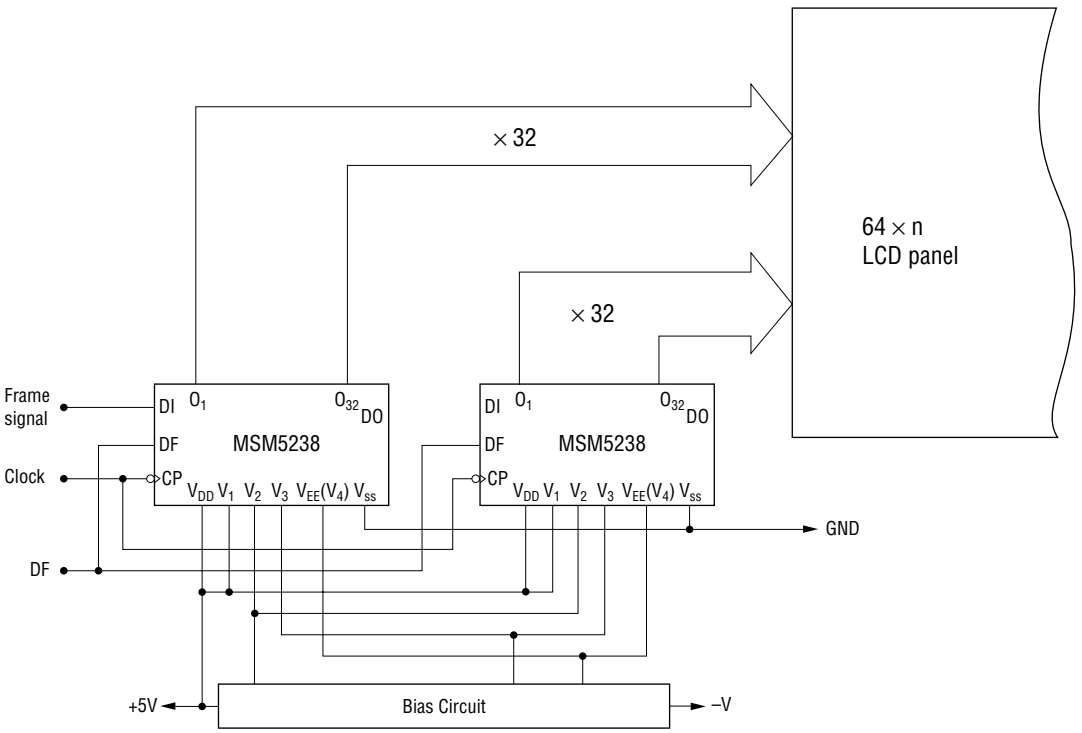


Figure 1

Truth Table

Latched data	DF	LCD driver output
L	L	V_2
	H	V_4
H	L	V_3
	H	V_1

NOTES ON USE

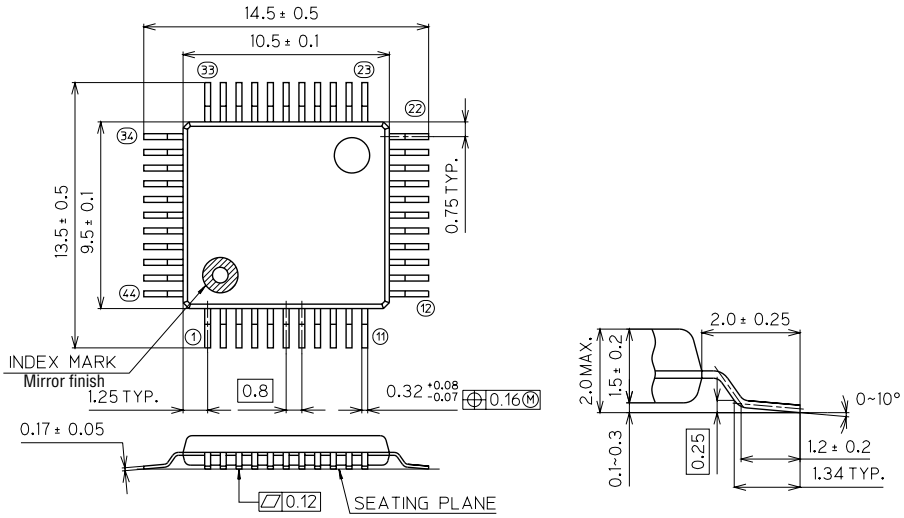
Note the following when turning power on and off:
The LCD drivers of this IC require a high voltage. For this reason, if a high voltage is applied to the LCD drivers with the logic power supply floating, excess current flows. This may damage the IC. Be sure to carry out the following power-on and power-off sequences:

When turning power on:
First V_{DD} ON, next V_{EE} (V_4), V_3, V_2, V_1 ON. Or both ON at the same time.
When turning power off:
First V_{EE} (V_4), V_3, V_2, V_1 OFF, next V_{DD} OFF. Or both OFF at the same time.

PACKAGE DIMENSIONS

(Unit : mm)

QFP44-P-910-0.80-K



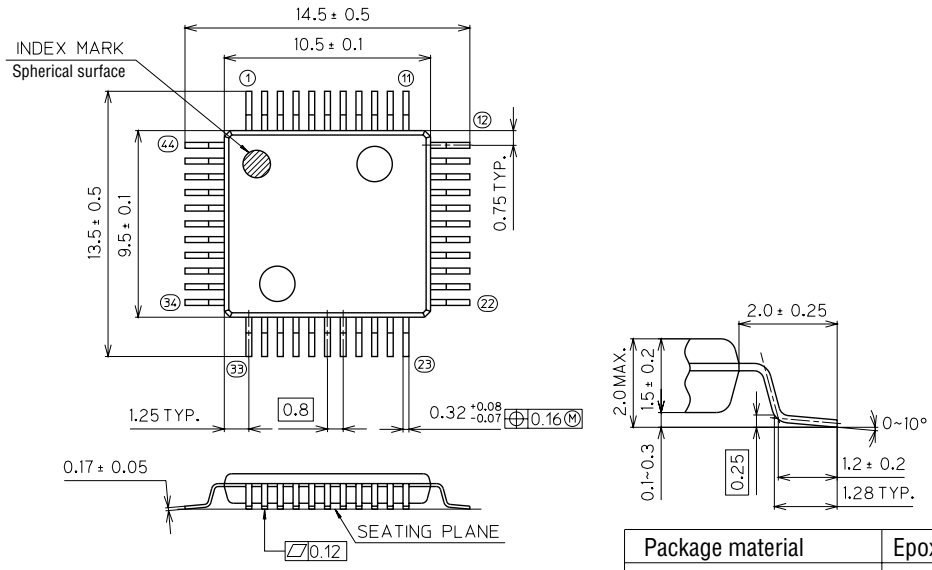
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.35 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

QFP44-P-910-0.80-L2



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.35 TYP.

Notes for Mounting the Surface Mount Type Package

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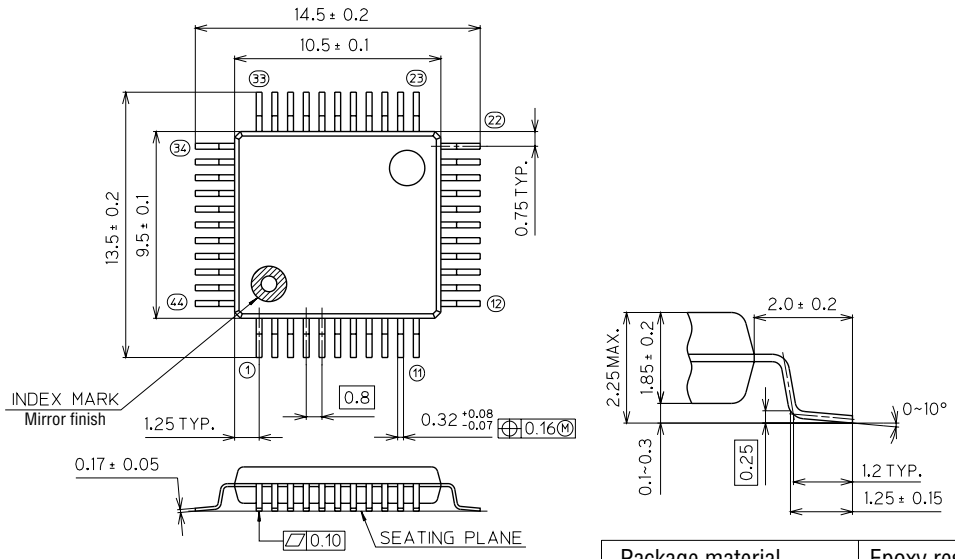
(Unit : mm)

QFP44-P-910-0.80-2K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.41 TYP.

Notes for Mounting the Surface Mount Type Package

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