

**MSM5116160D/DSL****1,048,576-Word × 16-Bit DYNAMIC RAM : FAST PAGE MODE TYPE****DESCRIPTION**

The MSM5116160D/DSL is a 1,048,576-word × 16-bit dynamic RAM fabricated in Oki's silicon-gate CMOS technology. The MSM5116160D/DSL achieves high integration, high-speed operation, and low-power consumption because Oki manufactures the device in a quadruple-layer polysilicon/double-layer metal CMOS process. The MSM5116160D/DSL is available in a 42-pin plastic SOJ or 50/44-pin plastic TSOP. The MSM5116160DSL (the self-refresh version) is specially designed for lower-power applications.

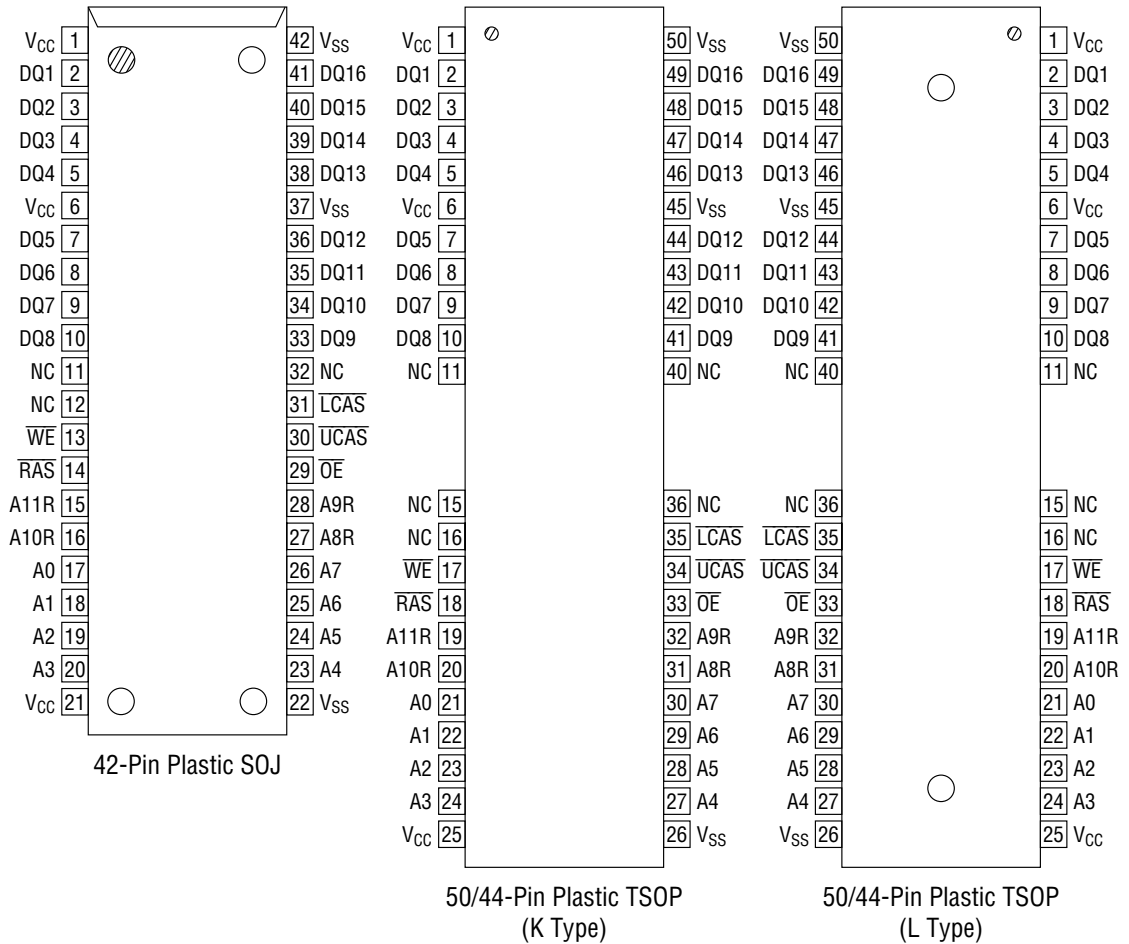
**FEATURES**

- 1,048,576-word × 16-bit configuration
  - Single 5 V power supply, ±10% tolerance
  - Input : TTL compatible, low input capacitance
  - Output : TTL compatible, 3-state
  - Refresh : 4096 cycles/64 ms, 4096 cycles/128 ms (SL version)
  - Fast page mode, read modify write capability
  - $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh, hidden refresh,  $\overline{\text{RAS}}$ -only refresh capability
  - $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  self-refresh capability (SL version)
  - Package options:
    - 42-pin 400 mil plastic SOJ (SOJ42-P-400-1.27) (Product : MSM5116160D/DSL-xxJS)
    - 50/44-pin 400 mil plastic TSOP (TSOPII50/44-P-400-0.80-K) (Product: MSM5116160D/DSL-xxTS-K)
    - (TSOPII50/44-P-400-0.80-L) (Product: MSM5116160D/DSL-xxTS-L)
- xx indicates speed rank.

**PRODUCT FAMILY**

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t <sub>RAC</sub>	t <sub>AA</sub>	t <sub>CAC</sub>	t <sub>OEA</sub>		Operating (Max.)	Standby (Max.)
MSM5116160D/DSL-50	50 ns	25 ns	13 ns	13 ns	90 ns	495 mW	5.5 mW/ 1.1 mW (SL version)
MSM5116160D/DSL-60	60 ns	30 ns	15 ns	15 ns	110 ns	468 mW	
MSM5116160D/DSL-70	70 ns	35 ns	20 ns	20 ns	130 ns	440 mW	

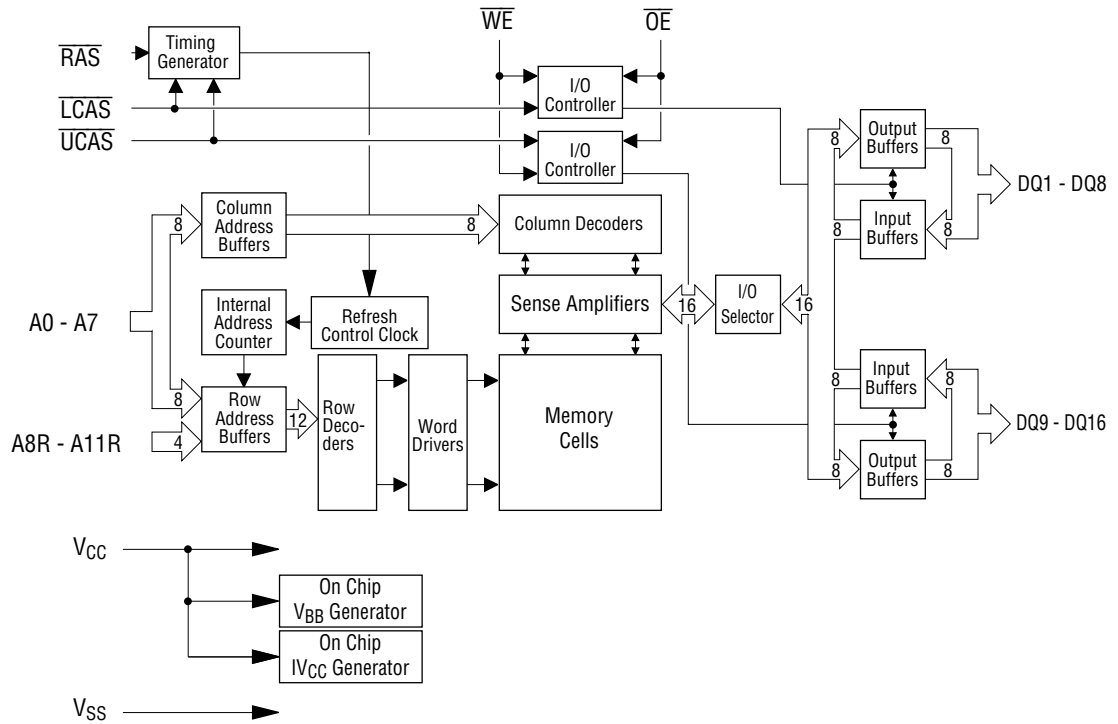
**PIN CONFIGURATION (TOP VIEW)**



Pin Name	Function
A0 - A7, A8R - A11R	Address Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{LCAS}}$	Lower Byte Column Address Strobe
$\overline{\text{UCAS}}$	Upper Byte Column Address Strobe
DQ1 - DQ16	Data Input/Data Output
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
V <sub>CC</sub>	Power Supply (5 V)
V <sub>SS</sub>	Ground (0 V)
NC	No Connection

Note : The same power supply voltage must be provided to every V<sub>CC</sub> pin, and the same GND voltage level must be provided to every V<sub>SS</sub> pin.

**BLOCK DIAGRAM**



**FUNCTION TABLE**

Input Pin					DQ Pin		Function Mode
RAS	LCAS	UCAS	WE	OE	DQ1 - DQ8	DQ9 - DQ16	
H	*	*	*	*	High-Z	High-Z	Standby
L	H	H	*	*	High-Z	High-Z	Refresh
L	L	H	H	L	D <sub>OUT</sub>	High-Z	Lower Byte Read
L	H	L	H	L	High-Z	D <sub>OUT</sub>	Upper Byte Read
L	L	L	H	L	D <sub>OUT</sub>	D <sub>OUT</sub>	Word Read
L	L	H	L	H	D <sub>IN</sub>	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	D <sub>IN</sub>	Upper Byte Write
L	L	L	L	H	D <sub>IN</sub>	D <sub>IN</sub>	Word Write
L	L	L	H	H	High-Z	High-Z	—

\*: "H" or "L"

## ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Voltage on $V_{CC}$ Supply Relative to $V_{SS}$	$V_{CC}$	-0.5 to 7	V
Short Circuit Output Current	$I_{OS}$	50	mA
Power Dissipation	$P_D^*$	1	W
Operating Temperature	$T_{opr}$	0 to 70	°C
Storage Temperature	$T_{stg}$	-55 to 150	°C

\*:  $T_a = 25^\circ\text{C}$

### Recommended Operating Conditions

( $T_a = 0^\circ\text{C}$  to  $70^\circ\text{C}$ )

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V
	$V_{SS}$	0	0	0	V
Input High Voltage	$V_{IH}$	2.4	—	$V_{CC} + 0.5^{*1}$	V
Input Low Voltage	$V_{IL}$	$-0.5^{*2}$	—	0.8	V

- Notes : \*1. The input voltage is  $V_{CC} + 2.0\text{V}$  when the pulse width is less than 20 ns (the pulse width is with respect to the point at which  $V_{CC}$  is applied).  
 \*2. The input voltage is  $V_{SS} - 2.0\text{V}$  when the pulse width is less than 20 ns (the pulse width is with respect to the point at which  $V_{SS}$  is applied).

### Capacitance

( $V_{CC} = 5\text{V} \pm 10\%$ ,  $T_a = 25^\circ\text{C}$ ,  $f = 1\text{MHz}$ )

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A7, A8R - A11R)	$C_{IN1}$	—	5	pF
Input Capacitance ( $\overline{\text{RAS}}$ , $\overline{\text{LCAS}}$ , $\overline{\text{UCAS}}$ , $\overline{\text{WE}}$ , $\overline{\text{OE}}$ )	$C_{IN2}$	—	7	pF
Output Capacitance (DQ1 - DQ16)	$C_{I/O}$	—	7	pF

DC Characteristics

( $V_{CC} = 5\text{ V} \pm 10\%$ ,  $T_a = 0^\circ\text{C}$  to  $70^\circ\text{C}$ )

Parameter	Symbol	Condition	MSM5116160 D/DSL-50		MSM5116160 D/DSL-60		MSM5116160 D/DSL-70		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
			Output High Voltage	$V_{OH}$	$I_{OH} = -5.0\text{ mA}$	2.4	$V_{CC}$	2.4		
Output Low Voltage	$V_{OL}$	$I_{OL} = 4.2\text{ mA}$	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	$I_{LI}$	$0\text{ V} \leq V_I \leq 6.5\text{ V}$ ; All other pins not under test = $0\text{ V}$	-10	10	-10	10	-10	10	$\mu\text{A}$	
Output Leakage Current	$I_{LO}$	DQ disable $0\text{ V} \leq V_O \leq V_{CC}$	-10	10	-10	10	-10	10	$\mu\text{A}$	
Average Power Supply Current (Operating)	$I_{CC1}$	$\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ cycling, $t_{RC} = \text{Min.}$	—	90	—	85	—	80	mA	1, 2
Power Supply Current (Standby)	$I_{CC2}$	$\overline{\text{RAS}}$ , $\overline{\text{CAS}} = V_{IH}$	—	2	—	2	—	2	mA	1
		$\overline{\text{RAS}}$ , $\overline{\text{CAS}}$	—	1	—	1	—	1	$\mu\text{A}$	1, 5
		$\geq V_{CC} - 0.2\text{ V}$	—	200	—	200	—	200	$\mu\text{A}$	1, 5
Average Power Supply Current ( $\overline{\text{RAS}}$ -only Refresh)	$I_{CC3}$	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}} = V_{IH}$ , $t_{RC} = \text{Min.}$	—	90	—	85	—	80	mA	1, 2
Power Supply Current (Standby)	$I_{CC5}$	$\overline{\text{RAS}} = V_{IH}$ , $\overline{\text{CAS}} = V_{IL}$ , DQ = enable	—	5	—	5	—	5	mA	1
Average Power Supply Current ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	$I_{CC6}$	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$	—	90	—	85	—	80	mA	1, 2
Average Power Supply Current (Fast Page Mode)	$I_{CC7}$	$\overline{\text{RAS}} = V_{IL}$ , $\overline{\text{CAS}}$ cycling, $t_{PC} = \text{Min.}$	—	85	—	80	—	75	mA	1, 3
Average Power Supply Current (Battery Backup)	$I_{CC10}$	$t_{RC} = 125\ \mu\text{s}$ , $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ , $t_{RAS} \leq 1\ \mu\text{s}$	—	400	—	400	—	400	$\mu\text{A}$	1, 4, 5
Average Power Supply Current ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self-Refresh)	$I_{CC8}$	$\overline{\text{RAS}} \leq 0.2\text{ V}$ , $\overline{\text{CAS}} \leq 0.2\text{ V}$	—	300	—	300	—	300	$\mu\text{A}$	1, 5

- Notes :
- $I_{CC}$  Max. is specified as  $I_{CC}$  for output open condition.
  - The address can be changed once or less while  $\overline{\text{RAS}} = V_{IL}$ .
  - The address can be changed once or less while  $\overline{\text{CAS}} = V_{IH}$ .
  - $V_{CC} - 0.2\text{ V} \leq V_{IH} \leq V_{CC} + 0.5\text{ V}$ ,  $-0.5\text{ V} \leq V_{IL} \leq 0.2\text{ V}$ .
  - SL version.

AC Characteristics (1/2)

(V<sub>CC</sub> = 5 V ±10%, T<sub>a</sub> = 0°C to 70°C) Note 1, 2, 3

Parameter	Symbol	MSM5116160 D/DSL-50		MSM5116160 D/DSL-60		MSM5116160 D/DSL-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
		Random Read or Write Cycle Time	t <sub>RC</sub>	90	—	110	—		
Read Modify Write Cycle Time	t <sub>RWC</sub>	131	—	155	—	185	—	ns	
Fast Page Mode Cycle Time	t <sub>PC</sub>	35	—	40	—	45	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t <sub>PRWC</sub>	76	—	85	—	100	—	ns	
Access Time from $\overline{\text{RAS}}$	t <sub>RAC</sub>	—	50	—	60	—	70	ns	4, 5, 6
Access Time from $\overline{\text{CAS}}$	t <sub>CAC</sub>	—	13	—	15	—	20	ns	4, 5
Access Time from Column Address	t <sub>AA</sub>	—	25	—	30	—	35	ns	4, 6
Access Time from $\overline{\text{CAS}}$ Precharge	t <sub>CPA</sub>	—	30	—	35	—	40	ns	4, 12
Access Time from $\overline{\text{OE}}$	t <sub>OEA</sub>	—	13	—	15	—	20	ns	4
Output Low Impedance Time from $\overline{\text{CAS}}$	t <sub>CLZ</sub>	0	—	0	—	0	—	ns	4
$\overline{\text{CAS}}$ to Data Output Buffer Turn-off Delay Time	t <sub>OFF</sub>	0	13	0	15	0	20	ns	7
$\overline{\text{OE}}$ to Data Output Buffer Turn-off Delay Time	t <sub>OEZ</sub>	0	13	0	15	0	20	ns	7
Transition Time	t <sub>T</sub>	3	50	3	50	3	50	ns	3
Refresh Period	t <sub>REF</sub>	—	64	—	64	—	64	ms	
Refresh Period (SL version)	t <sub>REF</sub>	—	128	—	128	—	128	ms	15
$\overline{\text{RAS}}$ Precharge Time	t <sub>RP</sub>	30	—	40	—	50	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t <sub>RAS</sub>	50	10,000	60	10,000	70	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t <sub>RASP</sub>	50	100,000	60	100,000	70	100,000	ns	
$\overline{\text{RAS}}$ Hold Time	t <sub>RSH</sub>	13	—	15	—	20	—	ns	
$\overline{\text{RAS}}$ Hold Time referenced to $\overline{\text{OE}}$	t <sub>ROH</sub>	13	—	15	—	20	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	t <sub>CP</sub>	7	—	10	—	10	—	ns	14
$\overline{\text{CAS}}$ Pulse Width	t <sub>CAS</sub>	13	10,000	15	10,000	20	10,000	ns	
$\overline{\text{CAS}}$ Hold Time	t <sub>CSH</sub>	50	—	60	—	70	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t <sub>CRP</sub>	5	—	5	—	5	—	ns	12
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t <sub>RHCP</sub>	30	—	35	—	40	—	ns	12
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t <sub>RCD</sub>	17	37	20	45	20	50	ns	5
$\overline{\text{RAS}}$ to Column Address Delay Time	t <sub>RAD</sub>	12	25	15	30	15	35	ns	6
Row Address Set-up Time	t <sub>ASR</sub>	0	—	0	—	0	—	ns	
Row Address Hold Time	t <sub>RAH</sub>	7	—	10	—	10	—	ns	
Column Address Set-up Time	t <sub>ASC</sub>	0	—	0	—	0	—	ns	11
Column Address Hold Time	t <sub>CAH</sub>	7	—	10	—	15	—	ns	11
Column Address to $\overline{\text{RAS}}$ Lead Time	t <sub>RAL</sub>	25	—	30	—	35	—	ns	
Read Command Set-up Time	t <sub>RCS</sub>	0	—	0	—	0	—	ns	11
Read Command Hold Time	t <sub>RCH</sub>	0	—	0	—	0	—	ns	8, 11
Read Command Hold Time referenced to $\overline{\text{RAS}}$	t <sub>RRH</sub>	0	—	0	—	0	—	ns	8

AC Characteristics (2/2)

(V<sub>CC</sub> = 5 V ±10%, T<sub>a</sub> = 0°C to 70°C) Note 1, 2, 3

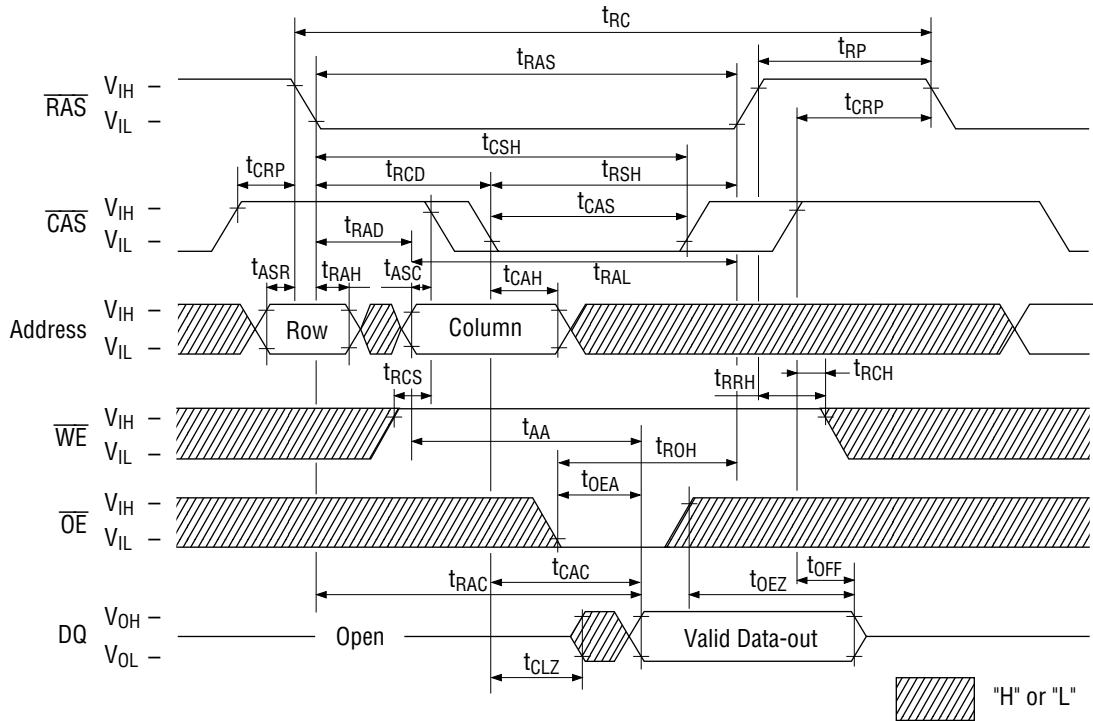
Parameter	Symbol	MSM5116160 D/DSL-50		MSM5116160 D/DSL-60		MSM5116160 D/DSL-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Command Set-up Time	t <sub>WCS</sub>	0	—	0	—	0	—	ns	9, 11
Write Command Hold Time	t <sub>WCH</sub>	7	—	10	—	15	—	ns	11
Write Command Pulse Width	t <sub>WCP</sub>	7	—	10	—	10	—	ns	
$\overline{\text{OE}}$ Command Hold Time	t <sub>OECH</sub>	13	—	15	—	20	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t <sub>RWL</sub>	13	—	15	—	20	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t <sub>CWL</sub>	13	—	15	—	20	—	ns	13
Data-in Set-up Time	t <sub>DS</sub>	0	—	0	—	0	—	ns	10, 11
Data-in Hold Time	t <sub>DH</sub>	7	—	10	—	15	—	ns	10, 11
$\overline{\text{OE}}$ to Data-in Delay Time	t <sub>OED</sub>	13	—	15	—	20	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t <sub>CWD</sub>	36	—	40	—	50	—	ns	9
Column Address to $\overline{\text{WE}}$ Delay Time	t <sub>AWD</sub>	48	—	55	—	65	—	ns	9
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t <sub>RWD</sub>	73	—	85	—	100	—	ns	9
$\overline{\text{CAS}}$ Precharge $\overline{\text{WE}}$ Delay Time	t <sub>CPWD</sub>	53	—	60	—	70	—	ns	9
$\overline{\text{CAS}}$ Active Delay Time from $\overline{\text{RAS}}$ Precharge	t <sub>RPC</sub>	5	—	5	—	5	—	ns	11
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Set-up Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ )	t <sub>CSR</sub>	10	—	10	—	10	—	ns	11
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Hold Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ )	t <sub>CHR</sub>	10	—	10	—	10	—	ns	12
$\overline{\text{RAS}}$ Pulse Width ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self-Refresh)	t <sub>RASS</sub>	100	—	100	—	100	—	μs	15
$\overline{\text{RAS}}$ Precharge Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self-Refresh)	t <sub>RPS</sub>	90	—	110	—	130	—	ns	15
$\overline{\text{CAS}}$ Hold Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self-Refresh)	t <sub>CHS</sub>	-50	—	-50	—	-50	—	ns	15

- Notes:
1. A start-up delay of 200  $\mu$ s is required after power-up, followed by a minimum of eight initialization cycles ( $\overline{\text{RAS}}$ -only refresh or  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh) before proper device operation is achieved.
  2. The AC characteristics assume  $t_T = 5$  ns.
  3.  $V_{IH}$  (Min.) and  $V_{IL}$  (Max.) are reference levels for measuring input timing signals. Transition times ( $t_T$ ) are measured between  $V_{IH}$  and  $V_{IL}$ .
  4. This parameter is measured with a load circuit equivalent to 2 TTL loads and 100 pF.
  5. Operation within the  $t_{RCD}$  (Max.) limit ensures that  $t_{RAC}$  (Max.) can be met.  $t_{RCD}$  (Max.) is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD}$  (Max.) limit, then the access time is controlled by  $t_{CAC}$ .
  6. Operation within the  $t_{RAD}$  (Max.) limit ensures that  $t_{RAC}$  (Max.) can be met.  $t_{RAD}$  (Max.) is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}$  (Max.) limit, then the access time is controlled by  $t_{AA}$ .
  7.  $t_{OFF}$  (Max.) and  $t_{OEZ}$  (Max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
  8.  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
  9.  $t_{WCS}$ ,  $t_{CWD}$ ,  $t_{RWD}$ ,  $t_{AWD}$  and  $t_{CPWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}$  (Min.), then the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If  $t_{CWD} \geq t_{CWD}$  (Min.),  $t_{RWD} \geq t_{RWD}$  (Min.),  $t_{AWD} \geq t_{AWD}$  (Min.) and  $t_{CPWD} \geq t_{CPWD}$  (Min.), then the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, then the condition of the data out (at access time) is indeterminate.
  10. These parameters are referenced to the  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$ , leading edges in an early write cycle, and to the  $\overline{\text{WE}}$  leading edge in an  $\overline{\text{OE}}$  control write cycle, or a read modify write cycle.
  11. These parameters are determined by the falling edge of either  $\overline{\text{UCAS}}$  or  $\overline{\text{LCAS}}$ , whichever is earlier.
  12. These parameters are determined by the rising edge of either  $\overline{\text{UCAS}}$  or  $\overline{\text{LCAS}}$ , whichever is later.
  13.  $t_{CWL}$  should be satisfied by both  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$ .
  14.  $t_{CP}$  is determined by the time both  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$  are high.
  15. Only SL version.

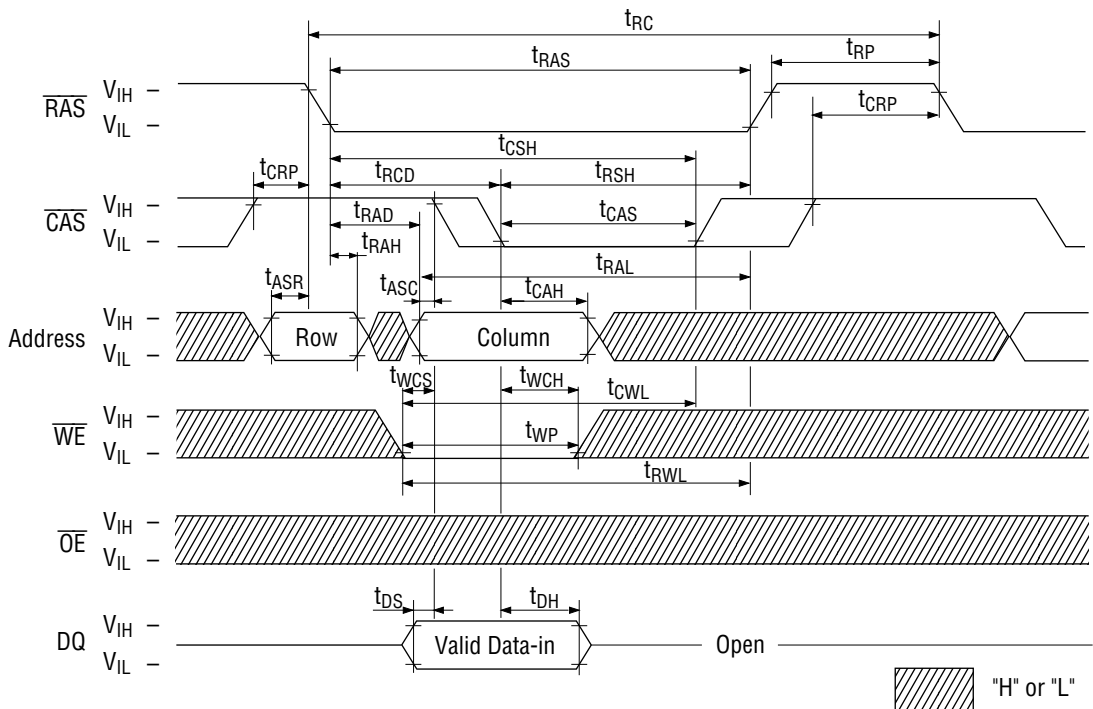


**TIMING WAVEFORM**

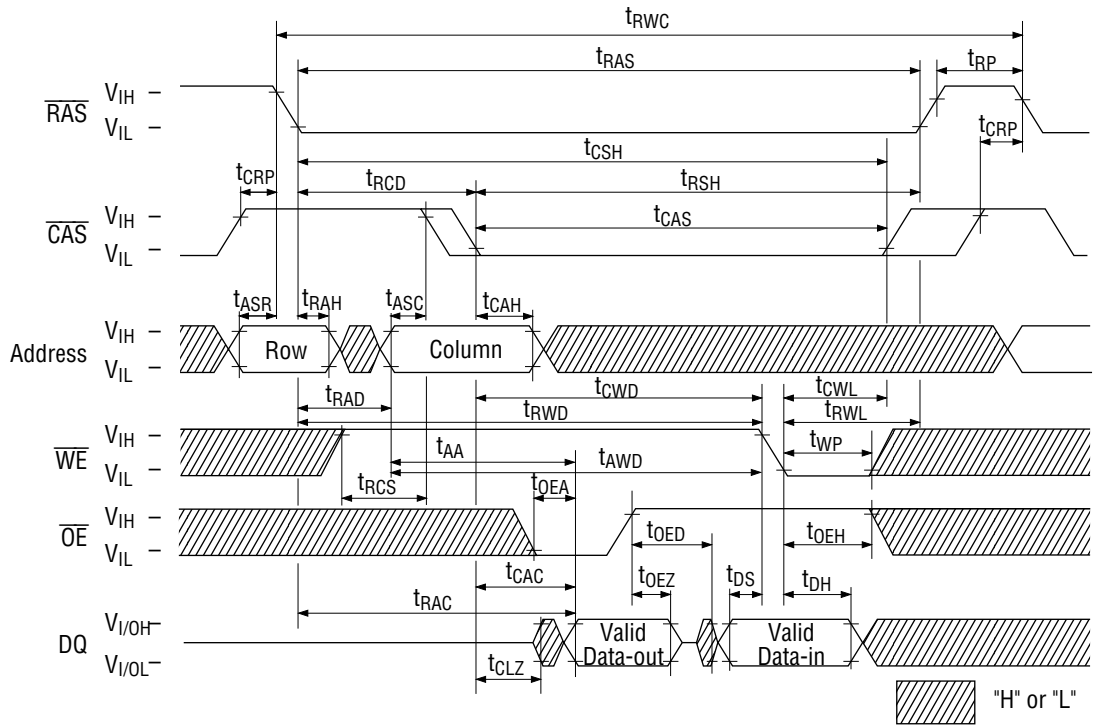
**Read Cycle**



**Write Cycle (Early Write)**



Read Modify Write Cycle

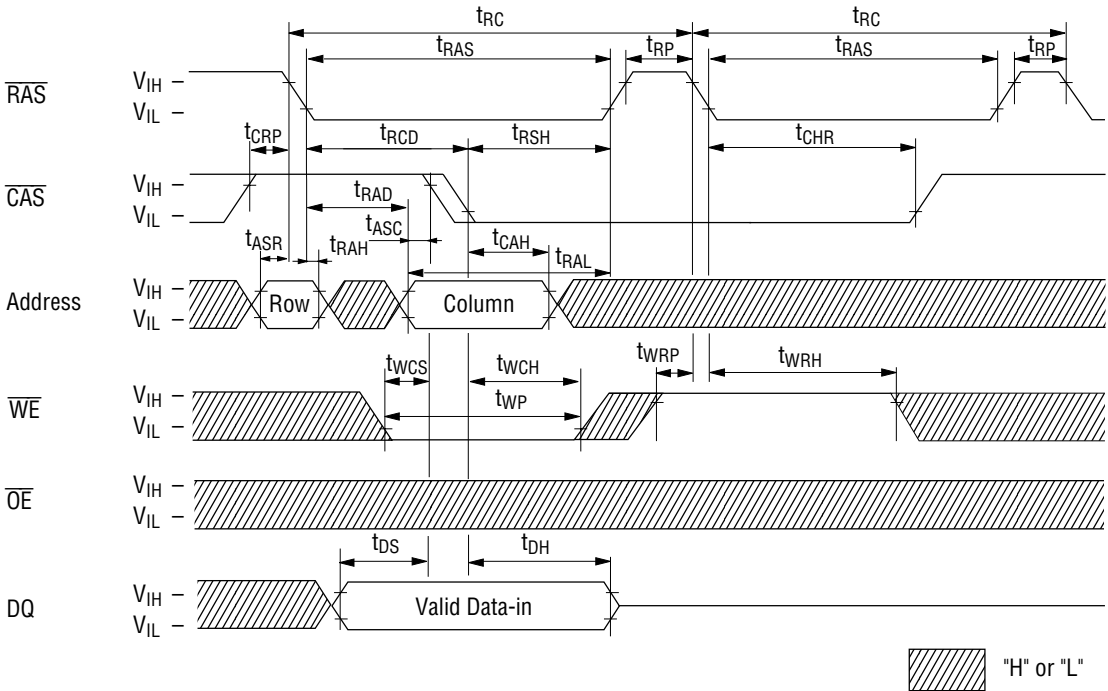




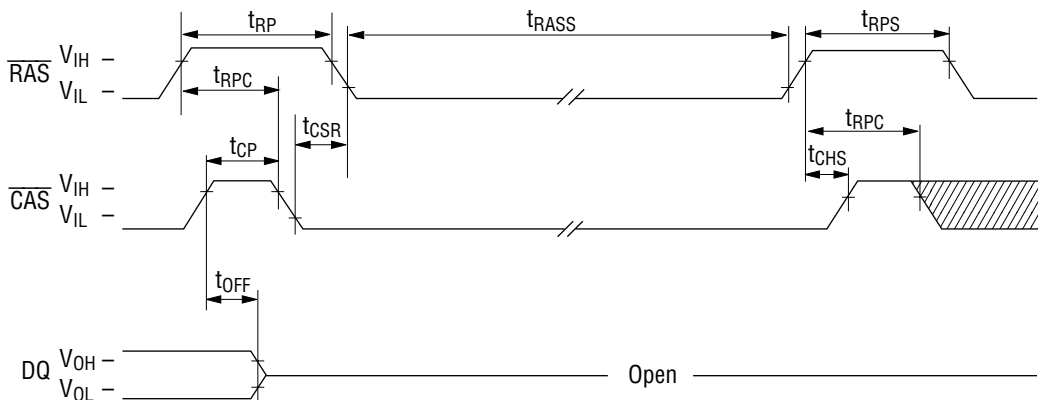




**Hidden Refresh Write Cycle**



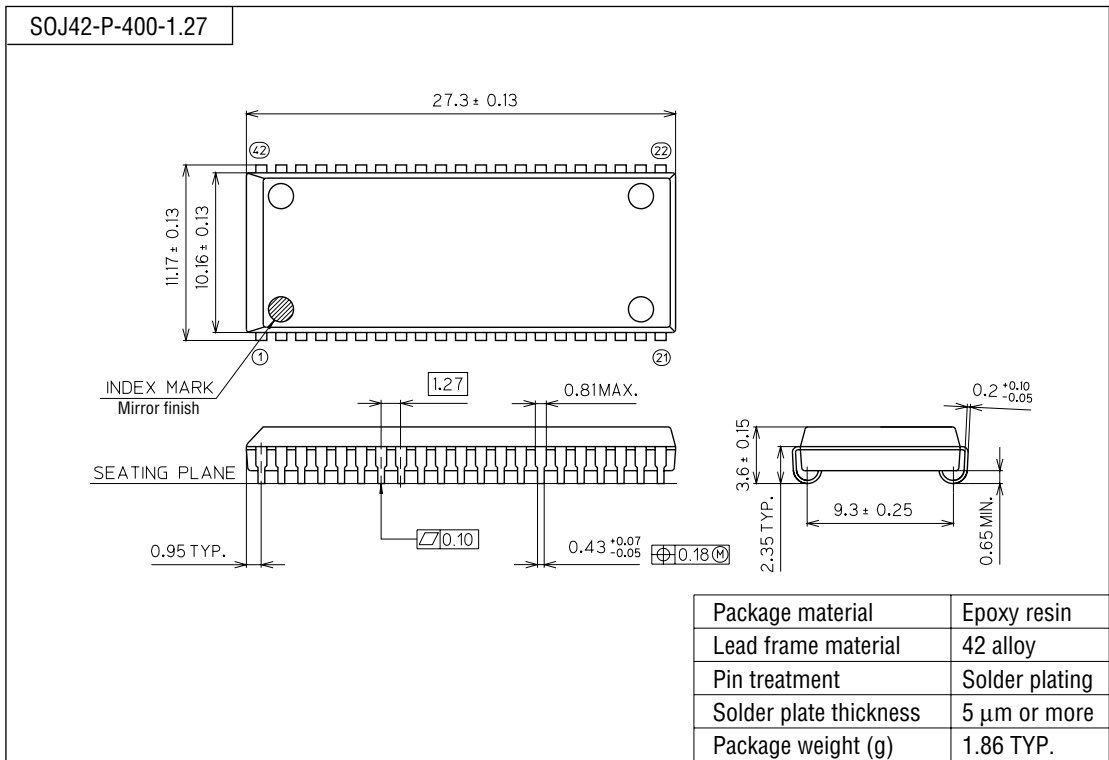
**CAS before RAS Self-Refresh Cycle**



**Note:**  $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$ , Address = "H" or "L" "H" or "L"  
Only SL version

**PACKAGE DIMENSIONS**

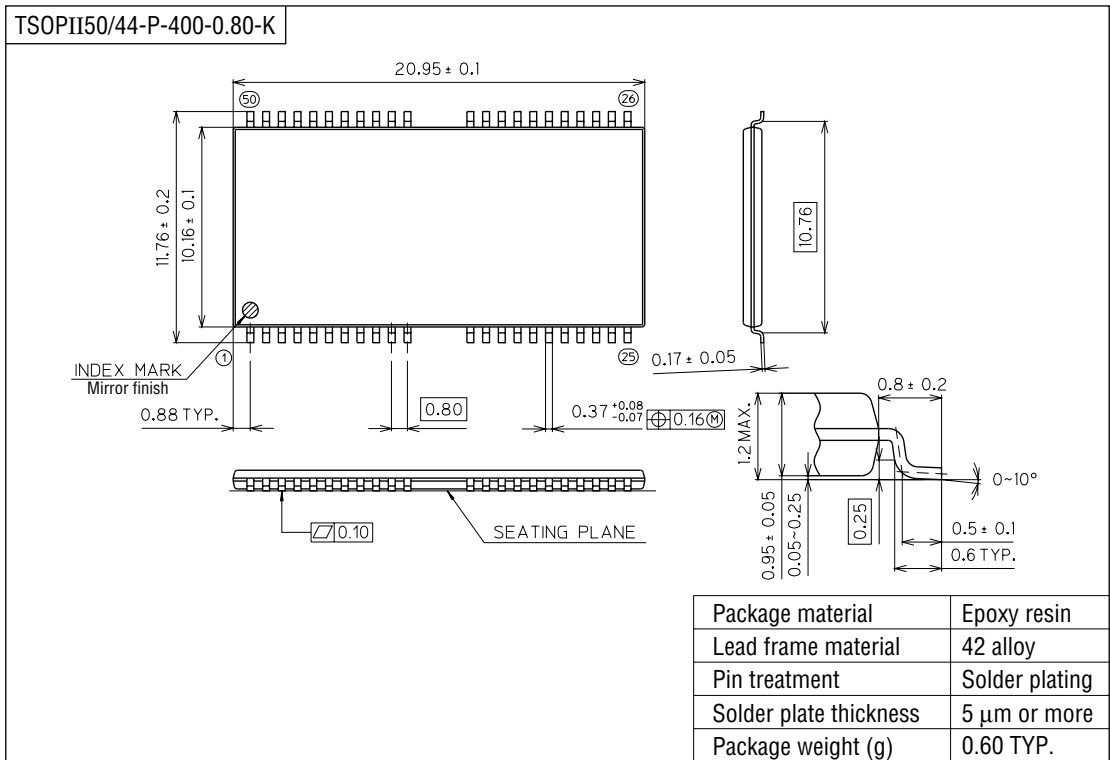
(Unit : mm)



**Notes for Mounting the Surface Mount Type Package**

The SOP, QFP, TSOP, TQFP, LQFP, SOJ, QFJ (PLCC), SHP, and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)



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2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.
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