OKI Semiconductor

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MSC7170-01

5×7 Dot Character × 16-Digit × 2-Line Display Controller/Driver with Keyscan Function

GENERAL DESCRIPTION

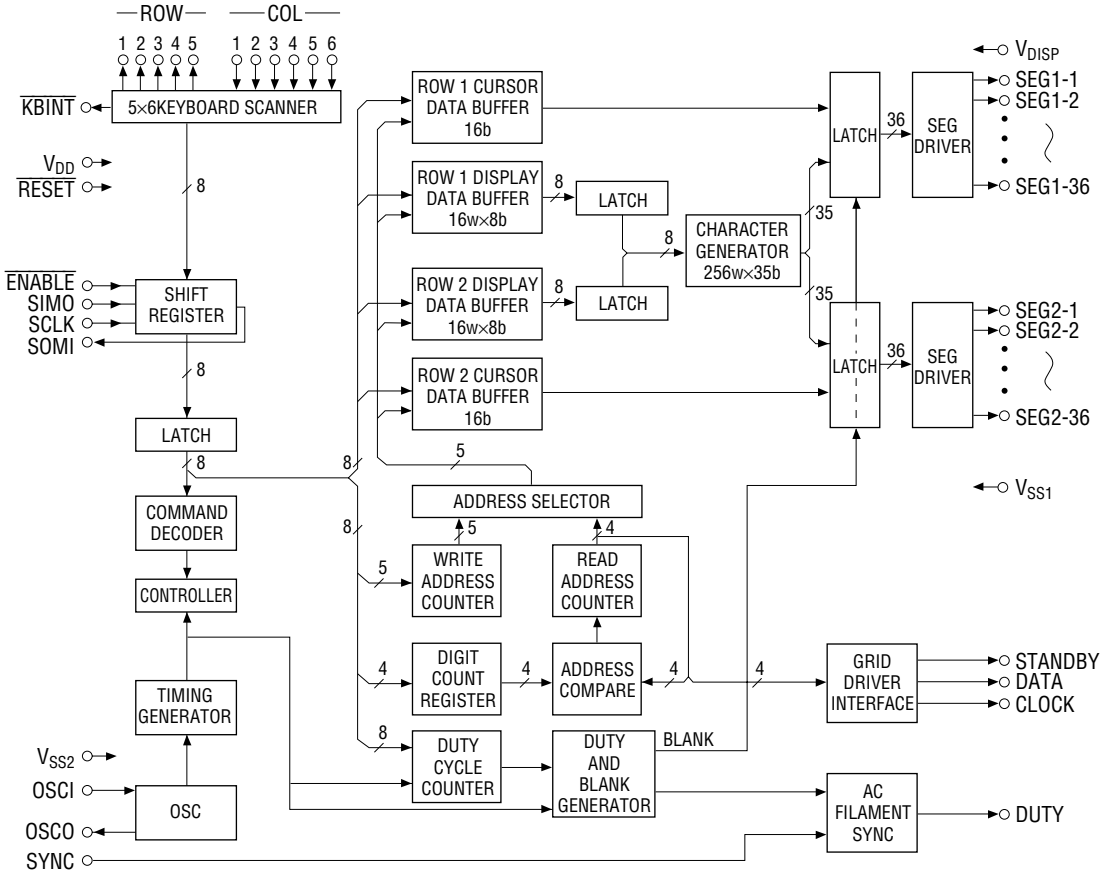
The MSC7170-01 is a display controller/segment driver containing a 5 × 6 keyscan circuit, designed for a 5 × 7 dot matrix type vacuum fluorescent (VF) display tube.

Use of the MSC1164 grid driver allows a maximum of 16-digit pair to be displayed, or use of the MSC7171 grid driver allows a maximum of 12 digit pairs to be displayed.

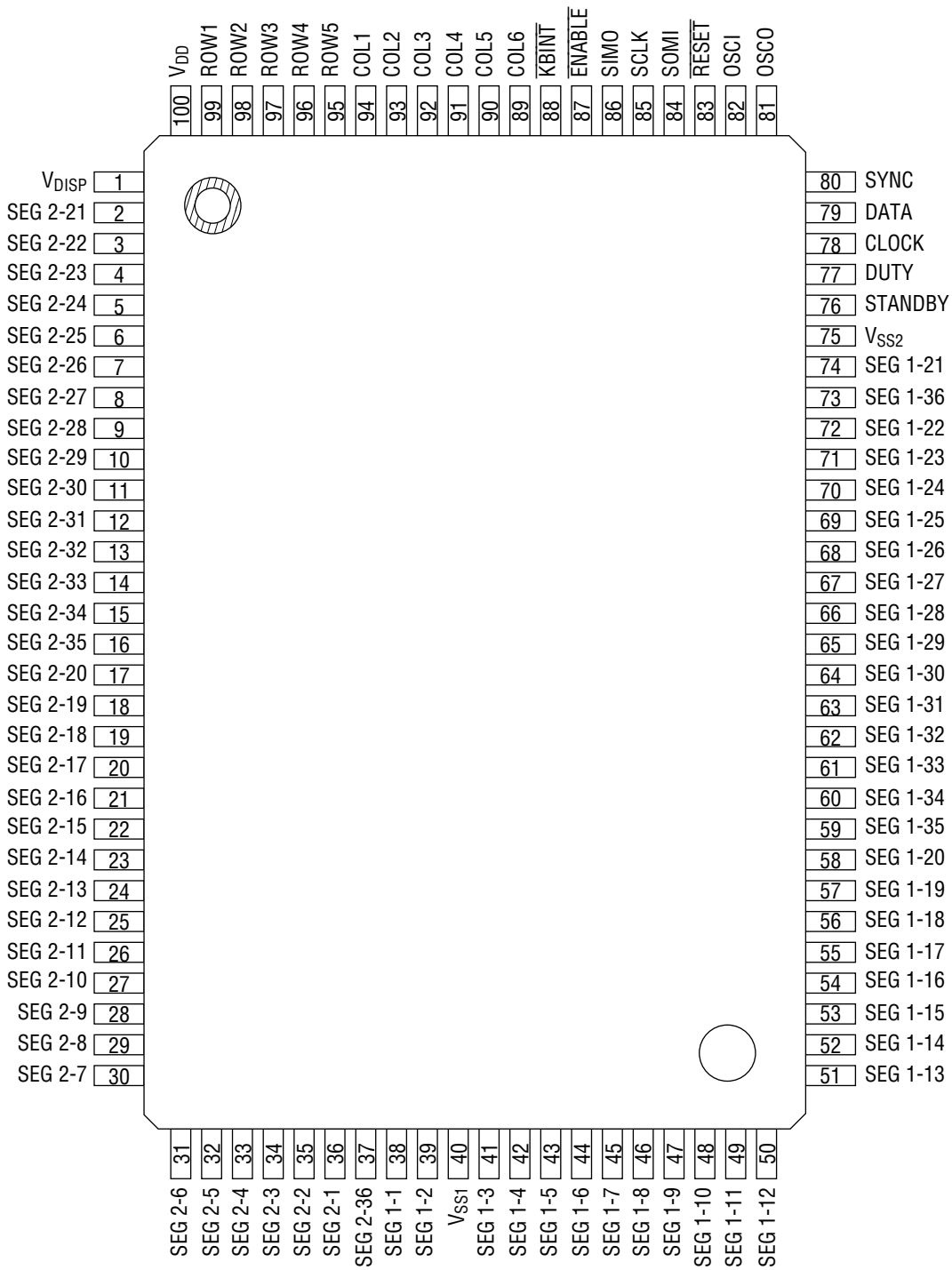
FEATURES

- Able to display 5 × 7 dot matrix type characters of a maximum of 16 digits × 2 lines (when MSC1164 is used)
- The number of display digits selectable in a range of 1 digit × 2 lines to 16 digits × 2 lines
- Standby function
  Combination of the MSC7171 grid driver and the MSC7170-01 decreases grid driver current during the standby mode of the driver.
- Display intensity selectable by 10-bit digital dimming
- Display characters selectable from among 256 types by internal PLA
- 8-bit synchronous serial data transfer
  SPI interface
- 5 × 6 keyscan circuit
- Driver output current (I_{OH}) : 1 mA (SEG1 to SEG35) : –15 mA (SEG36)
- Supply voltage: V_{DD} = 5 V±10% : V_{DISP} = 60 V (max.)
- Package:
  100-pin plastic QFP (QFP100-P-1420-0.65-BK) (Product name: MSC7170-01GS-BK)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



100-Pin Plastic QFP

Note: SEGn-x sequence depends on ROM code content and may be altered by changing segment number x relationship to ROM bit number. See Correspondence between Segment Output and VF Display Tube Dots.

PIN DESCRIPTIONS

Pin	Symbol	Description
1	V_{DISP}	High voltage power supply
2-36	SEG2-1 to SEG2-35	VF tube 5×7 dot anode driver outputs. These pins may be connected directly to the VF tube.
37	SEG2-36	VF tube cursor driver output.
38-39	SEG1-1 SEG1-2	VF tube 5×7 dot anode driver outputs. These pins may be connected directly to the VF tube.
40	V_{SS1}	High voltage ground
41-72	SEG1-3 to SEG1-35	VF tube 5×7 dot anode driver outputs. These pins may be connected directly to the VF tube.
73	SEG1-36	VF tube cursor driver output.
74	SEG1-21	VF tube 5×7 dot anode driver output. This pin may be connected directly to the VF tube.
75	V_{SS2}	Logic supply ground.
76	STANDBY	Grid driver standby output pin. A logic high level on this output forces the grid driver (MSC7171) into a low power standby mode.
77	DUTY	Duty cycle output pin.
78	CLOCK	Grid driver clock output pin.
79	DATA	Grid driver data output pin.
80	SYNC	AC filament synchronization input pin.
81	OSCO	Oscillator output pin. — Connects to crystal (or ceramic resonator) oscillator and capacitor. These pins have internal feedback resistors.
82	OSCI	Oscillator input pin.
83	$\overline{\text{RESET}}$	Reset input pin.
84	SOMI	SPI data output pin. Keyscan data is shifted out on the falling edge of SCLK.
85	SCLK	SPI clock input pin. Data is shifted in on the SIMO pin on the rising edge of SCLK.
86	SIMO	SPI data input pin. Command data is shifted in on the rising edge of SCLK.
87	$\overline{\text{ENABLE}}$	Chip select input pin. Interface to the microprocessor is possible only when a logic low level is applied to this pin. The SOMI output pin is tri-stated when $\overline{\text{ENABLE}}$ is at a logic high level so that multiple devices may use the SPI network.
88	$\overline{\text{KBINT}}$	Interrupt request output to the microprocessor for keyscan data read out. Keyscanning is started when any key is depressed or released. After completion of one cycle, $\overline{\text{KBINT}}$ goes to a logic low level to indicate new keyscan data is available. $\overline{\text{KBINT}}$ remains low until execution of Keyscan Data Output command.
89-94	COL6-1	Column 1-6 input pins from key switch matrix. A pull-up resistor is built in so that the pin is in the logic high state except when a key is depressed and a logic low level is input to the pin.

Pin	Symbol	Description
95-99	ROW5-1	Row 1-5 scanning signal output pins to key switch matrix. When any key is depressed or released, keyscanning is started and is continued until Keyscan Data Output command is executed. All Row 1-5 outputs go to logic low level when keyscanning is stopped.
100	V_{DD}	Logic voltage supply.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Logic Supply Voltage	V_{DD}	—	–0.3 to 6.0 *1	V
Driver Supply Voltage	V_{DISP}	—	–0.3 to 65 *1, 2	V
Input Voltage	V_{IN}	Applies to all inputs	–0.3 to V_{DD}+0.3 *1	V
Power Dissipation	P_D	Ta≤25°C	663	mW
Package Thermal Resistance	R_{j-a}	—	98 *3	°C/W
Driver Output Current	—	SEG1-1 to SEG1-35	–2	mA
		SEG2-1 to SEG2-35	–2	mA
		SEG1-36, SEG2-36	–15	mA
Storage Temperature	T_{STG}	—	–65 to 150	°C

Notes: *1 Voltage that can be applied to GND
*2 Stresses beyond the rating may cause permanent damage to the device.
*3 Package thermal resistance between junction and atomsphere.
Junction temperature T_j in the following expression must not exceed 150°C:
$T_j = P \times R_{j-a} + Ta$ (P: maximum IC power consumption)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Logic Circuit Supply Voltage	V_{DD}	Usable only for logic power terminal	4.5 to 5.5	V
Driver Supply Voltage	V_{DISP}	Usable only for driver power terminal	7 to 60	V
Operating Temperature	T_{op}	—	–40 to 85	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics

(Ta=–40 to 85°C, V_{DD}=4.5 to 5.5 V, V_{DISP}=7 to 60 V)

Parameter	Symbol	Condition	Min.	Max.	Unit	Applied Pin
"H" Input Voltage	V_{IH}	—	0.7 V_{DD}	—	V	All inputs
"L" Input Voltage	V_{IL}	—	—	0.3 V_{DD}	V	All inputs
"H" Input Current	I_{IH1}	V_{DD}=5.5 V V_{IN}=V_{DD}	–1	1	µA	SIMO, SCLK, $\overline{\text{ENABLE}}$, $\overline{\text{RESET}}$
	I_{IH2}		–30	30	µA	COL1-6, SYNC
"L" Input Current	I_{IL1}	V_{DD}=5.5 V V_{IN}=0.5 V	–1	1	µA	SIMO, SCLK, $\overline{\text{ENABLE}}$, $\overline{\text{RESET}}$
	I_{IL2}		–15	–160	µA	COL1-6, SYNC
"H" Output Voltage	V_{OH1}	I_{OH}=–500 µA	V_{DD}–0.6	—	V	OSCO
	V_{OH2}	I_{OH}=–1 mA	V_{DISP}–3	—	V	SEGn-1 to n-35, n=1, 2
	V_{OH3}	I_{OH}=–15 mA	V_{DISP}–4	—	V	SEG1-36, SEG2-36
	V_{OH4}	I_{OH}=–200 µA	4	—	V	DUTY, SOMI, $\overline{\text{KBINT}}$ DATA, CLOCK, STANDBY
"L" Output Voltage	V_{OL1}	I_{OL}=500 µA	—	V_{SS}+0.6	V	OSCO
	V_{OL2}	I_{OL}=100 µA	—	2.5	V	SEGn-1 to n-35, n=1, 2
	V_{OL3}	I_{OL}=3 mA	—	3	V	SEG1-36, SEG2-36
	V_{OL4}	I_{OL}=200 µA	—	0.5	V	ROW1-5, DUTY, SOMI, $\overline{\text{KBINT}}$,DATA, CLOCK, STANDBY
Power Supply	I_{DD1}	All SEGs on, 16-digit display, maximum brightness, no load, f_{osc}=4 MHz	—	10	mA	V_{DD}–V_{SS}
	I_{DD2}	All SEGs off	—	10	mA	
	I_{DD3}	Low power mode	—	25	µA	
	I_{DISP1}	All SEGs on, 16-digit display, maximum brightness, no load, f_{osc}=4 MHz	—	15	mA	V_{DISP}–V_{SS}
	I_{DISP2}	All SEGs off	—	1	µA	

AC Characteristics (1/2)

(Ta=–40 to 85°C, V_{DD}=4.5 to 5.5V, V_{DISP}=7 to 60 V, f_{OSC}=4 MHz, 12-digit display)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
ENABLE Setup Time	t_{ES}	See Fig. 1 (Data Transfer Timing)	50	—	—	ns
ENABLE Hold Time	t_{EH}	See Fig. 1 (Data Transfer Timing)	4	—	—	µs
SCLK Frequency	t_{CP}	See Fig. 1 (Data Transfer Timing)	—	0.5	2	MHz
SCLK Pulse Width	t_{cw}	See Fig. 1 (Data Transfer Timing)	250	—	—	ns
SCLK Rise/Fall Time	t_{cr}/t_{cf}	See Fig. 1 (Data Transfer Timing)	—	—	500	ns
SIMO Setup Time	t_{DS}	See Fig. 1 (Data Transfer Timing)	50	—	—	ns
SIMO Hold Time	t_{DH}	See Fig. 1 (Data Transfer Timing)	120	—	—	ns
SOMI Output Enable	t_{OE}	Enable to SOMI valid	—	—	200	ns
SOMI Output Disable	t_{OD}	Enable to SOMI tri-state	—	—	200	ns
SCLK to SOMI Delay	t_{PD}	See Fig. 1 (Data Transfer Timing)	—	—	100	ns
Byte Length	t_{BYTE}	MSB to LSB See Fig. 2 (Example of Data Transfer)	3.5	—	—	µs
Byte Delay	t_{DELAY}	MSB to LSB See Fig. 2 (Example of Data Transfer)	—	—	20	µs
SYNC Frequency	t_{SYNC}	Duty cycle=50%, f_{OSC}–4 MHz 12-digit display	0.4 *1	—	250	kHz
SEGn Pulse Width	t_{SEG}	f_{OSC}=4 MHz See Fig. 5 (Duty Cycle Timing) C_I=20pF	—	10	—	µs
Operating Frequency	t_{OSC}	Self-oscillation	1.5	4	4.5	MHz
DUTY Period	t_{GRID}	f_{OSC}=4 MHz, See Fig. 3 (12-digit Display Cycle Timing)	—	256	—	µs
Blank Interval (min.)	t_{BLANK}	f_{OSC}=4 MHz See Fig. 3 (12-digit Display Cycle Timing) t_{BLANK}=48/f_{OSC}	—	12	—	µs
DATA Pulse Width High	t_{DW}	f_{OSC}=4 MHz See Fig. 5 (Duty Cycle Timing)	—	256	—	µs
DATA Period	t_{DATA}	f_{OSC}=4 MHz See Fig. 3 (12-digit Display Cycle Timing)	—	3072	—	µs
DATA to CLOCK Delay	t_{DC}	f_{OSC}=4 MHz See Fig. 5 (Duty Cycle Timing)	—	5	—	µs
CLOCK Pulse Width	t_{PW}	f_{OSC}=4 MHz See Fig. 5 (Duty Cycle Timing)	—	250	—	µs
CLOCK Cycle	t_{CLOCK}	f_{OSC}=4 MHz See Fig. 5 (Duty Cycle Timing)	—	256	—	µs
Keyscan Cycle Time	t_{SCAN}	f_{OSC}=4 MHz See Fig. 6 (Keyscan Timing)	—	40	—	µs

AC Characteristics (2/2)

(Ta=–40 to 85°C, V_{DD}=4.5 to 5.5 V, V_{DISP}=7 to 60 V, f_{OSC}=4 MHz, 12-digit display)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Keyscan Pulse Width	t_{SPW}	f_{OSC}=4 MHz, See Fig. 6 (Keyscan Timing)		—	8	—	µs
Wake-up Time	t_{WAKE}	Keypress to KBINT at "L" level f_{OSC}=4 MHz	Ceramic resonator	—	—	5	ms
			Crystal	—	—	10	
Slew Rate (SEGn-1 to SEGn-35)	t_r	C_L=20 pF, V_{DISP}=60 V, V_{OL}=6 V, V_{OH}=50 V		0.5	1.3	5	µs
	t_f			1	3.4	5	µs
Slew Rate (SEGn-36)	t_r	C_L=20 pF, V_{DISP}=60 V, V_{OL}=6 V, V_{OH}=50 V		0.2	—	5	µs
	t_f			0.1	—	5	µs
Slew Rate (DUTY, DATA, CLOCK)	t_r/t_f	V_{OL}=0.1 V_{DD}, V_{OH}=0.9 V_{DD}, C_L=10 pF		5	20	200	ns
Input Capacitance	C_I	all pins		—	6	—	pF

*1) For the minimum value when digits other than 12 digits are displayed, refer to the following expression.

$$t_{SYNC\ (Min)} > \frac{f_{OSC}}{1024 \times (\text{digit display number})}$$

TIMING DIAGRAM

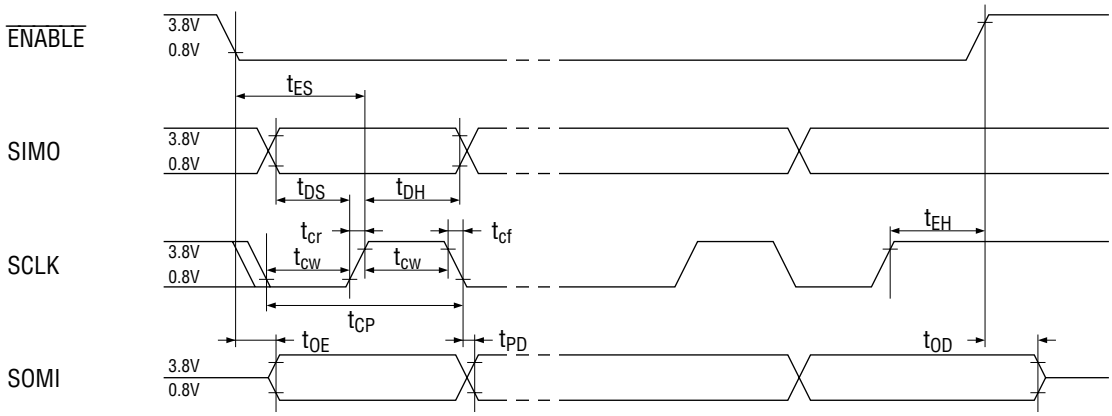


Figure 1. Data Transfer Timing

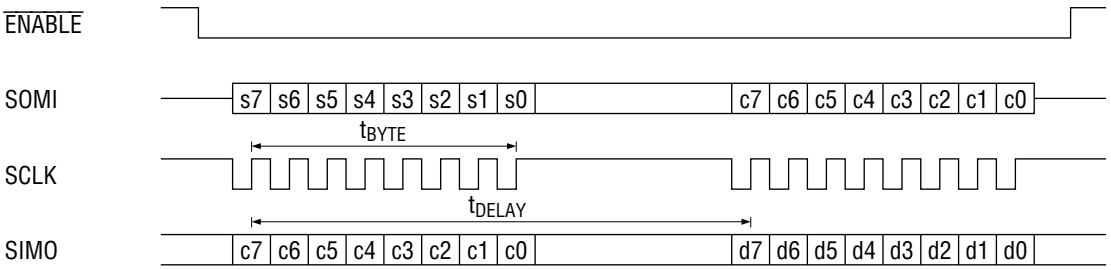


Figure 2. Data Transfer Example

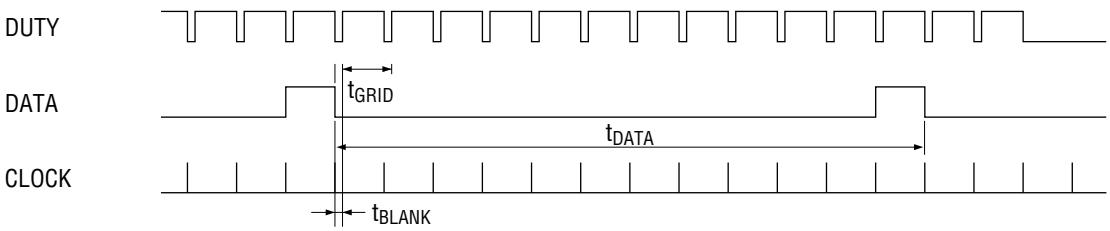


Figure 3. 12-Digit (n=12) Display Cycle Timing

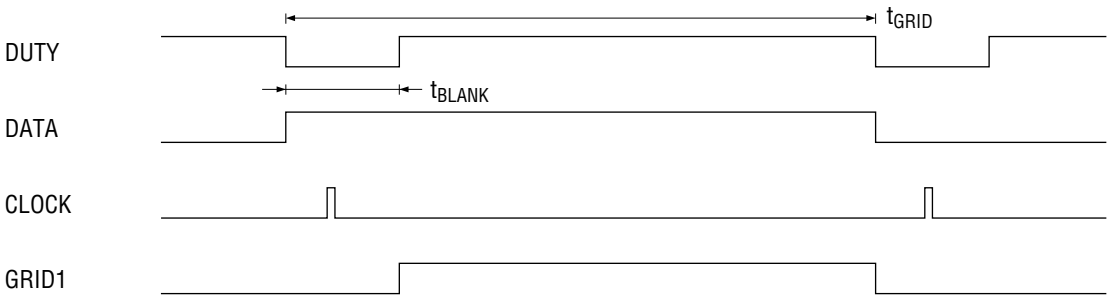
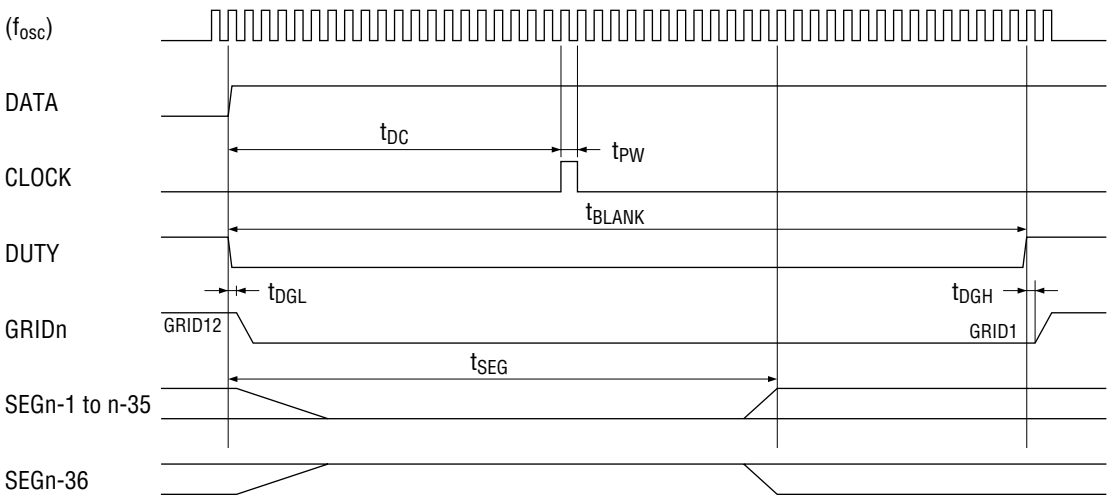


Figure 4. GRID1 Interval Timing



Note: (f_{OSC}) is internal to the MSC7170 and not visible externally.
GRIDn are outputs of, and t_{DGL} and t_{DGH} are timig parameters of, the MSC7171 (grid driver).

Figure 5. Duty Cycle Timing

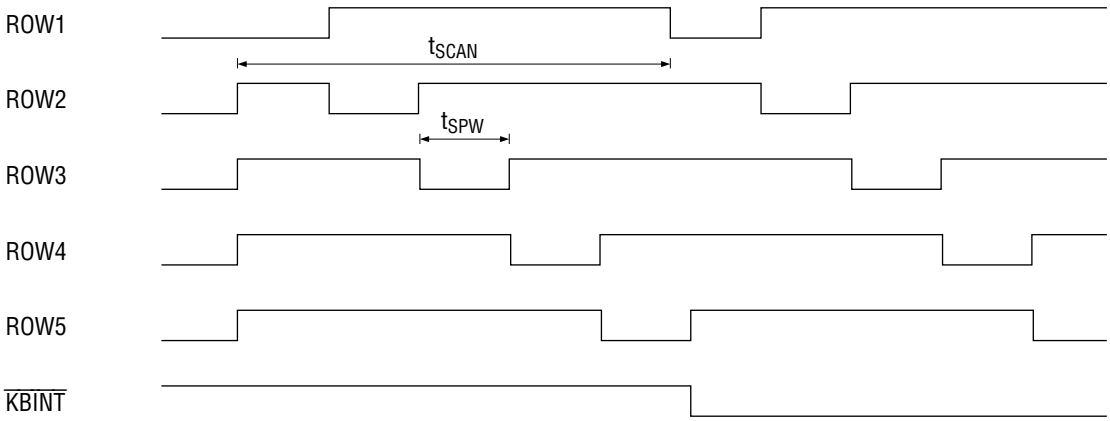


Figure 6. Keyscan Timing

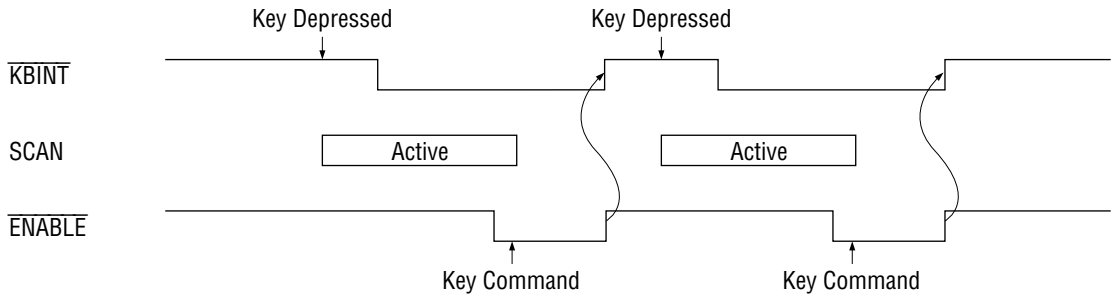


Figure 7-1. Single Keypress/Single Read

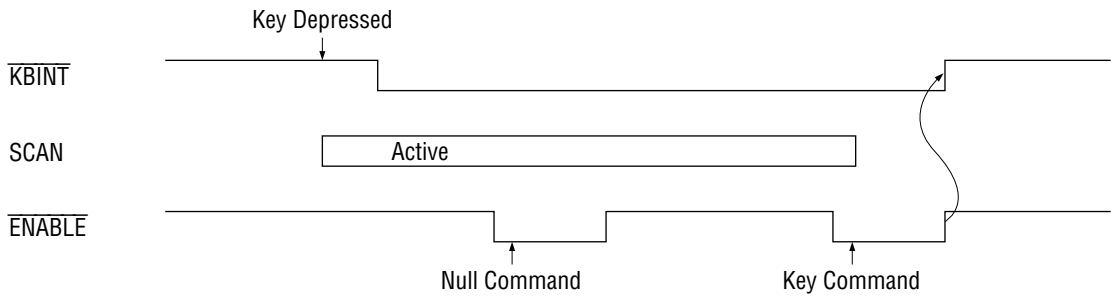


Figure 7-2. Single Keypress/Multiple Read

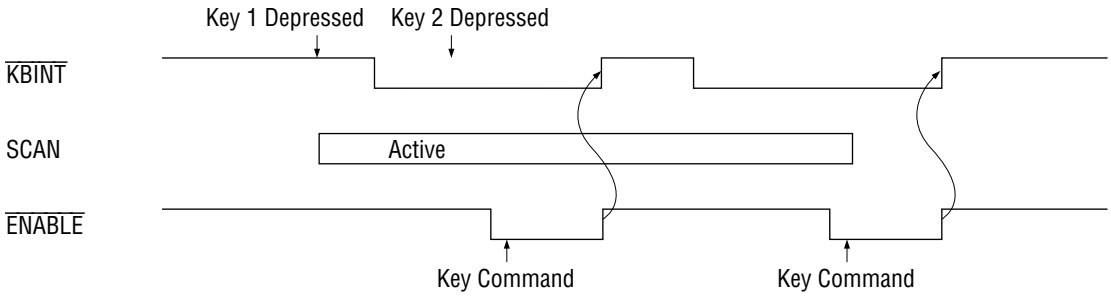


Figure 7-3. Multiple Keypress/Multiple Interrupt

Figure 7. Typical Cases of Keyscan Operation

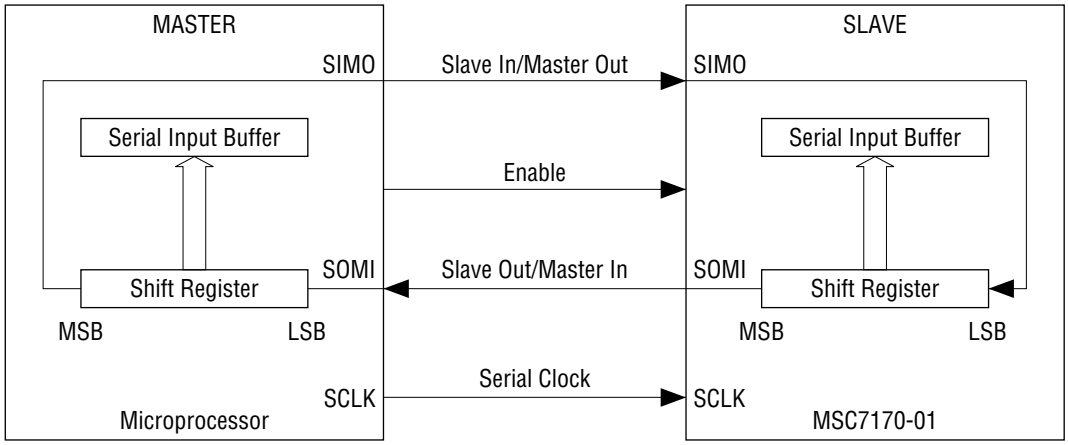
FUNCTIONAL DESCRIPTION

The MSC7170-01 (Dot Matrix VF Segment Driver) in conjunction with the MSC7171 (Dot Matrix VF Grid Driver) is capable of controlling a variety of dot matrix VF displays and keyboards. The MSC7170-01 is designed to drive the anodes of up to 32 dot matrix digits in two lines. Each digit is a 5 × 7 matrix of anodes, or dots, which requires a total of 70 segment driver outputs. There are two extra segment outputs for supplying drive to dedicated annunciators. The grid drivers of the MSC7171 are controlled by the MSC7170-01 through a two-line serial interface and a duty cycle control line, DUTY (see APPLICATION CIRCUIT). Additionally, the MSC7170-01 provides 10-bit digital dimming of all display data, a 5×6 keyscan function allowing control of up to 30 key pads and a low-power standby mode. The MSC7170-01 is controlled through a standard SPI interface.

All MSC7170-01 internal timings are generated through an external 4 MHz (typ) ceramic oscillator. One display cycle is defined as up to 16384 periods of the 4 MHz (250 ns) reference in increments of 1024 periods, one for each pair of digits displayed. Display intensity is determined by the duty cycle of the DUTY output within one display increment divided by the total number of increments, or character pairs, displayed (see Display Duty Cycle Set and Number of Display Digit Pairs Set commands below). The maximum duty cycle is defined as 976 out of 1024 increments or 95.3 percent.

The MSC7170-01 is capable of synchronizing the DUTY signal with an AC filament to avoid visible flicker during dimming conditions. This is required in VF tubes of greater than 100 mm, equivalent to 14 digits, in length. Synchronization is accomplished by alternately initiating display cycles coincident with rising and falling edges of the filament voltage. Upon completion of a rising/falling edge display cycle, the MSC7170-01 will wait for a falling/rising edge before initiating the next display cycle. The MSC7170-01 detects rising and falling edges of a CMOS-compatible SYNC input derived directly from the filament voltage. The amount of hold time between display cycles varies between no delay as a minimum and the period of the filament voltage as maximum. The amount of delay should be consistent for all display cycles assuming that the filament frequency is well defined.

The MSC7170-01 is controlled through a Serial Peripheral Interface (SPI) compatible communications port. The SPI is a high-speed synchronous serial I/O port that shifts a serial bit stream of eight data bits into or out of a device at a bit transfer rate programmed in a controlling device. The figure below shows a typical connection of the SPI for communications between a master (radio microprocessor) and slave (MSC7170-01). Three I/O pins are associated with the SPI interface — SPI slave-in master-out (SIMO), SPI slave-out master-in (SOMI), and SPI serial clock (SCLK). Additionally, a separate input pin is used to enable the MSC7170-01 to communicate with the microprocessor through this interface.



SPI Master/Slave Connection

The microprocessor provides the serial clock (500 kHz typ.) to all devices on the SPI network with a CLOCK POLARITY of 1 (inactive level is high). Data is transferred from the master (microprocessor) to the salve (MSC7170-01) over the SIMO line, while data is transferred from the slave to the master over the SOMI line. Data is clocked out of the transmitting device on the falling edge of SCLK and latched into the receiving device with the rising edge of SCLK. ALL data transmissions are made MSB (b7) first.

A typical data transfer cycle between the microprocessor and the MSC7170-01 is initiated by first bringing the $\overline{\text{ENABLE}}$ line low. The first byte transmitted defines the command or operation to be executed. All remaining bytes received, prior to $\overline{\text{ENABLE}}$ being returned high, are treated as data bytes for that operation. Each command or operation executed requires a separate $\overline{\text{ENABLE}}$ transfer cycle.
The maximum waiting period between byte transfers, measured from MSB to LSB, is 20 msec. All activity on the SCLK and SIMO pins while $\overline{\text{ENABLE}}$ is high is ignored. Additionally, the SOMI pin shall be in a tri-state condition when $\overline{\text{ENABLE}}$ is high so that other SPI devices on the network may drive the line without contention.

The MSC7170-01 controls up to 30 key pads via a 5 controls up to 30 key pads via a 5×6 key scan circuit. COL1 to 6 (inputs) and ROW1 to 5 (outputs) are connected to an external switch matrix with an impedance of 500Ω max. The ROW1 to 5 outputs start scanning only when a depression or release of any key is detected. Upon completion of the first keyscan cycle, see Figure 6, the keyboard interrupt, $\overline{\text{KBINT}}$, output is pulled low to indicate availability of new keyscan data. The keyscan circuit continues to scan and $\overline{\text{KBINT}}$ remains low until the keyscan data has been read using the Keyscan Data Output Command. In the event of a multiple key depression, a second interrupt will be generated following the clearing of the first interrupt. A stuck key switch will not generate multiple interrupts since only state transitions are detected by the keyscan circuitry.

Keyscan data may be read without stopping the keyscan by using the Null Command. The keyscan data is transmitted to the microprocessor by rows as shown in the Output Data Bytes section. The output of keyscan data wraps around to the first byte for SPI transactions of more than six bytes. After completion of the last keyscan cycle all ROW outputs go to low level.

Key switch data is latched internally for transfer to the microprocessor via the SPI port. The microprocessor may use $\overline{\text{KBINT}}$ as an interrupt request or for polling the MSC7170-01 to determine when new keyscan information is available. As an alternative for polling, the MSC7170-01 continuously outputs a status byte during any SPI transaction, with the exceptions of the Null Command and the Keyscan Data Output Command. An all zeros (00h) byte indicates the presence of new keyscan information while all ones (FFh) indicate no new keyscan information. For the Null and Keyscan Data Output commands, the first byte output is still the status byte followed by five bytes containing the data from the five keyscan rows as described above and in the Output Data Bytes section. The status byte is reset upon completion of a Keyscan Data Output command in the same fashion as $\overline{\text{KBINT}}$.

The MSC7170-01 can also be commanded into a low power or "standby" mode (see Mode Set command). In this mode all operation, including the internal oscillator, of the MSC7170-01 ceases. The only exception is the key scan detection circuitry which, on any key pad activity (depress or release), will cause the MSC7170-01 to return to normal operation. The MSC7170-01 will be fully operational within 10 msec (max) after return to normal operation. The wake-up cycle includes a full scan of the key matrix. $\overline{\text{KBINT}}$ will be pulled low to indicate full wake-up. Normal operation is also resumed when the $\overline{\text{ENABLE}}$ line is taken low. In this case, a scan of the key matrix is not executed, nor is the $\overline{\text{KBINT}}$ line pulled low to indicate full wake-up.

The RESET and $\overline{\text{ENABLE}}$ lines shall be maintained at logic high levels during standby operation. All segment outputs go to a high impedance state while in standby mode. The SPI interface lines (SLCK, SIMO, and SOMI) will not interfere with the operation of the SPI network when the standby mode is properly selected. To ensure correct operation of the SPI network, the standby mode of the MSC7170-01 should always be selected before the logic supply is switched off.

The following sequence of events should be followed to enter standby mode:

1) Set duty cycle to zero percent
2) Turn off high voltage (V_{DISP})
3) Send low power (standby) "on" command

Following wake-up, the high voltage should be turned on prior to setting a duty cycle greater than zero percent.

The MSC7170-01 may be commanded into Blank and Lamp Test modes. For Blank mode, the DUTY and SEGn-1 to SEGn-35 outputs remain at a continuous low level while the SEGn36 outputs assume a high level. The outputs remain at this level until the command is deselected. For Lamp Test mode, the DUTY output assumes a maximum duty cycle condition and the SEGn outputs are all forced to the on condition regardless of input data.

The MSC7170-01 accepts a reset signal from the microprocessor or other controller. There shall be no internal pull-up resistor on this signal. The state of the MSC7170-01 following a reset is as follows:

a) All segment driver outputs are low
b) The number of display digits is 16×2.
c) The display duty cycle is set to 0
d) Display Data Buffers are not cleared
e) SPI registers are reset
f) Keyscan registers are reset

The MSC7170-01 is protected against thermal overload or other failure caused by extreme display configurations (e.g. Lamp Test) or due to output short circuits to high voltage supply, ground, or another output. These shall be no performance degradation once the short circuit is removed.

Commands Description

No.	Instruction	Byte	c7	c6	c5	c4	c3	c2	c1	c0
0	Address Setup	1	1	0	0	0	X	X	X	X
		2	X	X	X	a4	a3	a2	a1	a0
1	Character Code Setup	1	1	0	0	1	X	X	X	X
		2	b7	b6	b5	b4	b3	b2	b1	b0
2	Display Duty Cycle Setup	1	1	0	1	0	X	X	DC9	DC8
		2	DC7	DC6	DC5	DC4	DC3	DC2	DC1	DC0
3	Display Digits Setup	1	1	0	1	1	n3	n2	n1	n0
4	Mode Setup	1	1	1	0	0	X	m2	m1	m0
5	Cursor Setup	1	1	1	0	1	X	X	X	X
		2	C1-7	C1-6	C1-5	C1-4	C1-3	C1-2	C1-1	C1-0
		3	C1-15	C1-14	C1-13	C1-12	C1-11	C1-10	C1-9	C1-8
		4	C2-7	C2-6	C2-5	C2-4	C2-3	C2-2	C2-1	C2-0
		5	C2-15	C2-14	C2-13	C2-12	C2-11	C2-10	C2-9	C2-8
6	Keyscan Data Output	1	1	1	1	0	X	X	X	X
7	Null	1	0	0	0	0	0	0	0	0

Address Setup Command

This command is used to setup a start position of display character code writing and must be executed before the desired character code is sent. In applications using less than the full 16-digit pair capability, only the first 2n memory locations are used. For example, if n = 12-digit pair is selected, only addresses 0 through 23 are used. Row 1 display data (SEG1 outputs) is stored in addresses 0 through 11 while Row 2 display data (SEG2 outputs) is stored in addresses 12 through 23. All bytes following Bytes 1 and 2 are treated as character code data bytes. Address 0 is set after reset.

	c7	c6	c5	c4	c3	c2	c1	c0
Byte 1	1	0	0	0	X	X	X	X

	d7	d6	d5	d4	d3	d2	d1	d0
Byte 2	X	X	X	a4	a3	a2	a1	a0

a4 to a0 : 00000=00h=0
: 11111=1Fh=31

Character Code Setup Command

This command is used to specify the character to be displayed in the display location previously specified by the Address Setup command. A built-in automatic address increment function simplifies writing more than one display character code. All bytes transmitted after Byte 2 are treated as character code data for successive locations. The internal address counter will be automatically incremented from the address set using the Address Set command through address 31 (or character 32), while executing valid write cycles, regardless of the number of digit pairs as defined using the Number of Display Digits Setup command. In the event that additional data is input to the MSC7170-01 following a valid write to address 31, the address counter will wrap-around and continue to increment (to address 0 etc.) with write cycles disabled. This prevents overwriting of the memory.

	c7	c6	c5	c4	c3	c2	c1	c0
Byte 1	1	0	0	1	X	X	X	X

	d7	d6	d5	d4	d3	d2	d1	d0
Byte 2	b7	b6	b5	b4	b3	b2	b1	b0

b4 to b0 : 8-bit character code — Select one of 256 codes

Display Duty Cycle Setup Command

This command is used to set the duty cycle of the display. The time allocated to a 1-digit display is 1024T, where T is the period of the internal oscillator (f_{OSC}). The display time for each digit may be specified as 0 to 976T in increment of T. Entries greater than 976 default to 976. The display duty cycle is calculated by dividing the input duty cycle value, DC, by 1024 times the number of digits, n, commanded to display. Note that the percent duty cycle depends on how many digits (characters) are displayed.

	c7	c6	c5	c4	c3	c2	c1	c0
Byte 1	1	0	1	0	X	X	DC9	DC8

	d7	d6	d5	d4	d3	d2	d1	d0
Byte 2	DC7	DC6	DC5	DC4	DC3	DC2	DC1	DC0

Number of Display Digits Setup Command

This command is used to set the number of digits to be displayed. The number of digits selectable ranges from 1 to 16.

	c7	c6	c5	c4	c3	c2	c1	c0
Byte 1	1	0	1	1	n3	n2	n1	n0

n3 to n0 : 0000=0h=16-digit pair
: 0001=1h=1-digit pair
:
: 1111=Fh=15-digit pair

Mode Setup Command

This command is used to select an operation mode for the MSC7170-01. Lamp Test and Blank modes turns all 36 segments of each displayable digit (as set by the Number of Display Digits Setup command) to the ON and OFF states respectively. The contents of the display buffer are not affected by either of these modes. The normal operation mode returns after reset. Low Power mode is described earlier.

	c7	c6	c5	c4	c3	c2	c1	c0
Byte 1	1	1	0	0	X	m2	m1	m0

m2	m1	m0	Mode
0	0	0	Normal operation
0	0	1	Lamp test (All display ON)
0	1	0	Low power
0	1	1	Normal operation
1	0	0	Blank (All display OFF)
1	0	1	Normal operation
1	1	0	Normal operation
1	1	1	Normal operation

Cursor Setup Command

This command is used to specify the on/off state of cursor segments (SEGn-36) in the display. The cursor outputs are issued inversely to allow an external PNP transistor to be used in applications requiring high current drive capability. Therefore, a logic high, l, in a given bit position will turn on the associated cursor. In applications requiring low current (less than 15 mA) drive capability, the cursor outputs may drive the VF display tube directly. In these applications, setting to "0" turns on the cursor.

	c7	c6	c5	c4	c3	c2	c1	c0
Byte 1	1	1	0	1	X	X	X	X

	d7	d6	d5	d4	d3	d2	d1	d0
Byte 2	C1-7	C1-6	C1-5	C1-4	C1-3	C1-2	C1-1	C1-0
Byte 3	C1-15	C1-14	C1-13	C1-12	C1-11	C1-10	C1-9	C1-8
Byte 4	C2-7	C2-6	C2-5	C2-4	C2-3	C2-2	C2-1	C2-0
Byte 5	C2-15	C2-14	C2-13	C2-12	C2-11	C2-10	C2-9	C2-8

Keyscan Data Output Command

This command is used to read keyscan data via the SPI interface and has no effect on the operation or state of the display portion of the MSC7170-01. Upon completion of this command the $\overline{\text{KBINT}}$ output is reset to its non-active state and the keyscan function is stopped. All bytes after Byte 1 are ignored.

	c7	c6	c5	c4	c3	c2	c1	c0
Byte 1	1	1	1	0	X	X	X	X

NULL Command

This command has the same function as the Keyscan Data Output command with the exception that $\overline{\text{KBINT}}$ is not reset and the keyscan function continues to scan the key matrix. The keyscan may stop momentarily to prevent changing data while data output is in progress. All bytes after Byte 1 are ignored.

	c7	c6	c5	c4	c3	c2	c1	c0
Byte 1	0	0	0	0	0	0	0	0

Output Data Byte Description

• Status output

The following byte is output from the MSC7170-01 during execution of every SPI command with the exceptions of the Keyscan Data Output and Null commands. The status byte is issued for each byte of the input command sequence.

	d7	d6	d5	d4	d3	d2	d1	d0	
Byte 1	s7	s6	s5	s4	s3	s2	s1	s0	Status

s7 to s0: indicates change status from last SPI transaction
00h = change, FFh = no change

• Keyscan data output

The following bytes are output from the MSC7170-01 during execution of the Keyscan Data Output and Null commands. The output of keyscan data wraps around to byte 1 for transactions of more than six bytes.

	d7	d6	d5	d4	d3	d2	d1	d0	
Byte 1	X	X	s16	s15	s14	s13	s12	s11	Row 1
Byte 2	X	X	s26	s25	s24	s23	s22	s21	Row 2
Byte 3	X	X	s36	s35	s34	s33	s32	s31	Row 3
Byte 4	X	X	s46	s45	s44	s43	s42	s41	Row 4
Byte 5	X	X	s56	s55	s54	s53	s52	s51	Row 5

sij : i=ROW1 to 5, j =Col1 to 6
sij=1: Switch on
sij=0: Switch off

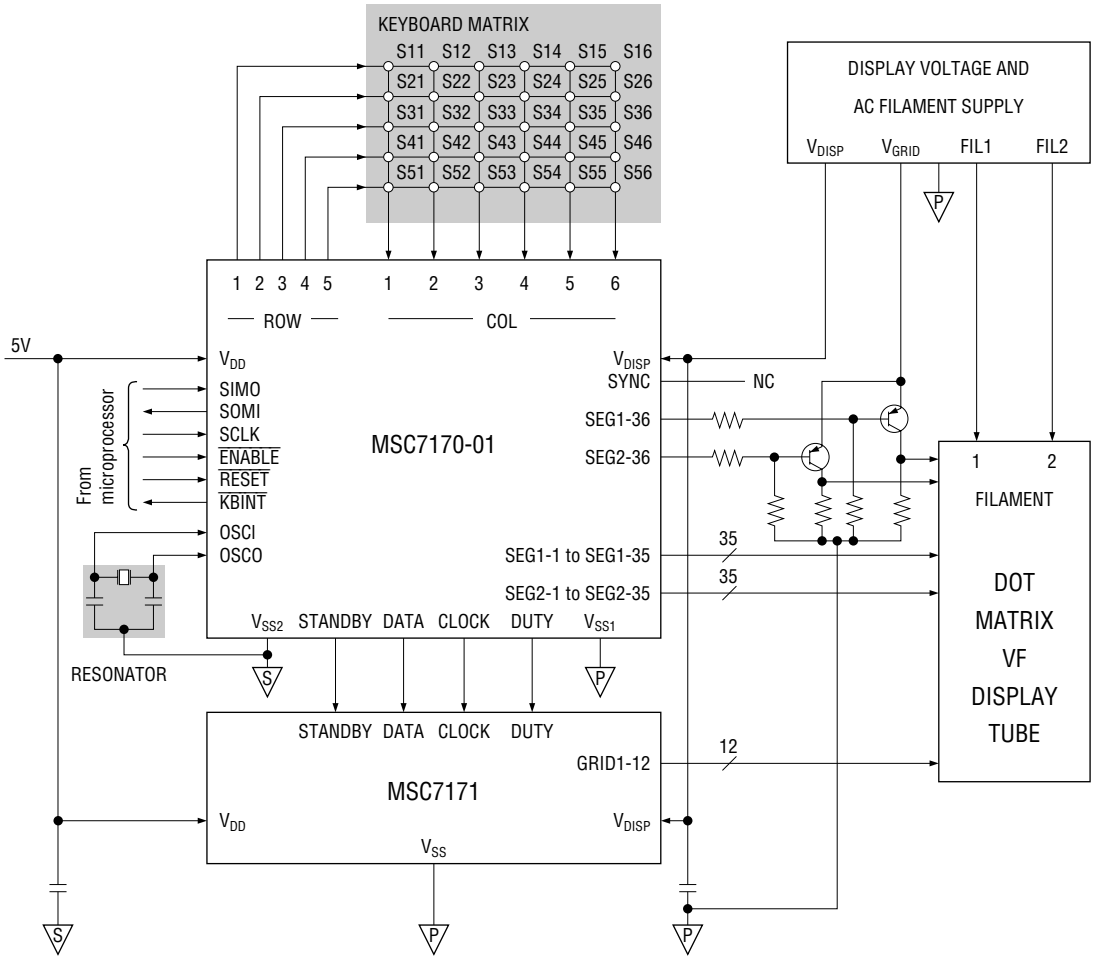
Character Codes and Character Patterns

Note: These character patterns are user programmable and can be selected by mask option.

Correspondence between Segment Outputs and VF Display Tube Dots

VF Dot: IC Pin:	1-1 SEGn-1	2-1 SEGn-2	3-1 SEGn-3	4-1 SEGn-4	5-1 SEGn-5
VF Dot: IC Pin:	1-2 SEGn-6	2-2 SEGn-7	3-2 SEGn-8	4-2 SEGn-9	5-2 SEGn-10
VF Dot: IC Pin:	1-3 SEGn-11	2-3 SEGn-12	3-3 SEGn-13	4-3 SEGn-14	5-3 SEGn-15
VF Dot: IC Pin:	1-4 SEGn-16	2-4 SEGn-17	3-4 SEGn-18	4-4 SEGn-19	5-4 SEGn-20
VF Dot: IC Pin:	1-5 SEGn-21	2-5 SEGn-22	3-5 SEGn-23	4-5 SEGn-24	5-5 SEGn-25
VF Dot: IC Pin:	1-6 SEGn-26	2-6 SEGn-27	3-6 SEGn-28	4-6 SEGn-29	5-6 SEGn-30
VF Dot: IC Pin:	1-7 SEGn-31	2-7 SEGn-32	3-7 SEGn-33	4-7 SEGn-34	5-7 SEGn-35

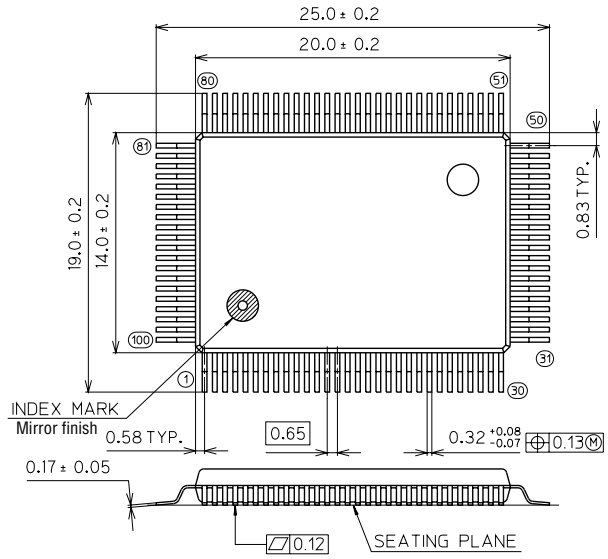
APPLICATION CIRCUIT

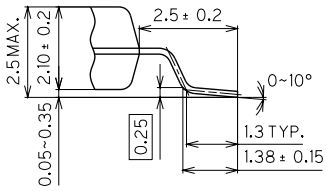


PACKAGE DIMENSIONS

(Unit : mm)

QFP100-P-1420-0.65-BK





Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.29 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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