OKI Semiconductor

This version: Sep. 2000
Previous version: Nov. 1997

MSC1215-01

17 × 2 Duplex Driver with Dimming, Keyscan and A/D Converter Function

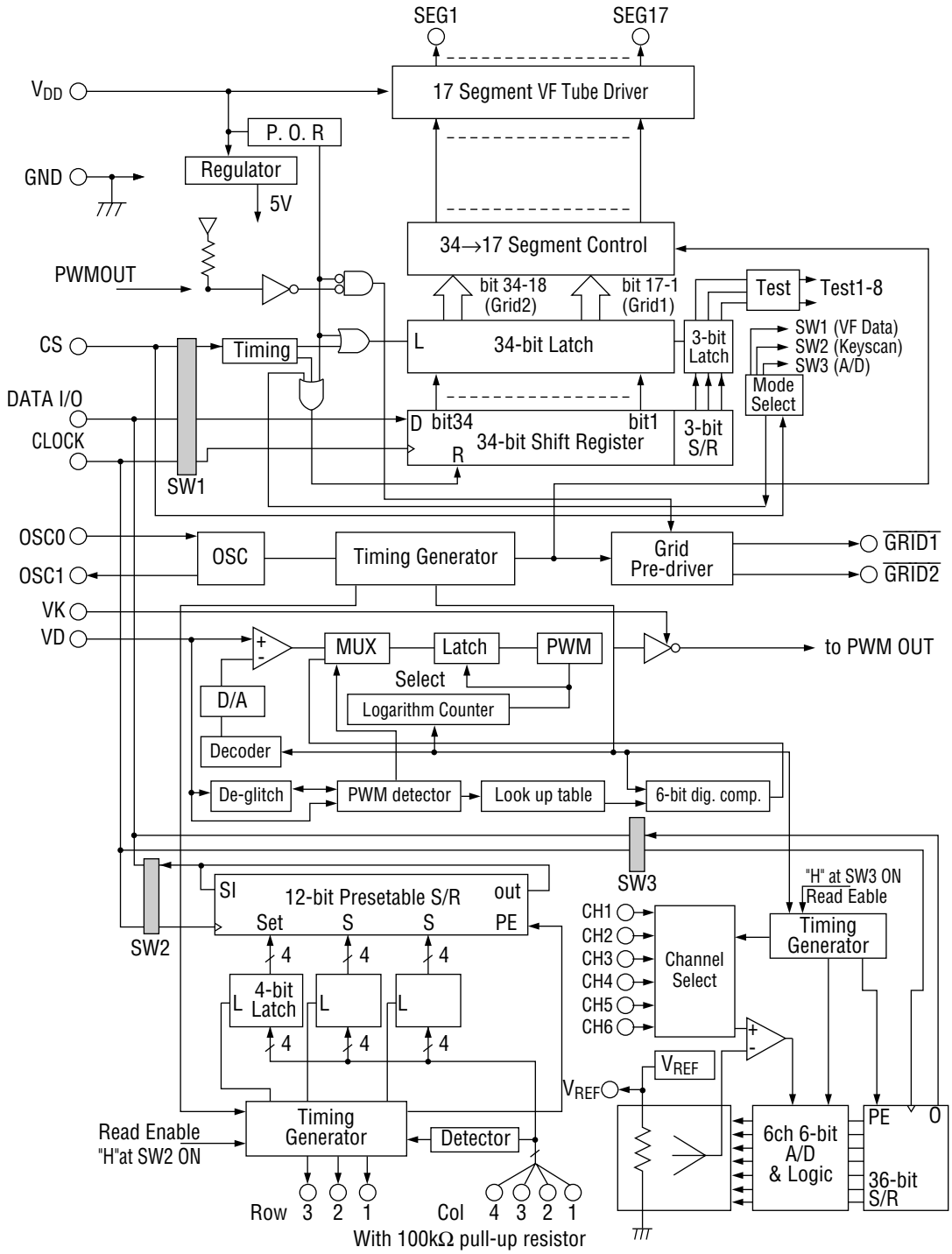
GENERAL DESCRIPTION

The MSC1215-01 is a 1/2-duty vacuum fluorescent display tube driver implemented in Bi-CMOS technology. This LSI consists of a 37-bit shift register, 34 latches, an analog dimming circuit, (a PWM conversion circuit), a 3×4 keyscan circuit, a 6ch-6-bit A/D converter and 17 segment drivers, and 2-grid pre-drivers.
The MSC1215-01 has capabilities of displaying audio system frequencies and various informations on a VFD tube for the automobile application and also interfacing with keyboard inputs and on an analog volume input.
For automobile audio systems, the front panel functions (such as a frequency display, keyboard input and analog voltage input from a volume) can be accomplished by this IC.
The analog dimming/PWM conversion modes can be selected automatically for the brightness control, so this IC is applicable to any type of automobile without any change of the specifications.
The interface with a MCU can be done only with 3 wires (CS, DATA I/O and CLOCK signals). Also, DATA I/O and CLOCK signal lines can be shared with other peripherals because of chip select function by CS signal.

FEATURES

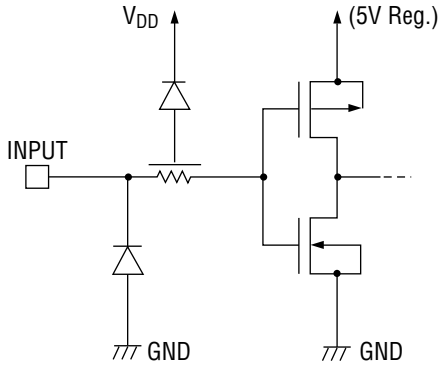
- Power supply voltage : V_{DD}=8 to 18 V
- Operating temperature range : Ta=–40 to +85°C)
- 17-segment driver outputs (I_{OH}=–5mA at V_{OH}=V_{DD}–0.8 V)
- Built-in analog dimming circuit (6-bit resolution)
- Built-in PWM conversion circuit (Lamp PWM signal to vacuum fluorescent display PWM signal)
- Built-in automatic-selection circuit for analog dimming/PWM conversion function
- Built-in 6ch 6-bit A/D converter
- Built-in 3 × 4 Keyscan circuit
- Built-in oscillation circuit (external R and C, f_{OSC}=3.3 MHz)
- Built-in Power-On-Reset circuit
- Package:
  42-pin plastic DIP (DIP 42-P-600-2.54) (Product name: MSM1215-01RS)

BLOCK DIAGRAM

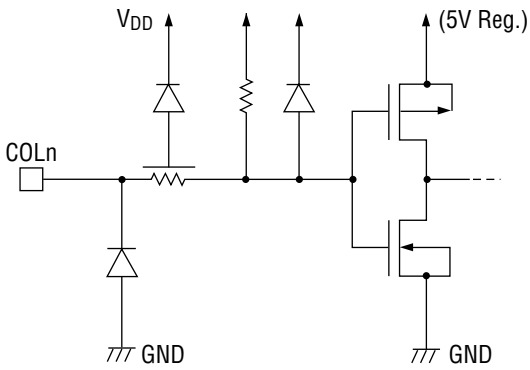


INPUT AND OUTPUT CONFIGURATION

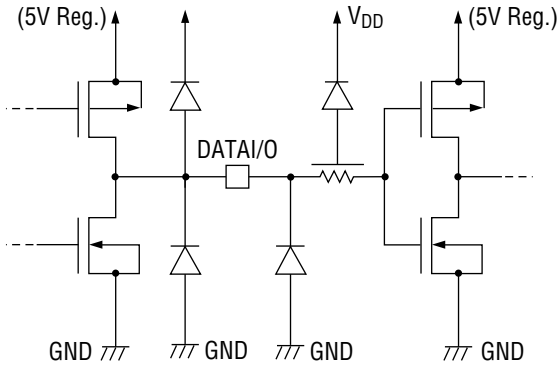
• Schematic Diagrams of Logic Portion Input Circuit 1



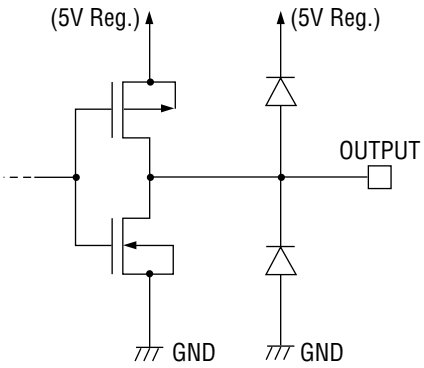
• Schematic Diagrams of Logic Portion Input Circuit 2



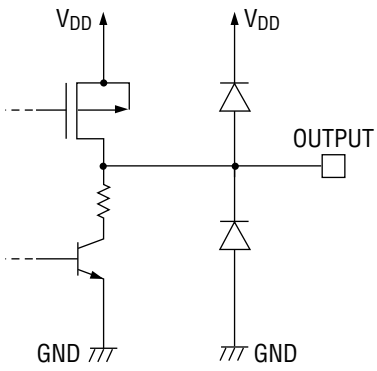
• Schematic Diagrams of Logic Portion Input/Output Circuit



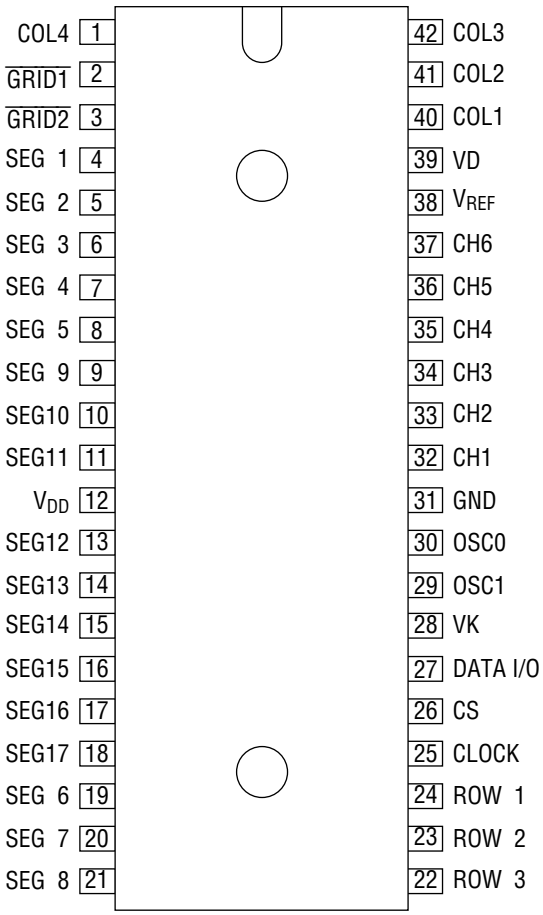
• Schematic Diagrams of Logic Portion Output Circuit



• Schematic Diagrams of Driver Output Circuit



PIN CONFIGURATION (TOP VIEW)



42-Pin Plastic DIP

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DD}	—	–0.3 to +20	V
Input Voltage (1)	V_{IN1}	All inputs except VK	–0.3 to +6	V
Input Voltage (2)	V_{IN2}	VK	–0.3 to +V_{DD}	V
Power Dissipation	P_D	Ta=85°C	400	mW
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	—	8	—	18	V
Operating Temperature	T_{OP}	—	–40	—	85	°C
High Level Input Voltage (1)	V_{IH1}	All inputs except VK	3.8	—	5.5	V
High Level Input Voltage (2)	V_{IH2}	VK	3.8	—	V_{DD}	V
Low Level Input Voltage	V_{IL}	All inputs	0	—	0.8	V
Clock Frequency	f_c	—	—	—	250	kHz
OSC Frequency	f_{osc}	R=4.7 kΩ, C=10 pF	—	3.33	—	MHz
Frame Frequency	f_{FR}	—	—	200	—	Hz

ELECTRICAL CHARACTERISTICS

DC Characteristics

(Ta=–40 to +85°C, V_{DD}=8 to 18V)

Parameter	Symbol	Condition	Min.	Max.	Unit
"H" Input Voltage	V_{IH}	All inputs except VD	3.8	—	V
"L" Input Voltage	V_{IL}	All inputs except VD	—	0.8	V
"H" Input Current (1)	I_{IH1}	All inputs except COL1-4 V_{IN}=4.4 V	–5	5	µA
"H" Input Current (2)	I_{IH2}	COL1-4, V_{IN}=3.8 V	–70	–5	µA
"L" Input Current (1)	I_{IL1}	All inputs except COL1-4 V_{IN}=0 V	–5	5	µA
"L" Input Current (2)	I_{IL2}	COL1-4, V_{IN}=0 V	–160	–10	µA
"H" Output Voltage (1)	V_{OH1}	SEG, GRID I_{OH1}=–5 mA, V_{DD}=9.5 V	V_{DD}-0.8	—	V
"H" Output Voltage (2)	V_{OH2}	DATA I/O, V_{DD}=9.5 V I_{OH2}=–200 µA Output open	 4 4.5	 — —	 V V
"L" Output Voltage (1)	V_{OL1}	SEG,GRID, V_{DD}=9.5 V I_{OL1}=500 µA I_{OL1}=200 µA I_{OL1}=2 µA	 — — —	 2 1 0.3	 V V V
"L" Output Voltage (2)	V_{OL2}	DATA I/O, ROW1-3 V_{DD}=9.5 V, I_{OL2}=200 µA	—	0.8	V
Current Consumption	I_{DD}	f_{osc}=3.3 MHz, no load	—	20	mA

Switching Characteristics

(Ta=–40 to +85°C, V_{DD}=8 to 18 V)

Parameter	Symbol	Condition	Min.	Max.	Unit
Oscillation Frequency	f_{osc}	—	2	4.5	MHz
Clock Frequency	f_c	—	—	250	kHz
Clock Pulse Width	t_{cw}	—	1.3	—	µs
Data Set-up Time	t_{DS}	—	1	—	µs
Data Hold Time	t_{DH}	—	200	—	ns
CS Pulse Width	t_{CSW}	Except reset mode	8	—	µs
CS Off Time	t_{CSL}	Except reset mode	32	—	µs
CS Pulse Width	t_{RCSW}	Reset mode	4	—	µs
CS Off Time	t_{RCSL}	Reset mode	4	—	µs
CS Set-up Time CS-clock Time	t_{CSS}	—	2	—	µs
CS Hold Time Clock-CS Time	t_{CSH}	—	2	—	µs
DATA Output Delay CLCOK-DATA Out Time	t_{PD}	—	—	1	µs
SEG & GRID Outputs Delay Time from CS	t_{ODS}	C_L=100 pF	—	8	µs
Slew Rate (All Drivers)	t_R	C_L=100 pF t=20% to 80% or 80% to 20% of V_{DD}	—	5	µs
Power on Timing	t_{PCS}	—	300	—	µs

Analog Dimming Characteristics

(Ta=–40 to +85°C, V_{DD}=8 to 18V)

Parameter	Condition	Min.	Typ.	Max.	Unit
D/A Ouput Voltage Error	—	—	—	±3	%
Reference Voltage Accuracy *1	—	—	—	±6	%

*1 Reference voltage is 6.6 V typical.

A/D Converter Characteristics

(Ta=–40 to +85°C, V_{DD}=8 to 18 V)

Parameter	Condition	Min.	Typ.	Max.	Unit
A/D Conversion Accuracy	—	—	—	±1	LSB
Reference Voltage (V_{REF})	*2	4.5	5	5.5	V
Output Current	—	—	—	4	mA
Input Voltage Range	—	GND	—	V_{REF}	V
Conversion Time/Channel	f_{OSC}=3.3MHz	384	543	896	µs

*2 When six loads of 10 kΩ are connected in parallel.

Keyscan Characteristics

(Ta=–40 to +85°C, V_{DD}=8 to 18 V)

Parameter	Condition	Min.	Typ.	Max.	Unit
Keyscan Cycle Time	f_{OSC}=3.3MHz	220	312	512	µs
Keyscan Pulse Width	f_{OSC}=3.3MHz	55	78	128	µs

PWM Conversion Characteristics

(Ta=–40 to +85°C, V_{DD}=8 to 18 V)

Parameter	Condition	Min.	Typ.	Max.	Unit
PWM Input Frequency	—	112	122	132	Hz
Rise/Fall Time	t_r=10%→90%, t_f=90%→10%	100	300	800	µs
PWM Pulse Width	t=50%→50%	125	—	—	µs
Input Duty Cycle	VD pin	1.65	—	98.3	%
"H" Input Threshold voltage	VD pin	$0.26V_{DD}$	$0.28V_{DD}$	$0.30V_{DD}$	V
"L" Input Threshold voltage	VD pin	$0.20V_{DD}$	$0.22V_{DD}$	$0.24V_{DD}$	V
Hysteresis Width	VD pin	$0.02V_{DD}$	$0.06V_{DD}$	$0.10V_{DD}$	V

TIMING DIAGRAM

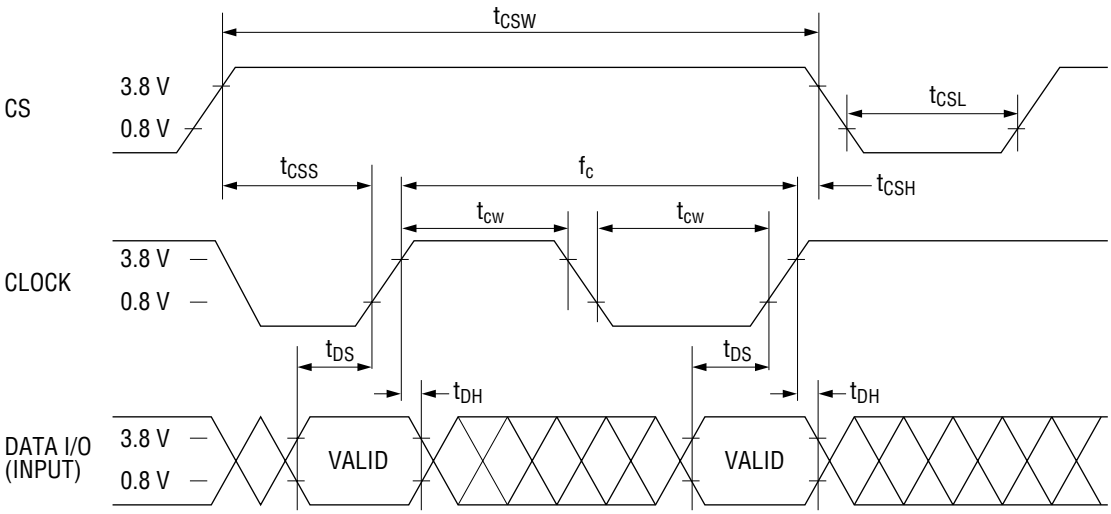


Figure 1. DATA Input Timing

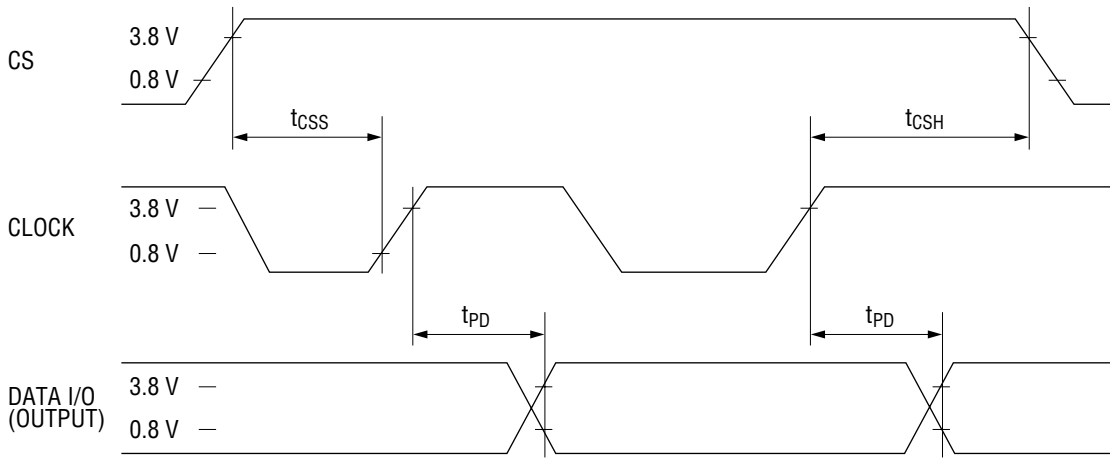


Figure 2. DATA Outpout Timing

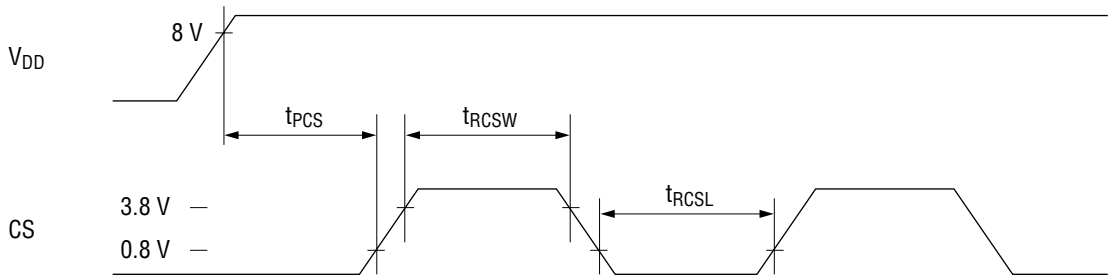


Figure 3. Power-on-Reset Timing

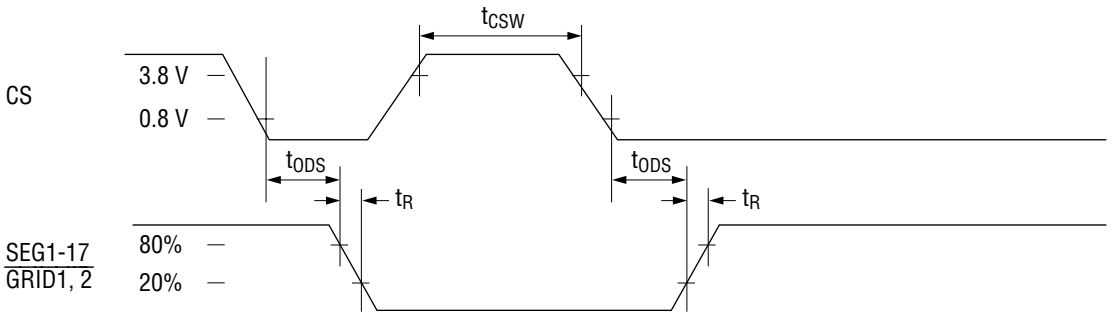


Figure 4. SEG and GRID Output Timing

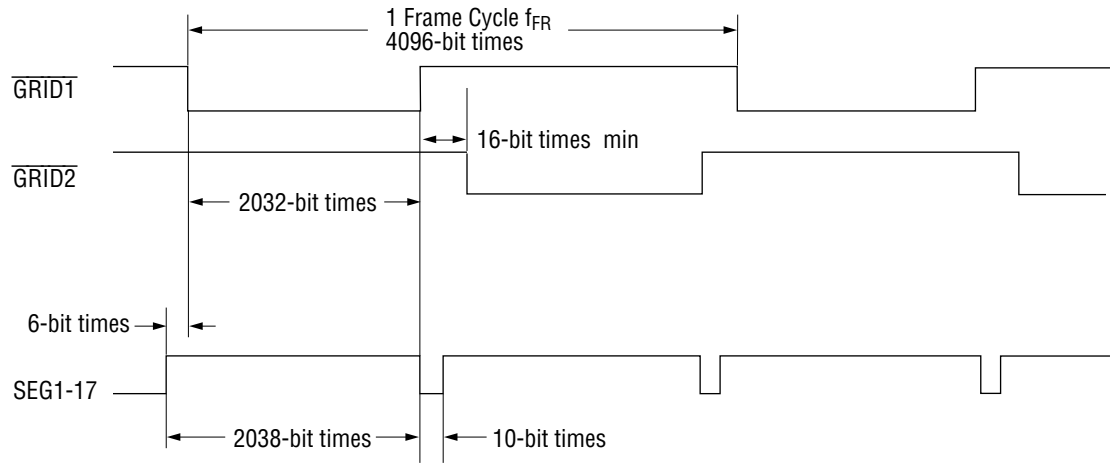


Figure 5. SEG-$\overline{GRID}$ output Timing (Daylight Mode)

Note: 1. Timing shown for analog dimming with a duty cycle of 2032/2048 at VK="L".
2. 1-bit time=T_{OSC} (=4/f_{OSC})=1.2 µs typical.

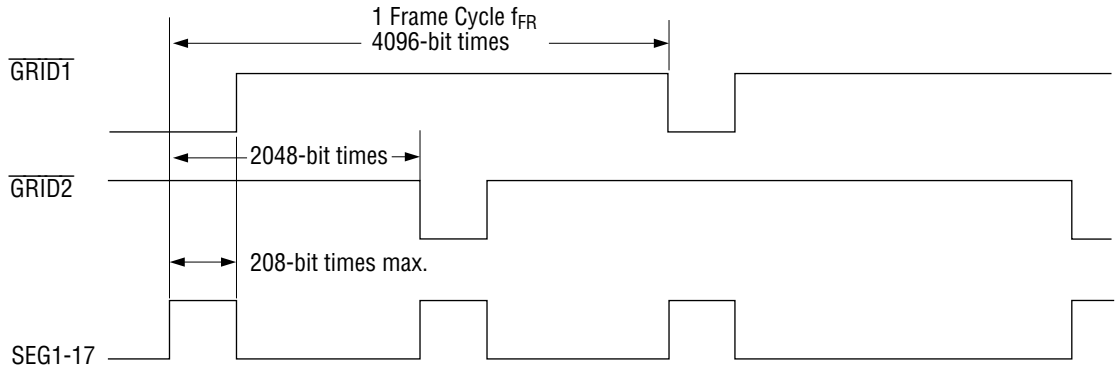


Figure 6. SEG-$\overline{\text{GRID}}$ output Timing (Dark Mode)

Note: 1. Timing shown for analog dimming with a duty cycle of 208/2048 at VK="H".
2. 1-bit time=T_{OSC} (=4/f_{OSC})=1.2 µs typical.

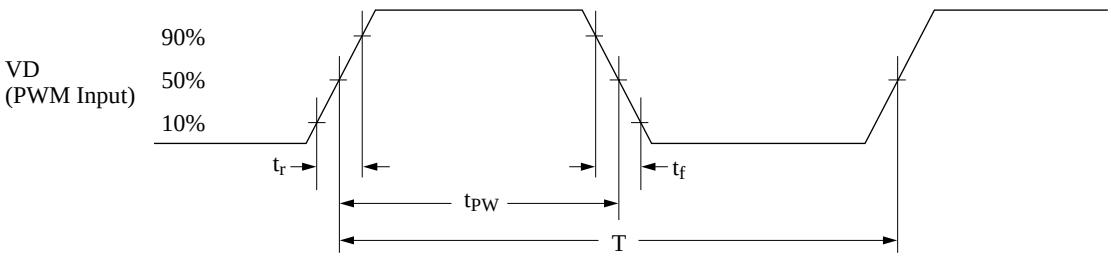


Figure 7. PWM Waveform

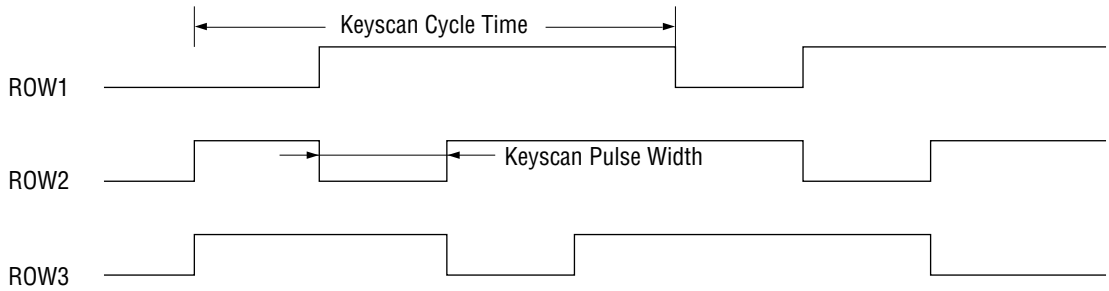


Figure 8. Keyscan Timing

Note: 1. Key scanning from ROW1 to ROW3 is started when any key is pushed down or released. Scanning will stop when CS turns to "L" from "H", after 2 times of CS pulses and the transfer of display data.

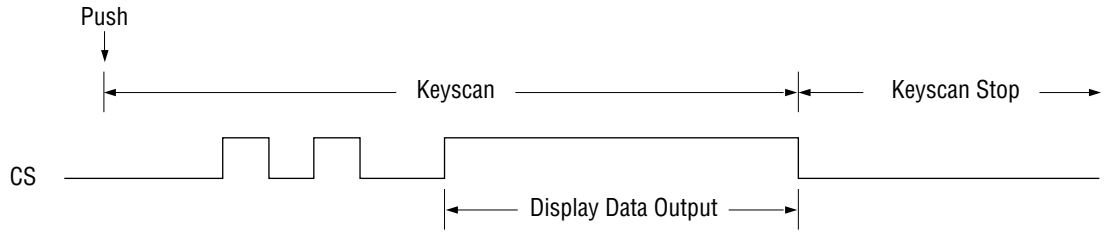


Figure 9. Keyscan Stop Timing

FUNCTIONAL DESCRIPTION

Pin Functional Description

- V_{DD}
  Power supply input pin
  Connected to a 12V power supply

- GND
  Ground Pin
  This pin is 0V level.

- CLOCK
  Serial clock input pin

- CS
  Chip select input pin
  When "H" is input to this pin, interfacing with a MCU is available through the CLOCK and the DATA pins.
  Therefore, 2 signal lines of the CLOCK and the DATA can be shared with other peripherals.

- DATA I/O (Input-output)
  Serial data input-output pin
  This pin inputs display data and outputs keyscan and A/D conversion data.

- VK
  Daylight/dark mode selection input pin
  When "H" is input, the dark mode is selected and an output duty cycle is determined by analog or PWM data input into the VD pin.
  When "L" is input, the daylight mode is selected and the output duty cycle becomes about 100%.

- VD
  Analog/PWM dimming data input pin
  Analog/PWM dimming mode selection will be done by an internal detection circuit automatically.

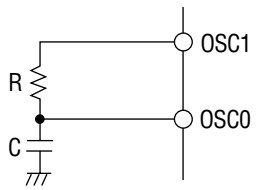
- V_{REF}
  Reference voltage output pin for the A/D converter

• CH1-6
Analog voltage input pin for the A/D converter

• COL1-4
Key matrix input pins
These pins are active "Low" and pulled up to "H" through built-in resistors except when "L" is input by a pushed down key.

• ROW1-3
Key matrix scanning output
Normally ROW1-3 output "L", by detecting the key switch to be pushed down or released, a key scan starts, sending CS pulses two times and VF data, after above turning the CS pin to "L" from "H". After scan stops, all the ROW outputs turn to "L".

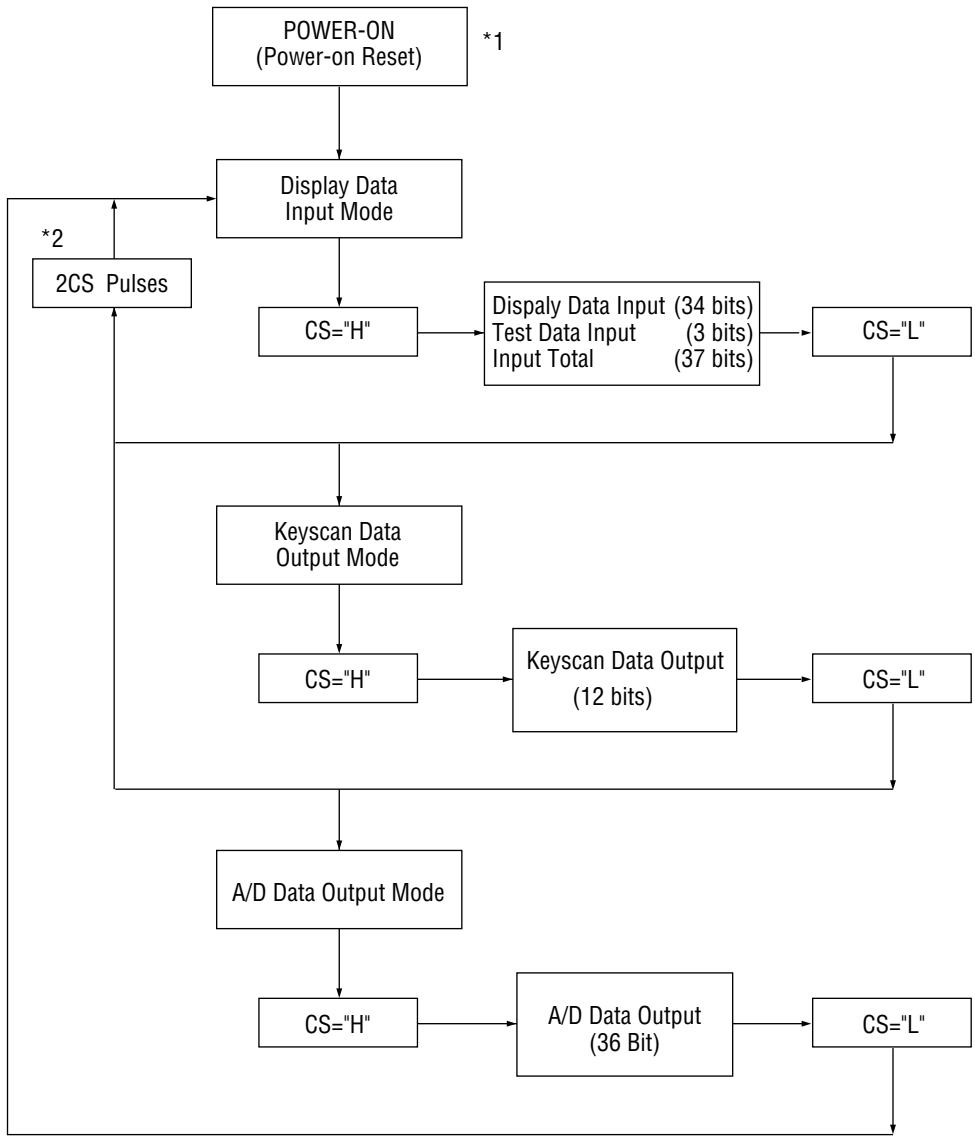
• OSC0, 1
RC oscillation input pins
A resistor and a capacitor are connected to these pins. (See figure below)



• SEG1-17
Segment output pins

• $\overline{\text{GRID1}}$, $\overline{2}$
Grid output pins
Output an inverted signal of a grid signal.
These pins are connected to inputs of external drivers (such as a PNP transistor).

Functional Flowchart



Note: 1. When power supply turns on, the internal circuits are initialized as follows by the built-in power-on reset circuit.
- Display data input mode is selected
- All segment outputs are in OFF state ("L")
- All internal registers and latches are set to "0" level

2. The status of the internal circuit after serial 2 CS pulses were applied, are as follows.
- Display data input mode is selected
- The other status are the same as before the serial 2CS pulses were applied.

Display Data Input

Data input is available only when "H" is applied to the "CS" pin. Input data is shifted into shift registers through the "DATA I/O" pin at the rising edge of the clock. The data is automatically loaded to latches at the falling edge of "CS" signal.

[Data Format]

Bit	37	36	35	----------	6	5	4	3	2	1
Data	34	33	32	----------	3	2	1	T3	T2	T1

→ First in

Display Data: 37 to 4 | Test Data: 3 to 1 (*1)

Note: Three bits (T1 to T3) for the test data are used for shipping inspection.
For the normal operation mode, all these bits should be set to "0" level.

Keyscan Data Output

Data output is available only when "H" is applied to the "CS" pin. When keyscan data output mode is selected, "DATA I/O" pin is changed to an output mode. Then, 12 bits of keyscan data come out from "DATA I/O" pin synchronizing with the rising edge of the clock. This output mode is changed to A/D data output mode at the falling edge of the CS input signal. To select directly the display input mode from this output mode, serial 2CS pulses should be input to the CS pin.

[Data Format]

Bit	12	11	10	9	8	7	6	5	4	3	2	1
Data	S34	S33	S32	S31	S24	S23	S22	S21	S14	S13	S12	S11

→ First out

*2

Note: Symbols of the keyscan data are as follows.

S_{RC}
- COL Number (COL1-4)
- ROW Number (ROW1-3)

A/D Data Output

A/D data output is available only when "H" is input to the CS pin.
When the A/D data output mode is selected, DATA I/O pin is changed to an output mode.
Then 36 bits of A/D data come out from DATA I/O pin synchronizing with the rising edge of the shift clock.
This output mode is changed to the display input mode at the falling edge of the CS input signal.

[Data Format]

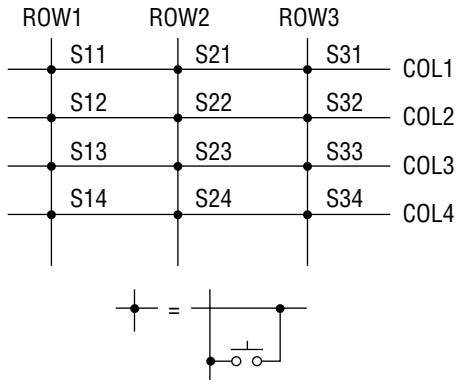
Bit	36-31	30-25	24-19	18-13	12-7	6-1
Data	MSB-LSB CH6	MSB-LSB CH5	MSB-LSB CH4	MSB-LSB CH3	MSB-LSB CH2	MSB-LSB CH1

→ First out

Keyscan

To keep a scanning noise to a minimum, a scanning of the key switch starts only when a key is pushed down or released. The scanning stops when CS input turns to "L" from "H" after sending CS pulses two times and display data.

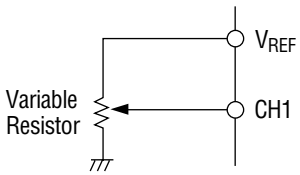
[Key Matrix of COL Input and ROW Output]



A/D Conversion

The IC has a built-in 6-ch × 6-bit A/D converter.
As shown in the circuit below, the V_{REF} output pin is connected to a variable resistor forming a voltage divider and the divided analog voltage is used to input into the CH1 to CH6 pins.

[Circuit Example]



PWM Dimming

Lamp PWM signal is input to the VD pin and converted to VF display PWM signal by the PWM conversion circuit.

Note: The duty cycle of the lamp PWM signal is measured with a reference point of the threshold voltage of the VD input pin. The threshold voltage changes due to process parameter deviation. Therefore, the PWM conversion error increases as the rise/fall time of the lamp PWM increases.

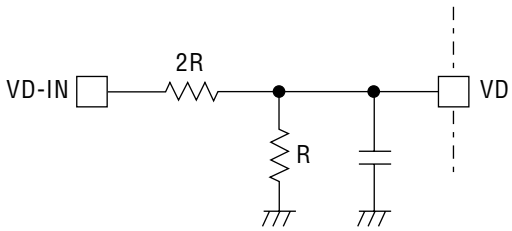
PWM Conversion Table

STEP No.	LAMP PWM DUTY CYCLE	VFD PWM DUTY CYCLE	STEP No.	LAMP PWM DUTY CYCLE	VFD PWM DUTY CYCLE
1	98.83%	8.98%	24	59.38%	2.34%
2	95.70%	8.59%	25	58.59%	2.25%
3	93.36%	8.20%	26	57.42%	2.15%
4	91.80%	7.81%	27	56.64%	2.05%
5	90.23%	7.42%	28	55.86%	1.95%
6	88.28%	7.03%	29	54.69%	1.86%
7	86.72%	6.64%	30	53.52%	1.76%
8	84.77%	6.25%	31	52.34%	1.66%
9	82.81%	5.86%	32	51.17%	1.56%
10	81.25%	5.47%	33	50.39%	1.46%
11	78.52%	5.08%	34	49.22%	1.37%
12	75.78%	4.69%	35	48.44%	1.27%
13	74.61%	4.49%	36	47.66%	1.17%
14	73.05%	4.30%	37	46.88%	1.12%
15	71.48%	4.10%	38	46.09%	1.07%
16	70.70%	3.91%	39	45.70%	1.03%
17	69.53%	3.71%	40	44.92%	0.98%
18	68.36%	3.52%	41	43.75%	0.93%
19	66.80%	3.32%	42	42.58%	0.88%
20	65.63%	3.13%	43	41.80%	0.83%
21	64.45%	2.93%	44	41.41%	0.78%
22	63.28%	2.73%	45	40.63%	0.73%
23	61.33%	2.54%	46	39.84%	0.68%
			47	39.06%	0.63%

Analog Dimming

The PWM duty cycle is controlled by analog voltage which is the output of the brightness control volume on a dashboard.

The input voltage to "VD" needs to use a voltage divider as shown below.



Note: The maximum voltage to the VD is 5 V.

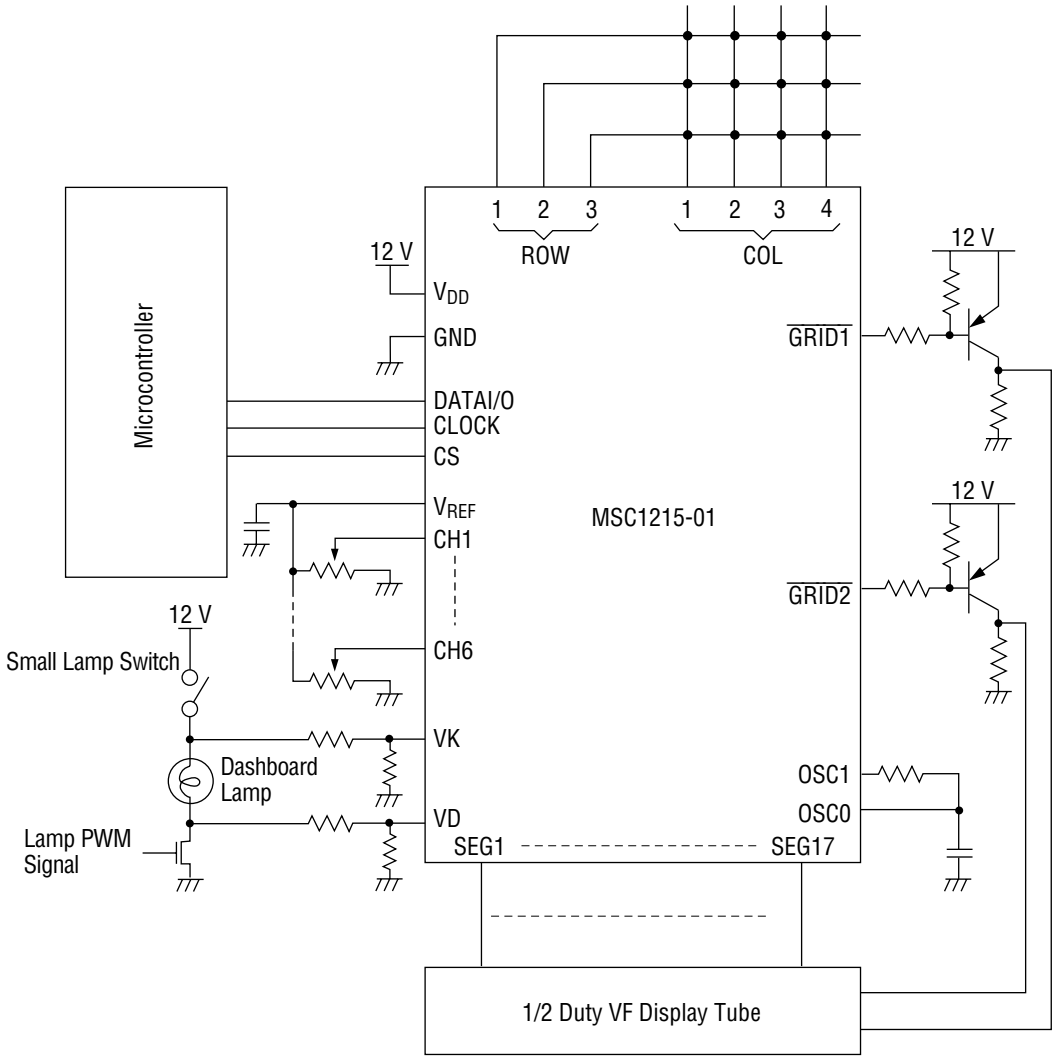
Dimming Voltage-Pulse width Correspondence Table

(@V_{DD}=2.8 V)

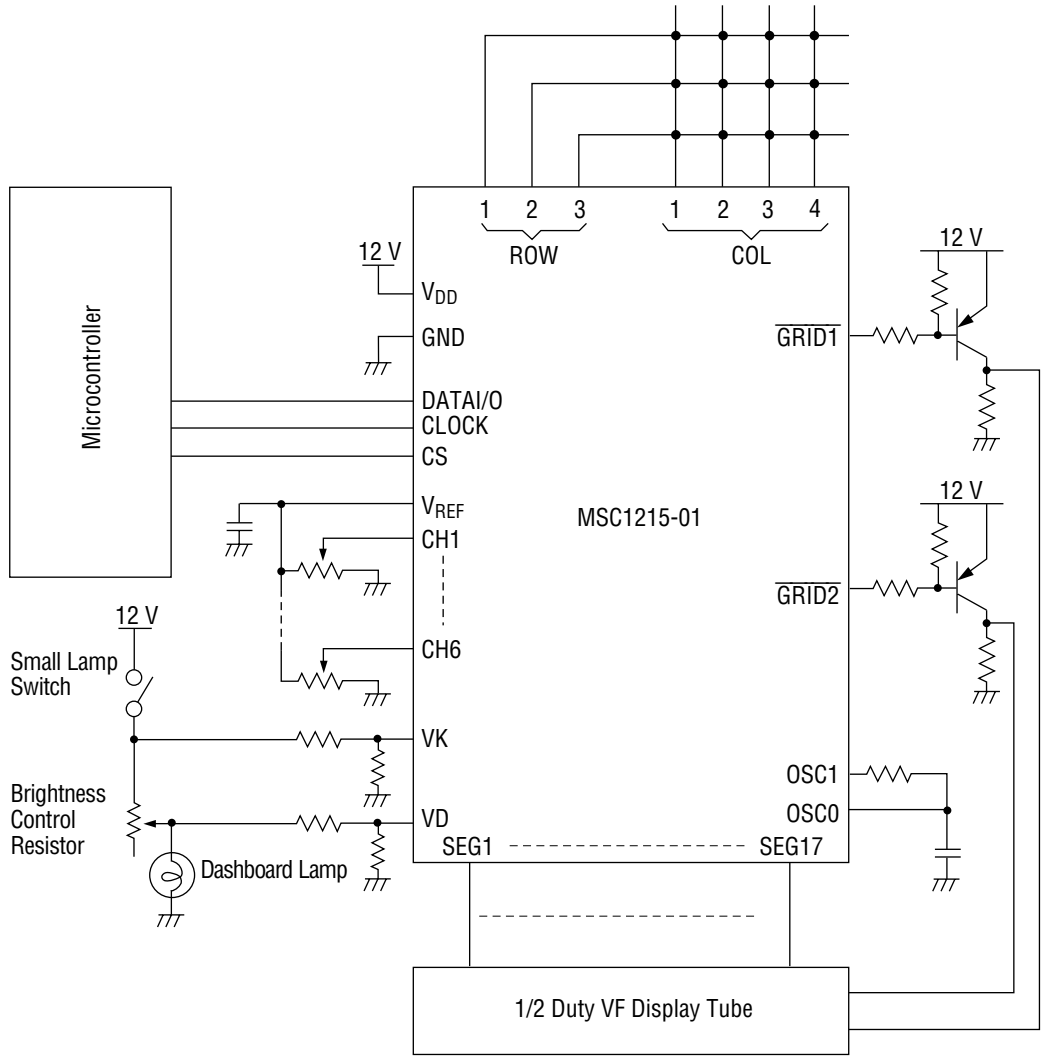
Pulse Step Number	PWM Duty Cycle		Threshold Voltage	Pulse Step Number	PWM Duty Cycle		Threshold Voltage
	Pulse Count	%			Pulse Count	%	
52	—	—	V_{REF}	26	56/2048	2.73	3.385
51	—	—	V_{REF}	25	52/2048	2.54	3.323
50	—	—	V_{REF}	24	48/2048	2.34	3.263
49	208/2048	10.2	V_{REF}	23	46/2048	2.25	3.204
48	192/2048	9.38	4.621	22	44/2048	2.15	3.155
47	184/2048	8.98	4.541	21	42/2048	2.05	3.118
46	176/2048	8.59	4.488	20	40/2048	1.95	3.076
45	168/2048	8.20	4.434	19	38/2048	1.86	3.027
44	160/2048	7.81	4.381	18	36/2048	1.76	2.983
43	152/2048	7.42	4.333	17	34/2048	1.66	2.941
42	144/2048	7.03	4.286	16	32/2048	1.56	2.898
41	136/2048	6.64	4.231	15	30/2048	1.46	2.860
40	128/2048	6.25	4.170	14	28/2048	1.37	2.822
39	120/2048	5.86	4.106	13	26/2048	1.27	2.785
38	112/2048	5.47	4.043	12	24/2048	1.17	2.744
37	104/2048	5.08	3.980	11	23/2048	1.12	2.692
36	96/2048	4.69	3.914	10	22/2048	1.07	2.650
35	92/2048	4.49	3.831	9	21/2048	1.03	2.622
34	88/2048	4.30	3.766	8	20/2048	0.98	2.597
33	84/2048	4.10	3.716	7	19/2048	0.93	2.569
32	80/2048	3.91	3.673	6	18/2048	0.88	2.539
31	76/2048	3.71	3.631	5	17/2048	0.83	2.511
30	72/2048	3.52	3.594	4	16/2048	0.78	2.478
29	68/2048	3.32	3.551	3	15/2048	0.73	2.455
28	64/2048	3.13	3.501	2	14/2048	0.68	2.425
27	60/2048	2.93	3.444	1	13/2048	0.63	2.392
			3.385				0.000

APPLICATION CIRCUITS

PWM Dimming Mode



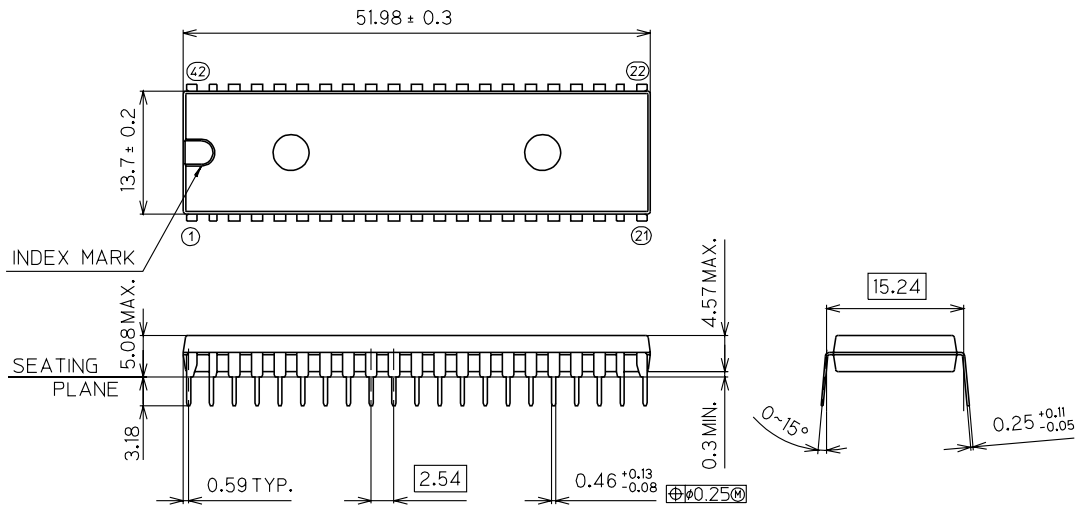
Analog Dimming Mode



PACKAGE DIMENSIONS

(Unit : mm)

DIP42-P-600-2.54



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5 μm)
Package weight (g)	6.20 TYP.
Rev. No./Last Revised	2/Dec. 11, 1996

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Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

4. Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.

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