OKI Semiconductor

MR27V3252D

2,097,152-Word x 16-Bit or 4,194,304-Word x 8-Bit

8-Word x 16-Bit or 16-Word x 8-Bit Page Mode
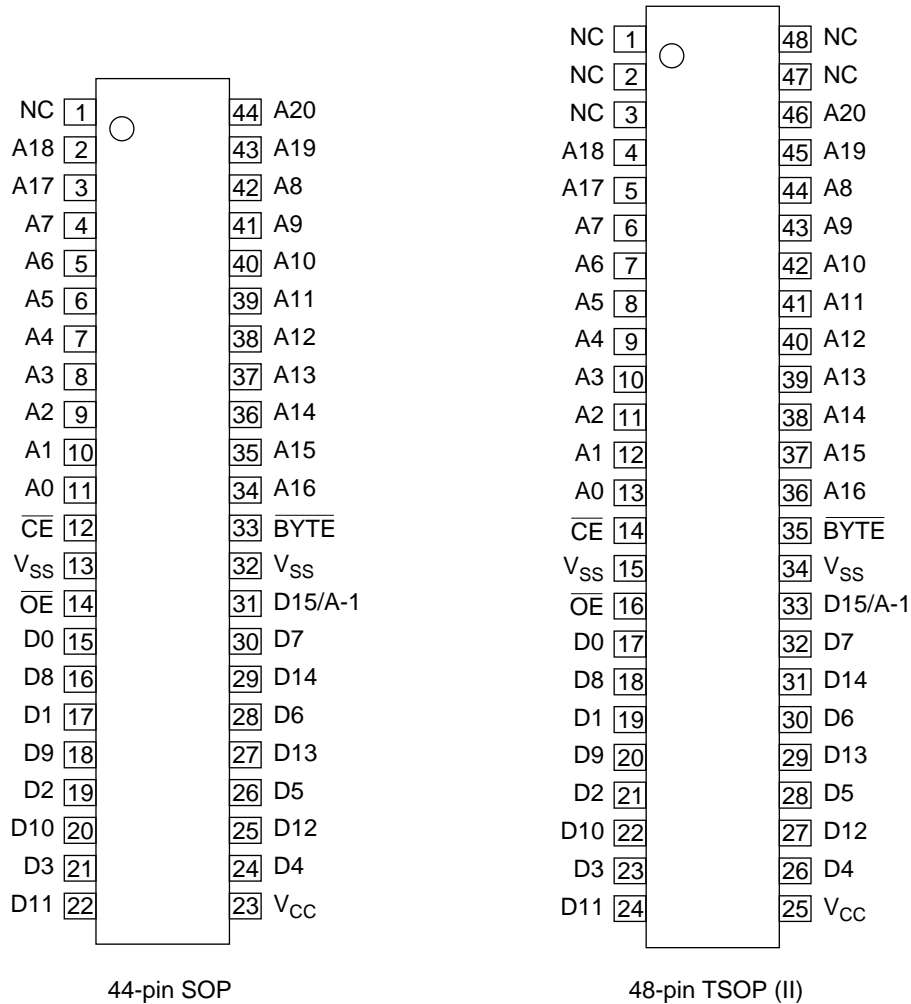
Production Programmed Read Only Memory (P2ROM)

DESCRIPTION

The MR27V3252D is a 32Mbit Production Programmed Read-Only Memory (P2ROM) with page mode. Its configuration can be electrically switched between 2,097,152 word x 16bit and 4,194,304 word x 8bit. The MR27V3252D operates on a single +3.3V power supply and is TTL compatible. The MR27V3252D provides Page mode which can greatly reduce the read access time. Since the MR27 V3252D operates asynchronously , external clocks are not required , making this device easy-to-use. The MR27V3252D is suitable as large-capacity fixed memory for microcomputers and data terminals. It is manufactured using a CMOS double silicon gate technology and is offered in 44-pin SOP or 48-pin TSOP packages.

FEATURES
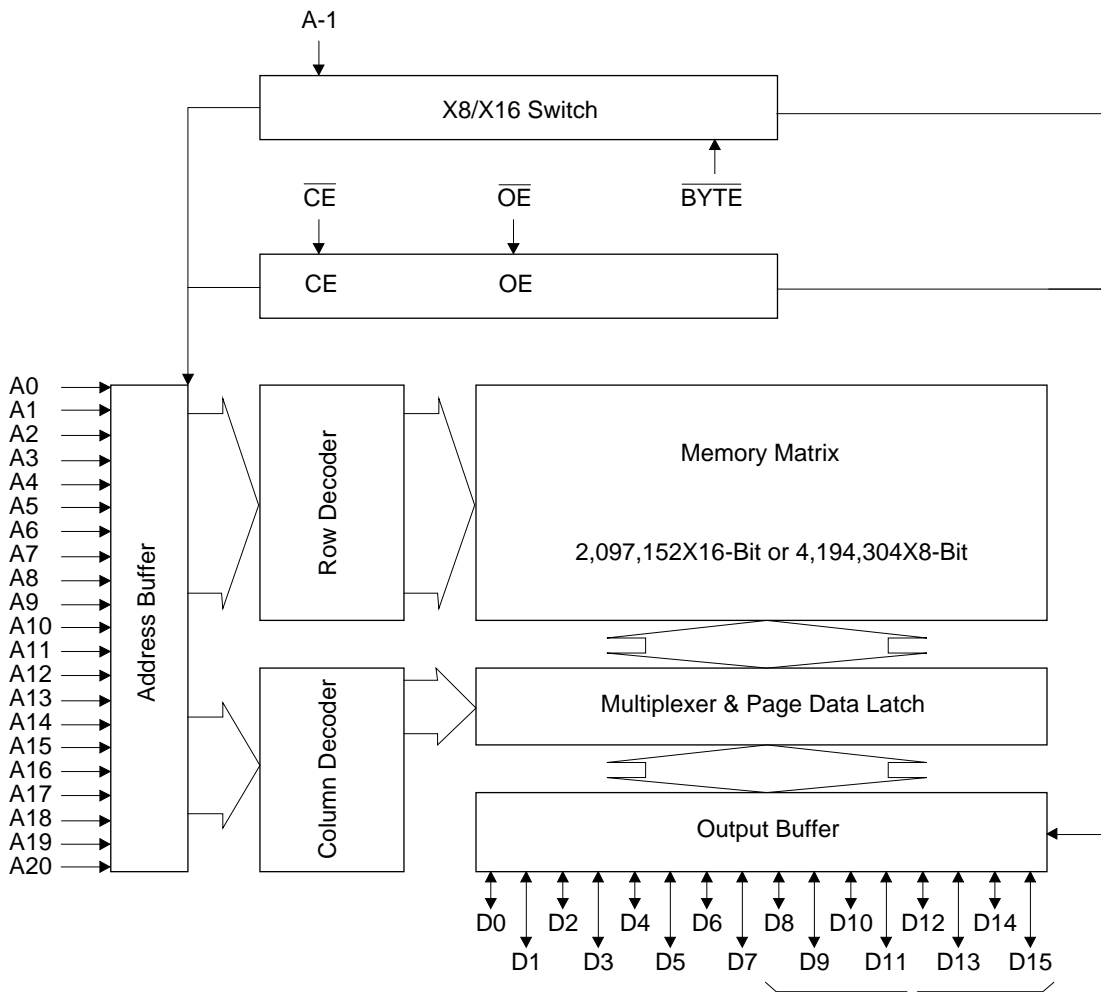
- 2,097,152 word x 16bit / 4,194,304 word x 8bit electrically switchable configuration
- Single +3.3V power supply
- Access time 100ns
  Page mode access time 30ns
- Input / Output TTL compatible
- Three-state output
- Packages
  - 44-pin plastic SOP (SOP44-P-600-1.27-K)   (Product name : MR27V3252D-xxMA)
  - 48-pin plastic TSOP (TSOP II 48-P-550-0.80-K) (Product name : MR27V3252D-xxTA)

PIN CONFIGURATION (TOP VIEW)

44-pin SOP

Left	Pin		Pin	Right
NC	1		44	A20
A18	2		43	A19
A17	3		42	A8
A7	4		41	A9
A6	5		40	A10
A5	6		39	A11
A4	7		38	A12
A3	8		37	A13
A2	9		36	A14
A1	10		35	A15
A0	11		34	A16
$\overline{CE}$	12		33	$\overline{BYTE}$
V_{SS}	13		32	V_{SS}
$\overline{OE}$	14		31	D15/A-1
D0	15		30	D7
D8	16		29	D14
D1	17		28	D6
D9	18		27	D13
D2	19		26	D5
D10	20		25	D12
D3	21		24	D4
D11	22		23	V_{CC}

44-pin SOP

48-pin TSOP (II)

Left	Pin		Pin	Right
NC	1		48	NC
NC	2		47	NC
NC	3		46	A20
A18	4		45	A19
A17	5		44	A8
A7	6		43	A9
A6	7		42	A10
A5	8		41	A11
A4	9		40	A12
A3	10		39	A13
A2	11		38	A14
A1	12		37	A15
A0	13		36	A16
$\overline{CE}$	14		35	$\overline{BYTE}$
V_{SS}	15		34	V_{SS}
$\overline{OE}$	16		33	D15/A-1
D0	17		32	D7
D8	18		31	D14
D1	19		30	D6
D9	20		29	D13
D2	21		28	D5
D10	22		27	D12
D3	23		26	D4
D11	24		25	V_{CC}

48-pin TSOP (II)

PIN NAMES	FUNCTIONS
D15/A-1	Data output / Address input
A0 - A20	Address input
D0 - D14	Data output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
V_{CC}	Power supply voltage
V_{SS}	GND
$\overline{BYTE}$	Mode switch
NC	Non connection

BLOCK DIAGRAM

In 8-bit output mode, these pins are three-stated and pin D15 functions as the A-1 address pin.

FUNCTION TABLE

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$	V_{CC}	D0 - D7	D8 - D14	D15/A-1
READ (16-Bit)	L	L	H		D_{OUT}		
READ (8-Bit)	L	L	L		D_{OUT}	Hi-Z	L/H
OUTPUT DISABLE	L	H	H	3.3V		Hi-Z	
			L				*
STAND-BY	H	*	H			Hi-Z	
			L				*

* : Don't Care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Value	Unit
Operating temperature under bias	T_{opr}	-	0 to 70	°C
Storage temperature	T_{stg}		-55 to 125	°C
Input voltage	V_I		-0.5 to V_{CC} + 0.5	V
Output voltage	V_O	relative to V_{SS}	-0.5 to V_{CC} + 0.5	V
Power supply voltage	V_{CC}		-0.5 to 5	V
Power dissipation per package	P_D	-	1.0	W

RECOMMENDED OPERATING CONDITIONS FOR READ

(Ta=0 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
V_{CC} power supply voltage	V_{CC}		3.0	-	3.6	V
Input "H" level	V_{IH}	V_{CC}=3.0V-3.6V	2.2	-	V_{CC}+0.5*	V
Input "L" level	V_{IL}		-0.5**	-	0.6	V

Voltage is relative to Vss

* : Vcc+1.5V (Max.) when pulse width of overshoot is less than 10nS.

** : -1.5V (Min.) when pulse width of undershoot is less than 10nS.

ELECTRICAL CHARACTERISTICS (Read operation)

DC Characteristics

(V_{CC}=3.3V±0.3V, Ta=0 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input leakage current	I_{LI}	V_I=0 to Vcc	-	-	10	μA
Output leakage current	I_{LO}	V_O=0 to Vcc	-	-	10	μA
V_{CC} power supply current (Standby)	I_{CS1}	$\overline{CE}$=V_{CC}	-	-	50	μA
	I_{CS2}	$\overline{CE}$=V_{IH}	-	-	1	mA
V_{CC} power supply current (Read)	I_{CCA}	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH} tc=100ns	-	-	100	mA
Input "H" level	V_{IH}	-	2.2	-	V_{CC}+0.5*	V
Input "L" level	V_{IL}	-	-0.5**	-	0.6	V
Output "H" level	V_{OH}	I_{OH}=-400μA	2.4	-	-	V
Output "L" level	V_{OL}	I_{OL}=2.1mA	-		0.4	V

Voltage is relative to Vss

* : Vcc+1.5V (Max.) when pulse width of overshoot is less than 10nS.

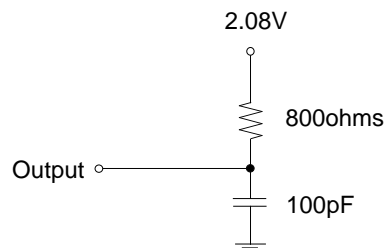** : -1.5V (Min.) when pulse width of undershoot is less than 10nS.

AC Characteristics

(V_{CC}=3.3V±0.3V, Ta=0 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Address access cycle time	T_C	-	100	-	ns
Address access time	T_{ACC}	$\overline{CE}$=$\overline{OE}$=V_{IL}	-	100	ns
Page access cycle time	T_{PC}	-	30	-	ns
Page access time	T_{PAC}	-	-	30	ns
$\overline{CE}$ access time	T_{CE}	$\overline{OE}$=V_{IL}	-	100	ns
$\overline{OE}$ access time	T_{OE}	$\overline{CE}$=V_{IL}	-	40	ns
Output disable time	T_{CHZ}	$\overline{OE}$=V_{IL}	0	30	ns
	T_{OHZ}	$\overline{CE}$=V_{IL}	0	25	ns
Output hold time	T_{OH}	$\overline{CE}$=$\overline{OE}$=V_{IL}	0	-	ns

Measurement conditions
Input signal level ------------------- 0V/3V
Input timing reference level ----------- 0.8V/2.0V
Output load ------------------------- 100pF
Output timing reference level ----------- 0.8V/2.0V
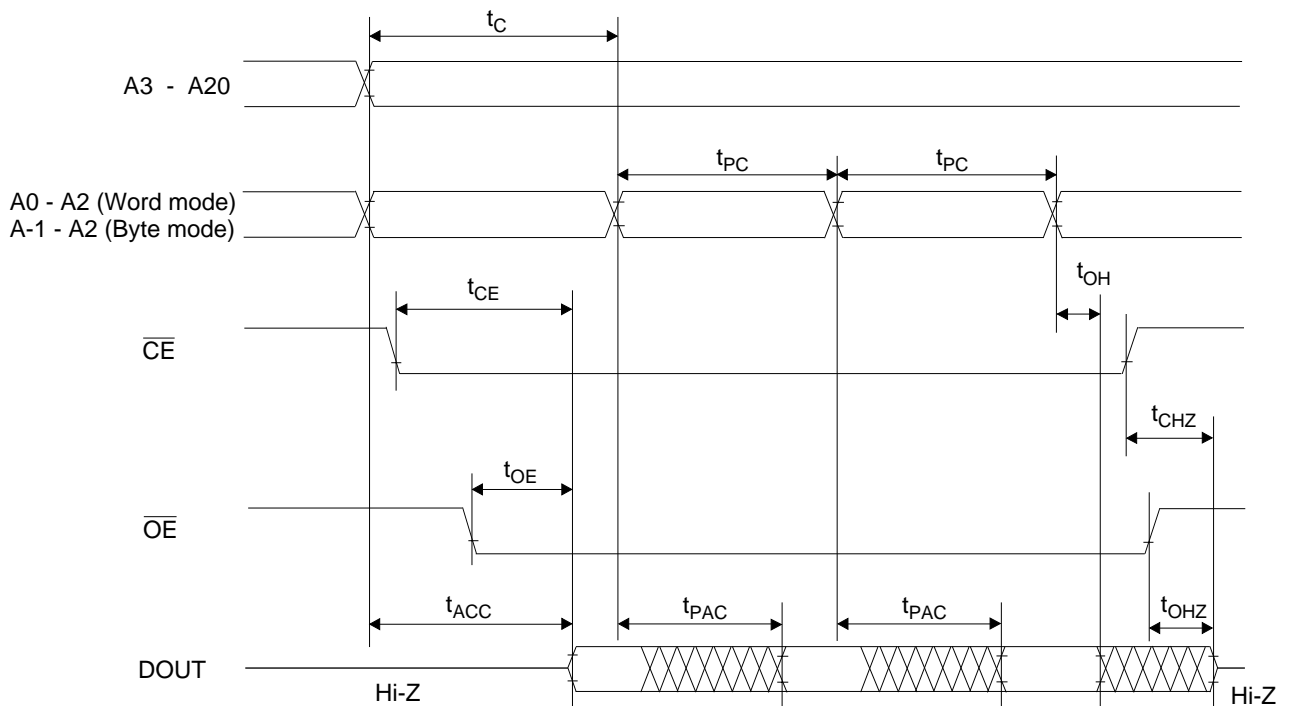
2.08V

800ohms

Output

100pF

TIMING CHART

NORMAL MODE READ CYCLE

PAGE MODE READ CYCLE

PIN Capacitance

$(V_{CC}=3.3V, Ta=25°C, f=1MHz)$

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input	C_{IN1}	$V_I=0V$	-	-	8	pF
$\overline{BYTE}$	C_{IN2}		-	-	120	
Output	C_{OUT}	$V_O=0V$	-	-	10	