Preliminary

OKI Semiconductor

This version: Dec. 1999
Previous version: Jun. 1999

ML9050/9051

132-Channel LCD Driver with Built-in RAM for LCD Dot Matrix Displays

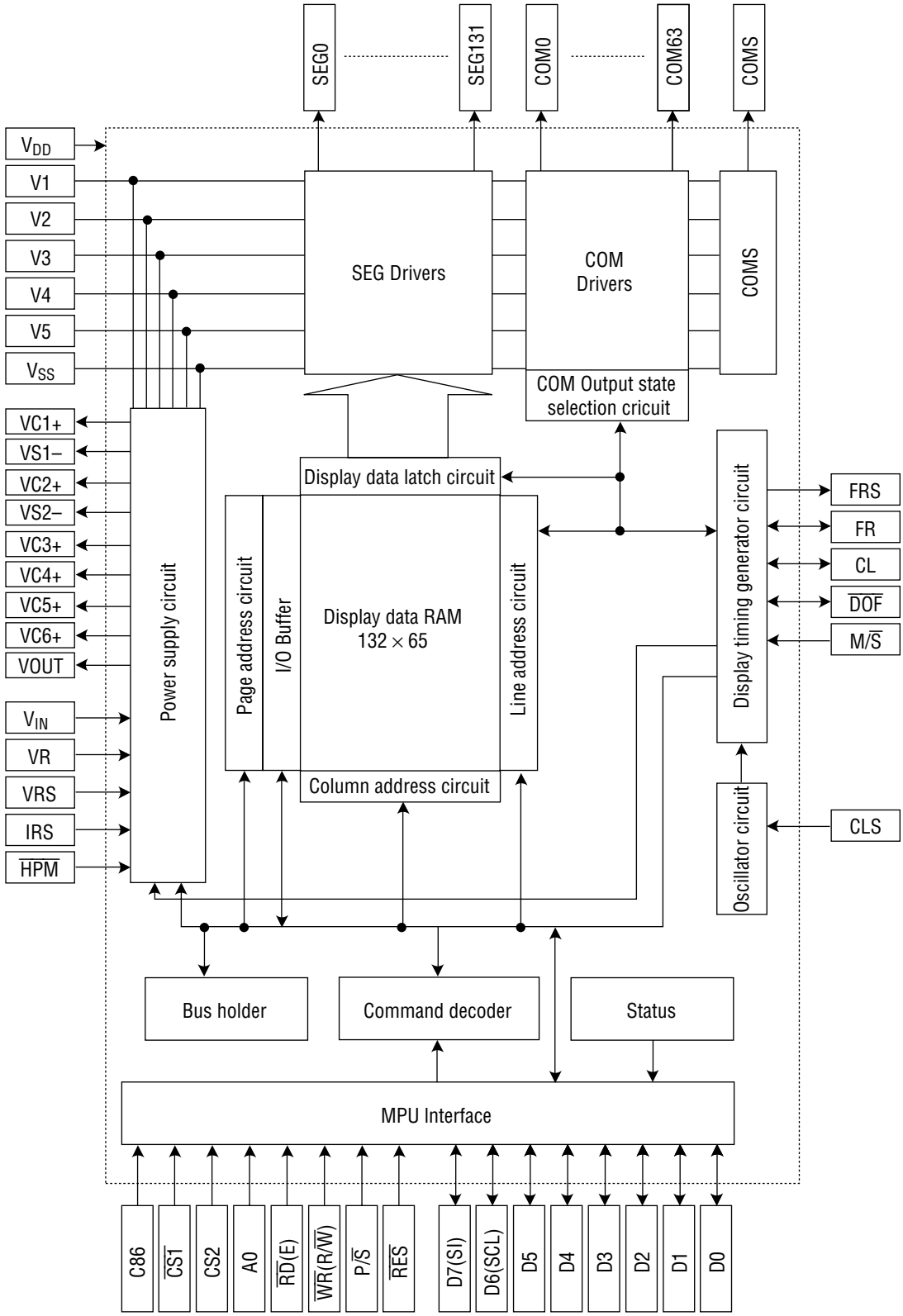
GENERAL DESCRIPTION

The ML9050/9051 is an LSI for dot matrix graphic LCD devices carrying out bit map display. This LSI can drive a dot matrix graphic LCD display panel under the control of an 8-bit microcomputer. Since all the functions necessary for driving a bit map type LCD device are incorporated in a single chip, using the ML9050/9051 makes it possible to realize a bit map type dot matrix graphic LCD display system with only a few chips.
Since the bit map method in which one bit of display RAM data turns ON or OFF one dot in the display panel, it is possible to carry out displays with a high degree of freedom such as Chinese character displays, etc. With one chip, it is possible to construct a graphic display system with a maximum of 132 × 65 dots. The display can be expanded further using two chips.
The ML9050/9051 is made using a CMOS process. Because it has a built-in RAM, low power consumption is one of its features, and is therefore suitable for displays in battery-operated portable equipment.
The ML9050 has 65 common signal outputs and 132 segment signal outputs and one chip can drive a display of up to 65 × 132 dots.
The ML9051 has 49 common signal outputs and 132 segment signal outputs and one chip can drive a display of up to 49 × 132 dots.
This device is not resistant to radiation or to light.

FEATURES

- Direct display of the RAM data using the bit map method
  Display RAM data "1" ... Dot is displayed
  Display RAM data "0" ... Dot is not displayed
- Display RAM capacity
  ML9050/9051: 65 × 132 = 8580 dots
- LCD Drive circuits
  ML9050: 65 common outputs, 132 segment outputs
  ML9051: 49 common outputs, 132 segment outputs
- Microcomputer interface: Can select an 8-Bit parallel or serial interface
- Built-in voltage multiplier circuit for the LCD drive power supply
- Built-in LCD drive power supply adjustment circuit
- Built-in LCD drive bias resistors
- Line reversal drive/frame reversal drive (selected by a command)
- Built-in oscillator circuit (Internal RC oscillator/external clock input)
- A variety of commands
  Read/write of display data, display ON/OFF, normal/reverse display, all dots ON/all dots OFF, set page address, set display start address, etc.
- Power supply voltage
  Logic power supply: V_{DD}-V_{SS} = 1.8 V to 5.5 V
  Voltage multiplier reference voltage: V_{IN}-V_{SS} = 1.8 V to V_{DD}
  (5-Times multiplier → 1.8 V to 3.6 V, 6-times multiplier → 1.8 to 3 V, 7-times multiplier → 1.8 to 2.5 V)
  LCD Drive voltage: V_{BI}-V_{SS} = 6.0 to 18 V
- Package: Gold bump chip, TCP

BLOCK DIAGRAM



PIN DESCRIPTION

Function	Pin name	Number of pins	I/O	Description
MPU Interface	D0 to D7	8	I/O	This is an 8-bit bi-directional data bus that can be connected to an 8-bit or 16-bit standard MPU data bus. When a serial interface is selected (P/$\overline{S}$ = "L"): D7: Serial data input pin (SI) D6: Serial clock input pin (SCL) In this case, D0 to D5 will be in the Hi-Z state. D0 to D7 will all be in the Hi-Z state when the chip select is in the inactive state.
	A0	1	I	Normally, the lowest bit of the MPU address bus is connected and used for distinguishing between data and commands. A0 = "H": Indicates that D0 to D7 is display data. A1 = "L": Indicates that D0 to D7 is control data.
	$\overline{RES}$	1	I	Initial setting is made by making $\overline{RES}$ = "L". The reset operation is made during the active level of the RES signal.
	$\overline{CS1}$ CS2	2	I	These are the chip select signals. The Chip Select of the LSI becomes active when $\overline{CS1}$ is "L" and also CS2 is "H" and allows the input/output of data or commands.
	$\overline{RD}$ (E)	1	I	The active level of this signal is "L" when connected to an 80-series MPU. This terminal is connected to the $\overline{RD}$ signal of the 80-series MPU, and the data bus of the ML9050/9051 goes into the output state when this signal is "L". The active level of this signal is "H" when connected to a 68-series MPU. This pin will be the Enable and clock input pin when connected to a 68-series MPU.
	$\overline{WR}$ (R/$\overline{W}$)	1	I	The active level of this signal is "L" when connected to an 80-series MPU. This terminal is connected to the $\overline{WR}$ signal of the 80-series MPU. The data on the data bus is latched into the ML9052 at the rising edge of the $\overline{WR}$ signal. When connected to a 68-series MPU, this pin becomes the input pin for the Read/Write control signal. R/$\overline{W}$ = "H": Read, R/$\overline{W}$ = "L": Write
	C86	1	I	This is the pin for selecting the MPU interface type. C86 = "H": 68-Series MPU interface. C86 = "L": 80-Series MPU interface.

<table>
<tr><th>Function</th><th>Pin name</th><th>Number of pins</th><th>I/O</th><th>Description</th></tr>
<tr><td>MPU Interface</td><td>P/$\overline{S}$</td><td>1</td><td>I</td><td>This is the pin for selecting parallel data input or serial data input.
P/$\overline{S}$ = "H": Parallel data input.
P/$\overline{S}$ = "L": Serial data input.
The pins of the LSI have the following functions depending on the state of P/$\overline{S}$ input.
<table><tr><th>P/$\overline{S}$</th><th>Data/command</th><th>Data</th><th>Read/Write</th><th>Serial clock</th></tr><tr><td>"H"</td><td>A0</td><td>D0 to D7</td><td>$\overline{RD}$, $\overline{WR}$</td><td rowspan="2">SCL (D6)</td></tr><tr><td>"L"</td><td>A0</td><td>SI (D7)</td><td>Write only</td></tr></table>
When P/$\overline{S}$ is "L", D0 to D5 will go into the Hi-Z state. In this condition, the data on the lines D0 to D5 can be "H", "L", or open. The pins $\overline{RD}$ (E) and $\overline{WR}$ (R/$\overline{W}$) should be tied to either the "H" level or the "L" level.
During serial data input, it is not possible to read the display data in the RAM.</td></tr>
<tr><td>Oscillator circuit</td><td>CLS</td><td>1</td><td>I</td><td>This is the pin for selecting whether to enable or disable the internal oscillator circuit for the display clock.
CLS = "H": The internal oscillator circuit is enabled.
CLS = "L": The internal oscillator circuit is disabled (External input).
When CLS = "L", the display clock is input at the pin CL.</td></tr>
<tr><td>Display timing generator circuit</td><td>M/$\overline{S}$</td><td>1</td><td>I</td><td>This is the pin for selecting whether master operation or slave operation is made towards the ML9050/9051. During master operation, the synchronization with the LCD display system is achieved by inputting the timing signals necessary for LCD display.
M/$\overline{S}$ = "H": Master operation
M/$\overline{S}$ = "L": Slave operation
The functions of the different circuits and pins will be as follows depending on the states of M/$\overline{S}$ and CLS signals.
<table><tr><th>M/$\overline{S}$</th><th>CLS</th><th>Oscillator circuit</th><th>Power supply circuit</th><th>CL</th><th>FR</th><th>FRS</th><th>$\overline{DOF}$</th></tr><tr><td>"H"</td><td>"H"</td><td>Enabled</td><td>Enabled</td><td>Output</td><td>Output</td><td>Output</td><td>Output</td></tr><tr><td></td><td>"L"</td><td>Disabled</td><td>Enabled</td><td>Input</td><td>Output</td><td>Output</td><td>Output</td></tr><tr><td>"L"</td><td>"H"</td><td>Disabled</td><td>Disabled</td><td>Input</td><td>Input</td><td>Output</td><td>Input</td></tr><tr><td></td><td>"L"</td><td>Disabled</td><td>Disabled</td><td>Input</td><td>Input</td><td>Output</td><td>Input</td></tr></table></td></tr>
</table>

<table>
<tr><th>Function</th><th>Pin name</th><th>Number of pins</th><th>I/O</th><th>Description</th></tr>
<tr><td rowspan="5">Display timing generator circuit</td><td>CL</td><td>1</td><td>I/O</td><td>This is the display clock input/output pin.
The function of this pin will be as follows depending on the states of M/$\overline{S}$ and CLS signals.
<table><tr><th>M/$\overline{S}$</th><th>CLS</th><th>CL</th></tr><tr><td rowspan="2">"H"</td><td>"H"</td><td>Output</td></tr><tr><td>"L"</td><td>Input</td></tr><tr><td rowspan="2">"L"</td><td>"H"</td><td>Input</td></tr><tr><td>"L"</td><td>Input</td></tr></table>
When the ML9050/9051 is used in the master/slave mode, the corresponding CL pin has to be connected.</td></tr>
<tr><td>FR</td><td>1</td><td>I/O</td><td>This is the input/output pin for LCD display frame reversal signal.
M/$\overline{S}$ = "H": Output
M/$\overline{S}$ = "L": Input
When the ML9050/9051 is used in the master/slave mode, the corresponding FR pin has to be connected.</td></tr>
<tr><td>$\overline{DOF}$</td><td>1</td><td>I/O</td><td>This is the blanking control pin for the LCD display.
M/$\overline{S}$ = "H": Output
M/$\overline{S}$ = "L": Input
When the ML9050/9051 is used in the master/slave mode, the corresponding $\overline{DOF}$ pin has to be connected.</td></tr>
<tr><td>FRS</td><td>1</td><td>O</td><td>This is the output pin for static drive.
This pin is used in combination with the FR pin.</td></tr>
<tr><td rowspan="4">Power supply circuit</td><td>IRS</td><td>1</td><td>I</td><td>This is the pin for selecting the resistor for adjusting the voltage V1.
IRS = "H": The internal resistor is used.
IRS = "L": The internal resistor is not used. The voltage V1 is adjusted using the external potential divider resistors connected to the pins VR.
This pin is effective only in the master operation. This pin is tied to the "H" or the "L" level during slave operation.</td></tr>
<tr><td>$\overline{HPM}$</td><td>1</td><td>I</td><td>This is the power control pin for the LCD drive power supply circuit.
$\overline{HPM}$ = "H": Normal mode
$\overline{HPM}$ = "L": High power mode
This pin is effective only during master operation mode. This pin is tied to the "H" or the "L" level during slave operation.</td></tr>
<tr><td>V_{DD}</td><td>13</td><td>—</td><td>This pin is tied to the MPU power supply terminal VCC.</td></tr>
<tr><td>V_{SS}</td><td>9</td><td>—</td><td>This is the 0 V pin connected to the system ground (GND).</td></tr>
<tr><td></td><td>V_{IN}</td><td>4</td><td>—</td><td>This is the reference power supply of the voltage multiplier circuit for driving the LCD.</td></tr>
</table>

<table>
<tr><th>Function</th><th>Pin name</th><th>Number of pins</th><th>I/O</th><th>Description</th></tr>
<tr><td rowspan="6">Power supply circuit</td><td>V_{RS}</td><td>2</td><td>—</td><td>This is the external input VREG power supply for the LCD power supply voltage adjustment circuit.
(This pin should be left open when not used as an external input)
This pin is effective only in the case of optional devices with the VREG external input option.</td></tr>
<tr><td>V_{OUT}</td><td>2</td><td>O</td><td>These are the output pins during voltage multiplication. Connect a capacitor between these pins and V_{SS}.</td></tr>
<tr><td>V1
V2
V3
V4
V5</td><td>10</td><td>—</td><td>These are the multiple level power supply pins for the LCD power supply. The voltages specified for the LCD cells are applied to these pins after resistor network voltage division or after impedance transformation using operational amplifiers. The voltages are specified taking V_{SS} as the reference, and the following relationship should be maintained among them.
$V1 \geq V2 \geq V3 \geq V4 \geq V5 \geq V_{SS}$
Master operation: When the power supply is ON, the following voltages are applied to V2 to V5 from the built-in power supply circuit. The selection of voltages is determined by the LCD bias set command.
<table>
<tr><td></td><td colspan="2">ML9050</td></tr>
<tr><td>V2</td><td>$8/9 \times V1$</td><td>$6/7 \times V1$</td></tr>
<tr><td>V3</td><td>$7/9 \times V1$</td><td>$5/7 \times V1$</td></tr>
<tr><td>V4</td><td>$2/9 \times V1$</td><td>$2/7 \times V1$</td></tr>
<tr><td>V5</td><td>$1/9 \times V1$</td><td>$1/7 \times V1$</td></tr>
</table>
<table>
<tr><td></td><td colspan="2">ML9051</td></tr>
<tr><td>V2</td><td>$7/8 \times V1$</td><td>$5/6 \times V1$</td></tr>
<tr><td>V3</td><td>$6/8 \times V1$</td><td>$4/6 \times V1$</td></tr>
<tr><td>V4</td><td>$2/8 \times V1$</td><td>$2/6 \times V1$</td></tr>
<tr><td>V5</td><td>$1/8 \times V1$</td><td>$1/6 \times V1$</td></tr>
</table></td></tr>
<tr><td>VR</td><td>2</td><td>I</td><td>Voltage adjustment pins. Voltages between V1 and VSS are applied using a resistance voltage divider.
These pins are effective only when the internal resistors for voltage V1 adjustment are not used (IRS = "L").
Do not use these pins when the internal resistors for voltage V1 adjustment are used (IRS = "H").</td></tr>
<tr><td>VC1+</td><td>2</td><td>O</td><td>These are the pins for connecting the positive side of the capacitors for voltage multiplication.
Connect capacitors between VS1– and these pins.</td></tr>
<tr><td>VS1–</td><td>2</td><td>O</td><td>These are the pins for connecting the negative side of the capacitors for voltage multiplication.
Connect capacitors between these pins and VC1+, VC3+, and VC5+.</td></tr>
</table>

<table>
<tr><th>Function</th><th>Pin name</th><th>Number of pins</th><th>I/O</th><th>Description</th></tr>
<tr><td rowspan="6">Power supply circuit</td><td>VC2+</td><td>2</td><td>O</td><td>These are the pins for connecting the positive side of the capacitors for voltage multiplication.
Connect capacitors between VS2– and these pins.</td></tr>
<tr><td>VS2–</td><td>2</td><td>O</td><td>These are the pins for connecting the negative side of the capacitors for voltage multiplication.
Connect capacitors between these pins and VC2+, VC4+, and VC6+ (during 7-times voltage multiplication).</td></tr>
<tr><td>VC3+</td><td>2</td><td>O</td><td>These are the pins for connecting the positive side of the capacitors for voltage multiplication.
Connect capacitors between VS1– and these pins.</td></tr>
<tr><td>VC4+</td><td>2</td><td>O</td><td>These are the pins for connecting the positive side of the capacitors for voltage multiplication.
Connect capacitors between VS2– and these pins.</td></tr>
<tr><td>VC5+</td><td>2</td><td>O</td><td>These are the pins for connecting the positive side of the capacitors for voltage multiplication.
Connect capacitors between VS1– and these pins.</td></tr>
<tr><td>VC6+</td><td>2</td><td>O</td><td>These are the pins for connecting the positive side of the capacitors for voltage multiplication.
Connect capacitors between VS2– and these pins (during 7-times voltage multiplication).
For 6-times voltage multiplication, connect these pins to the V_{OUT} pin.</td></tr>
<tr><td>LCD Drive output</td><td>SEG0 to SEG131</td><td>132</td><td>O</td><td>These are the LCD segment drive outputs.
One of the levels among V1, V3, V4, and V_{SS} is selected depending on the combination of the display RAM content and the FR signal.
<table>
<tr><th rowspan="2">RAM Data</th><th rowspan="2">FR</th><th colspan="2">Output voltage</th></tr>
<tr><th>Normal display</th><th>Reverse display</th></tr>
<tr><td>H</td><td>H</td><td>V1</td><td>V3</td></tr>
<tr><td>H</td><td>L</td><td>VSS</td><td>V4</td></tr>
<tr><td>L</td><td>H</td><td>V3</td><td>V1</td></tr>
<tr><td>L</td><td>L</td><td>V4</td><td>V_{SS}</td></tr>
<tr><td>Power save</td><td>—</td><td colspan="2">V_{SS}</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Function</th><th>Pin name</th><th>Number of pins</th><th>I/O</th><th>Description</th></tr>
<tr><td rowspan="2">LCD Drive output</td><td>COM0 to COMn</td><td>96</td><td>O</td><td>These are the LCD common drive outputs.
<table><tr><td></td><td>COM</td></tr><tr><td>ML9050</td><td>COM0 to COM63</td></tr><tr><td>ML9051</td><td>COM0 to COM47</td></tr></table>
One of the levels among V1, V2, V5, and VSS is selected depending on the combination of the scan data and the FR signal.
<table><tr><td>Scan data</td><td>FR</td><td>Output voltage</td></tr><tr><td>H</td><td>H</td><td>VSS</td></tr><tr><td>H</td><td>L</td><td>V1</td></tr><tr><td>L</td><td>H</td><td>V2</td></tr><tr><td>L</td><td>L</td><td>V5</td></tr><tr><td>Power save</td><td>—</td><td>V_{SS}</td></tr></table></td></tr>
<tr><td>COMS</td><td>2</td><td>O</td><td>These are the COM output pins only for indicators. Both pins output the same signal. Leave these pins open when they are not used.
The same signal is output in both master and slave operation modes.</td></tr>
<tr><td rowspan="2">Test pin</td><td>TEST0</td><td></td><td>I</td><td rowspan="2">These are the pins for testing the IC chip. Leave these pins open during normal use.</td></tr>
<tr><td>TEST1</td><td></td><td>O</td></tr>
</table>

FUNCTIONAL DESCRIPTION

MPU Interface

• Selection of interface type

The ML9050/9051 carries out data transfer using either the 8-bit bi-directional data bus (D7 to D0) or the serial data input line (SI). Either the 8-bit parallel data input or serial data input can be selected as shown in Table 1 by setting the P/$\overline{S}$ pin to the "H" or the "L" level.

Table 1

P/$\overline{S}$	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5 to D0
H: Parallel input	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5 to D0
L: Serial input	$\overline{CS1}$	CS2	A0	—	—	—	SI	SCL	(HZ)

A hyphen (—) indicates that the pin can be tied to the "H" or the "L" level.

• Parallel interface

When the parallel interface is selected, (P/$\overline{S}$ = "H"), it is possible to connect this LSI directly to the MPU bus of either an 80-series MPU or a 68-series MPU as shown in Table 2 depending on whether the pin C86 is set to "H" or "L".

Table 2

P/$\overline{S}$	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D7 to D0
H: 68-Series MPU bus	$\overline{CS1}$	CS2	A0	E	R/$\overline{W}$	D7 to D0
L: 80-Series MPU bus	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D7 to D0

The data bus signals are identified as shown in Table 3 below depending on the combination of the signals A0, $\overline{RD}$(E), and $\overline{WR}$(R/$\overline{W}$) of Table 2.

Table 3

	Common	68-Series	80-Series	
	A0	R/$\overline{W}$	$\overline{RD}$	$\overline{WR}$
Display data read	1	1	0	1
Display data write	1	0	1	0
Status read	0	1	0	1
Control data write (command)	0	0	1	0

Serial interface

When the serial interface is selected (P/$\overline{S}$ = "L"), the serial data input (SI) and the serial clock input (SCL) can be accepted if the chip is in the active state ($\overline{CS1}$ = "L" and CS2 = "H"). The serial interface consists of an 8-bit shift register and a 3-bit counter. The serial data is read in from the serial data input pin in the sequence D7, D6, ... , D0 at the rising edge of the serial clock input, and is converted into parallel data at the rising edge of the 8th serial clock pulse and processed further. The identification of whether the serial data is display data or command is judged based on the A0 input, and the data is treated as display data when A0 is "H" and as command when A0 is "L". The A0 input is read in and identified at the rising edge of the (8 × n) th serial clock pulse after the chip has become active. Fig. 1 shows the signal chart of the serial interface. (When the chip is not active, the shift register and the counter are reset to their initial states. No data read out is possible in the case of the serial interface. It is necessary to take sufficient care about wiring termination reflection and external noise in the case of the SCL signal. We recommend verification of operation in an actual unit.)

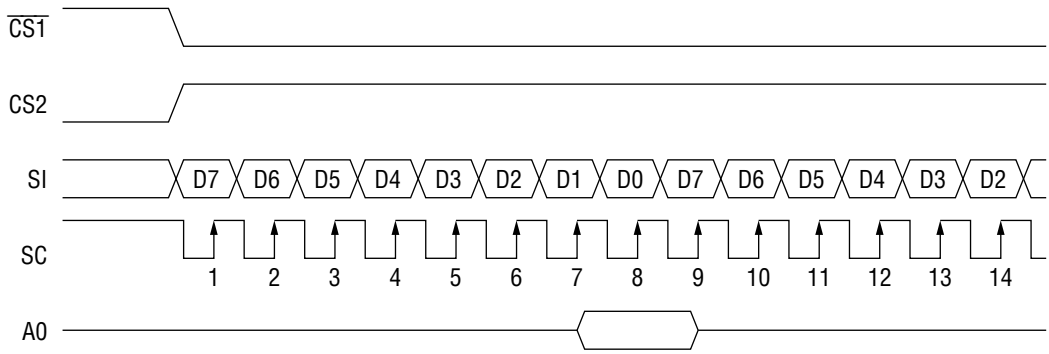


Fig. 1

• Chip select

The ML9050/9051 has the two chip select pins $\overline{CS1}$ and CS2, and the MPU interface or the serial interface is enabled only when $\overline{CS1}$ = "L" and CS2 = "H". When the chip select signals are in the inactive state, the D0 to D7 lines will be in the high impedance state and the inputs A0, $\overline{RD}$, and $\overline{WR}$ will not be effective. When the serial interface has been selected, the shift register and the counter are reset when the chip select signals are in the inactive state.

• Accessing the display data RAM and the internal registers

Accessing the ML9050/9051 from the MPU side requires merely that the cycle time (t_{CYC}) be satisfied, and high speed data transfer without requiring any wait time is possible. Also, during the data transfer with the MPU, the ML9050/9051 carries out a type of pipeline processing between LSIs via a bus holder associated with the internal data bus. For example, when the MPU writes data in the display data RAM, the data is temporarily stored in the bus holder, and is then written into the display data RAM before the next data read cycle. Further, when the MPU reads out data in the display data RAM, first a dummy data read cycle is carried out to temporarily store the data in the bus holder which is then placed on the system bus and is read out during the next read cycle. There is a restriction on the read sequence of the display data RAM, which is that the read instruction immediately after setting the address does not read out the data of that address, but that data is output as the data of the address specified during the second data read sequence, and hence care should be taken about this during reading. Therefore, always one dummy read is necessary immediately after setting the address or after a write cycle. This relationship is shown in Figs 2(a) and 2(b).

• Data write

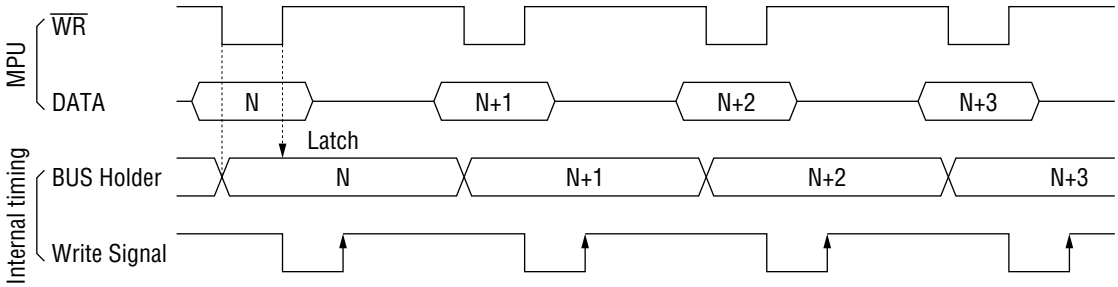


Fig. 2(a)

• Data read

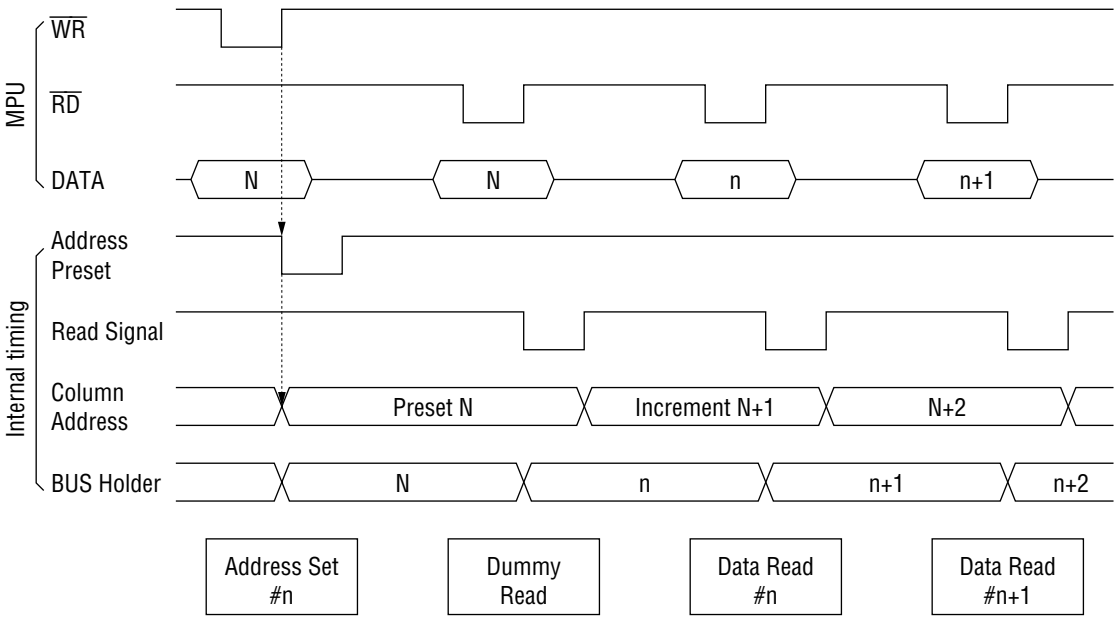


Fig. 2(b)

• Busy flag

The busy flag being "1" indicates that the ML9050/9051 is carrying out internal operations, and hence no instruction other than a status read instruction is accepted during this period. The busy flag is output at pin D7 when a status read instruction is executed. If the cycle time (t_{CYC}) is established, there is no need to check this flag before issuing every command and hence the processing performance of the MPU can be increased greatly.

Display data RAM

• Display data RAM

This is the RAM storing the dot data for display and has an organization of 65 (8 pages × 8 bits +1) × 132 bits. It is possible to access any required bit by specifying the page address and the column address. Since the display data D7 to D0 from the MPU corresponds to the LCD display in the direction of the common lines as shown in Fig. 3, there are fewer restrictions during display data transfer when the ML9050/9051 is used in a multiple chip configuration, thereby making it easily possible to realize a display with a high degree of freedom. Also, since the display data RAM read/write from the MPU side is carried out via an I/O buffer, it is done independent of the signal read operation for the LCD drive. Consequently, the display is not affected by flickering, etc., even when the display data RAM is accessed asynchronously during the LCD display operation.

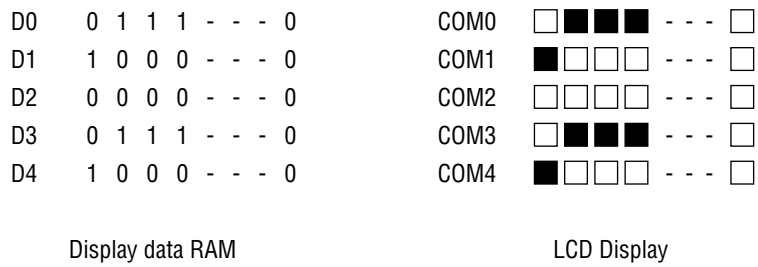


Fig. 3

• Page address circuit

The page address of the display data RAM is specified using the page address set command as shown in Fig. 4. Specify the page address again when accessing after changing the page. The page address 8 (D3, D2, D1, D0 → 1, 0, 0, 0) is the RAM area dedicated to the indicator, and only the display data D0 is valid in this page.

• Column address circuit

The column address of the display data RAM is specified using the column address set command as shown in Fig. 4. Since the specified column address is incremented (by +1) every time a display data read/write command is issued, the MPU can access the display data continuously. Further, the incrementing of the column address is stopped at the column address of 83H. Since the column address and the page address are independent of each other, it is necessary, for example, to specify separately the new page address and the new column address when changing from column 83H of page 0 to column 00H of page 1. Also, as is shown in Table 4, it is possible to reverse the correspondence relationship between the display data RAM column address and the segment output using the ADC command (the segment driver direction select command). This reduces the IC placement restrictions at the time of assembling LCD modules.

Table 4

	SEG Output	
ADC	SEG0	SEG131
D0 = "0"	0(H) → Column Address →	83(H)
D0 = "1"	83(H) ← Column Address ←	0(H)

• Line address circuit

The line address circuit is used for specifying the line address corresponding to the COM output when displaying the contents of the display data RAM as is shown in Fig. 4. Normally, the topmost line in the display (COM0 output in the normal display state of the common output, and COM63 output and COM47 output for the ML9050 and the ML9051, respectively, in the reverse display stage) is specified using the display start line address set command. The display area is 65 lines and 49 lines for the ML9050 and the ML9051, respectively, in the direction of increasing line address from the specified display start line address. It is possible to carry out screen scrolling and page changing by dynamically changing the line address using the display start line address set command.

• Display data latch circuit

The display data latch circuit is a latch for temporarily storing the data from the display data RAM before being output to the LCD drive circuits. Since the commands for selecting normal/reverse display and turning the display ON/OFF control the data in this latch, the data in the display data RAM will not be changed.

Oscillator circuit

This is an RC oscillator that generates the display clock. The oscillator circuit is effective only when M/$\overline{S}$ = "H" and also CLS = "H". The oscillations will be stopped when CLS = "L", and the display clock has to be input to the CL pin.

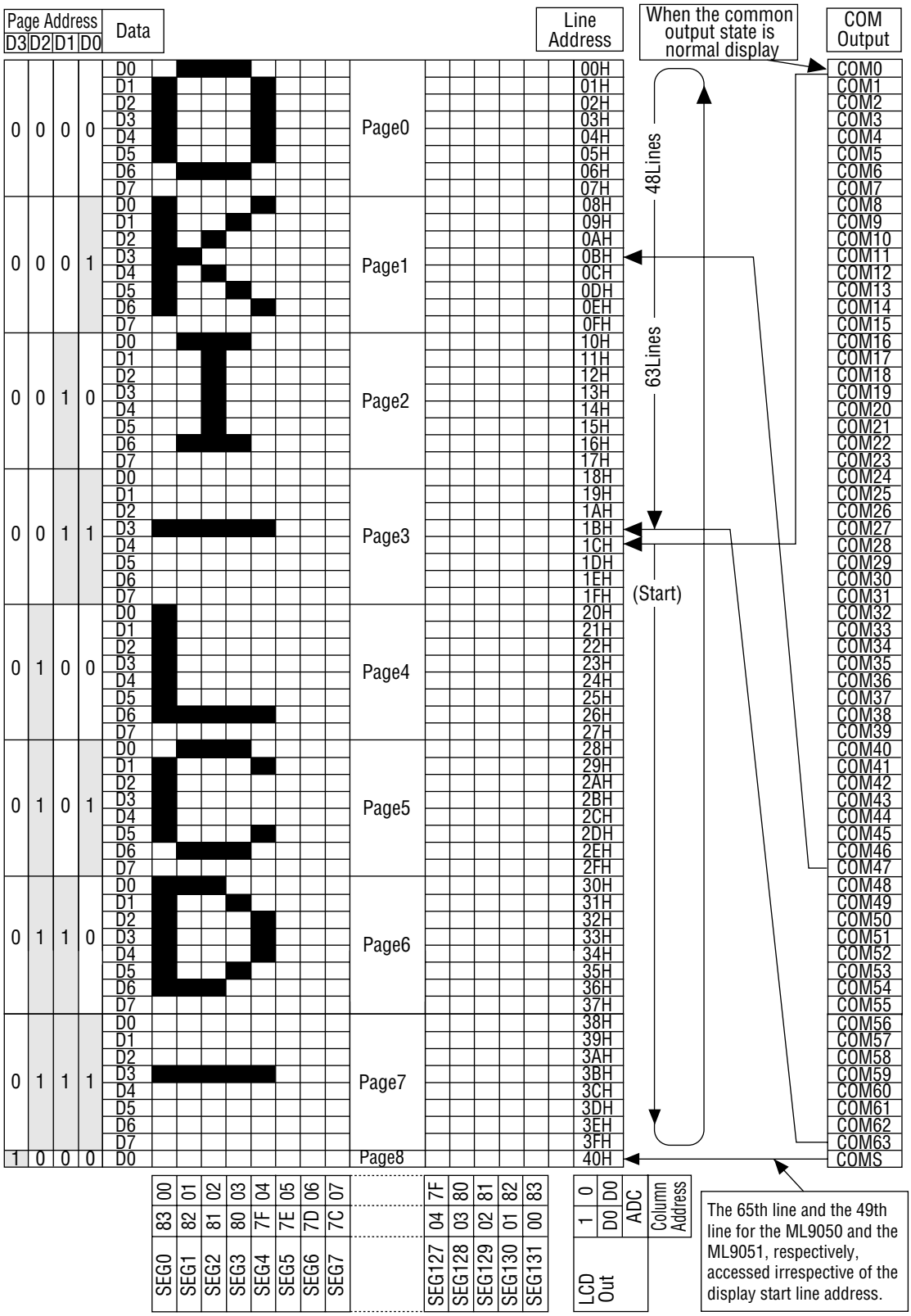

Page Address
D3 D2 D1 D0
Data
Line Address
When the common output state is normal display
COM Output
Page0
Page1
Page2
Page3
Page4
Page5
Page6
Page7
Page8
48Lines
63Lines
(Start)
COM0 COM1 COM2 COM3 COM4 COM5 COM6 COM7 COM8 COM9 COM10 COM11 COM12 COM13 COM14 COM15 COM16 COM17 COM18 COM19 COM20 COM21 COM22 COM23 COM24 COM25 COM26 COM27 COM28 COM29 COM30 COM31 COM32 COM33 COM34 COM35 COM36 COM37 COM38 COM39 COM40 COM41 COM42 COM43 COM44 COM45 COM46 COM47 COM48 COM49 COM50 COM51 COM52 COM53 COM54 COM55 COM56 COM57 COM58 COM59 COM60 COM61 COM62 COM63 COMS
SEG0 SEG1 SEG2 SEG3 SEG4 SEG5 SEG6 SEG7
SEG127 SEG128 SEG129 SEG130 SEG131
LCD Out
ADC
Column Address
The 65th line and the 49th line for the ML9050 and the ML9051, respectively, accessed irrespective of the display start line address.

Fig. 4

Display timing generator circuit

This circuit generates the timing signals for the line address circuit and the display data latch circuit from the display clock. The display data is latched in the display data latch circuit and is output to the segment drive output pins in synchronization with the display clock. This circuit generates the timing signals for the line address circuit and the display data latch circuit from the display clock. The display data is latched in the display data latch circuit and is output to the segment drive output pins in synchronization with the display clock. The read out of the display data to the LCD drive circuits is completely independent of the display data RAM access from the MPU. As a result, there is no bad influence such as flickering on the display even when the display data RAM is accessed asynchronously during the LCD display. Also, the internal common timing and LCD frame reversal (FR) signals are generated by this circuit from the display clock. The drive waveforms of the frame reversal drive method shown in Fig. 5(a) for the LCD drive circuits are generated by this circuit. Further, the drive waveforms of the line reversal method shown in Fig. 5(b) can also be generated depending on the issued command.

In the line reversal drive method, it is possible to carry out reverse display drive at every line to a maximum of 32 lines. Fig. 5(b) shows the waveforms of the 1 line reversal drive method.

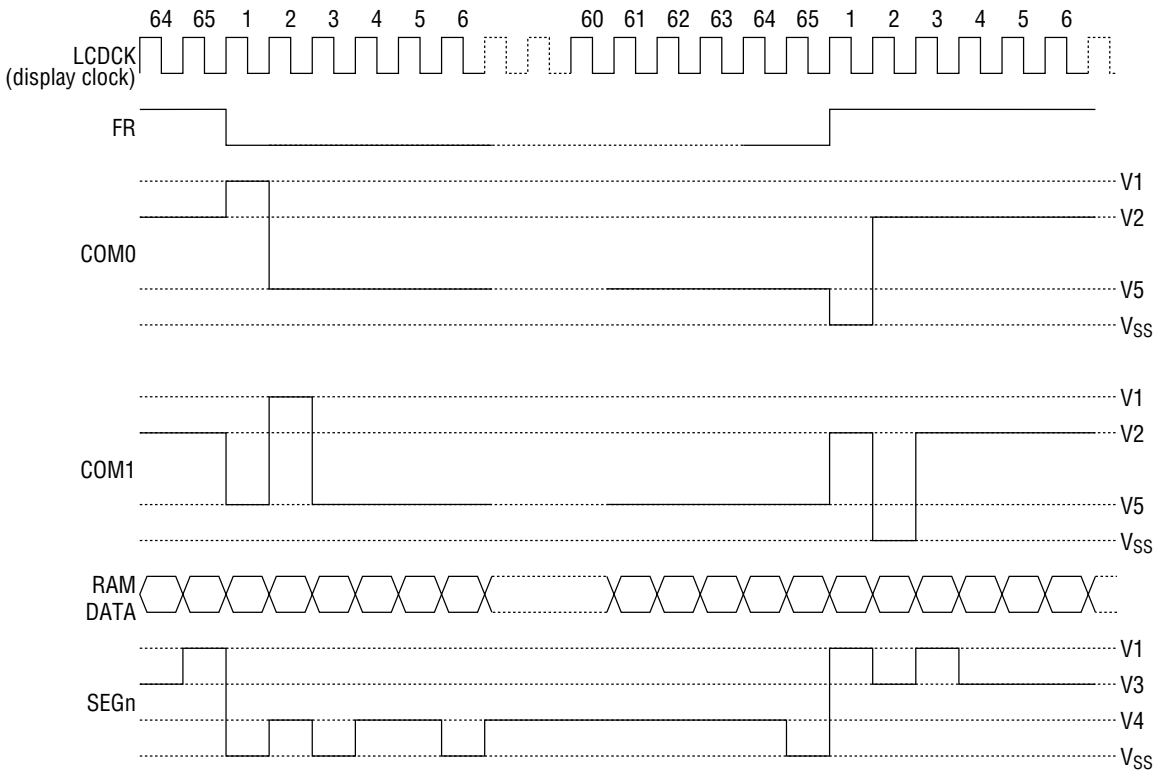


Fig. 5(a) Waveforms in the frame reversal drive method

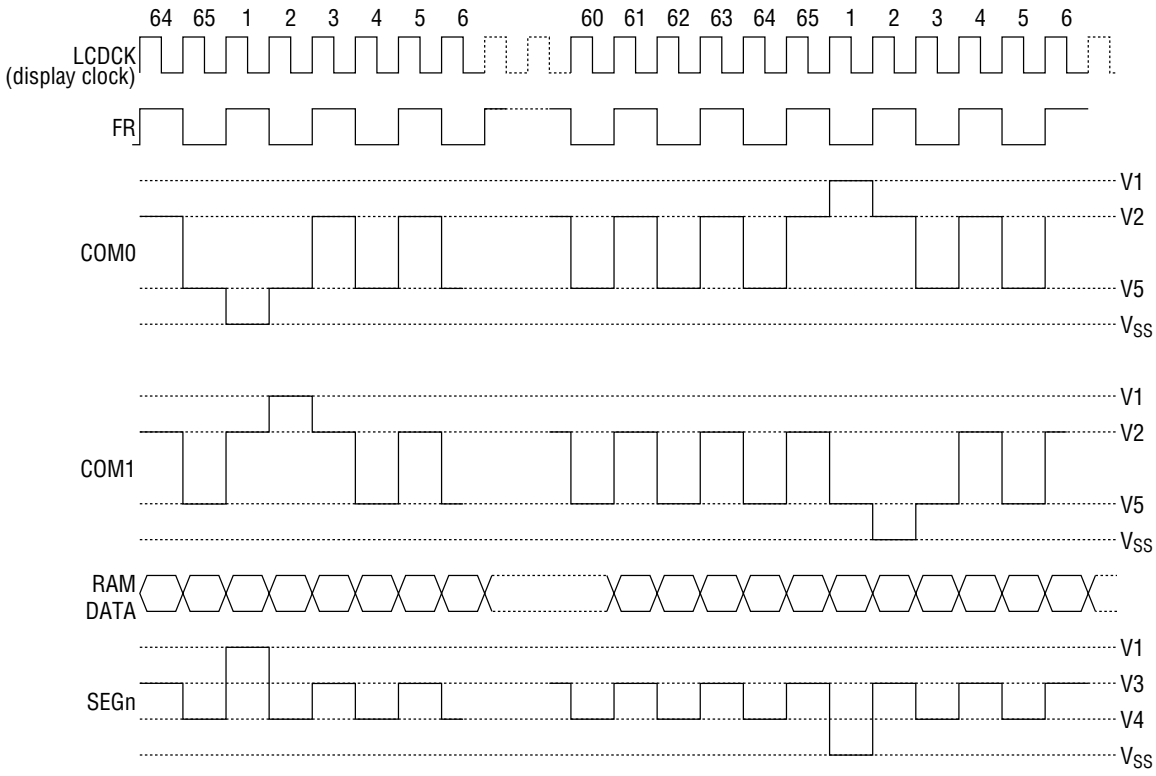


Fig. 5(b) Waveforms in the line reversal drive method

When the ML9050/9051 is used in a multiple chip configuration, it is necessary to supply the slave side display timing signals (FR, CL, and $\overline{DOF}$) from the master side.
The statuses of the signals FR, CL, and $\overline{DOF}$ are shown in Table 5.

Table 5

Operating mode		FR	CL	$\overline{DOF}$
Master mode (M/$\overline{S}$ = "H")	Internal oscillator circuit enabled (CLS = H)	Output	Output	Output
	Internal oscillator circuit disabled (CLS = L)	Output	Input	Output
Slave mode (M/$\overline{S}$ = "L")	Internal oscillator circuit enabled (CLS = H)	Input	Input	Input
	Internal oscillator circuit disabled (CLS = L)	Input	Input	Input

Common output state selection circuit (see Table 6)

Since the COM output scanning directions can be set using the common output state selection command in the ML9050/9051, it is possible to reduce the IC placement restrictions at the time of assembling LCD modules.

Table 6

State	COM Scanning direction	
	ML9050	ML9051
Normal Display	COM0 → COM63	COM0 → COM47
Reverse Display	COM63 → COM0	COM47 → COM0

LCD Drive circuits

This LSI incorporates 197 sets and 181 sets of multiplexers for the ML9050 and the ML9051, respectively, that generate 4-level outputs for driving the LCD. These output the LCD drive voltage in accordance with the combination of the display data, COM scanning signals, and the FR signal. Fig. 6 shows examples of the SEG and COM output waveforms in the frame reversal drive method.

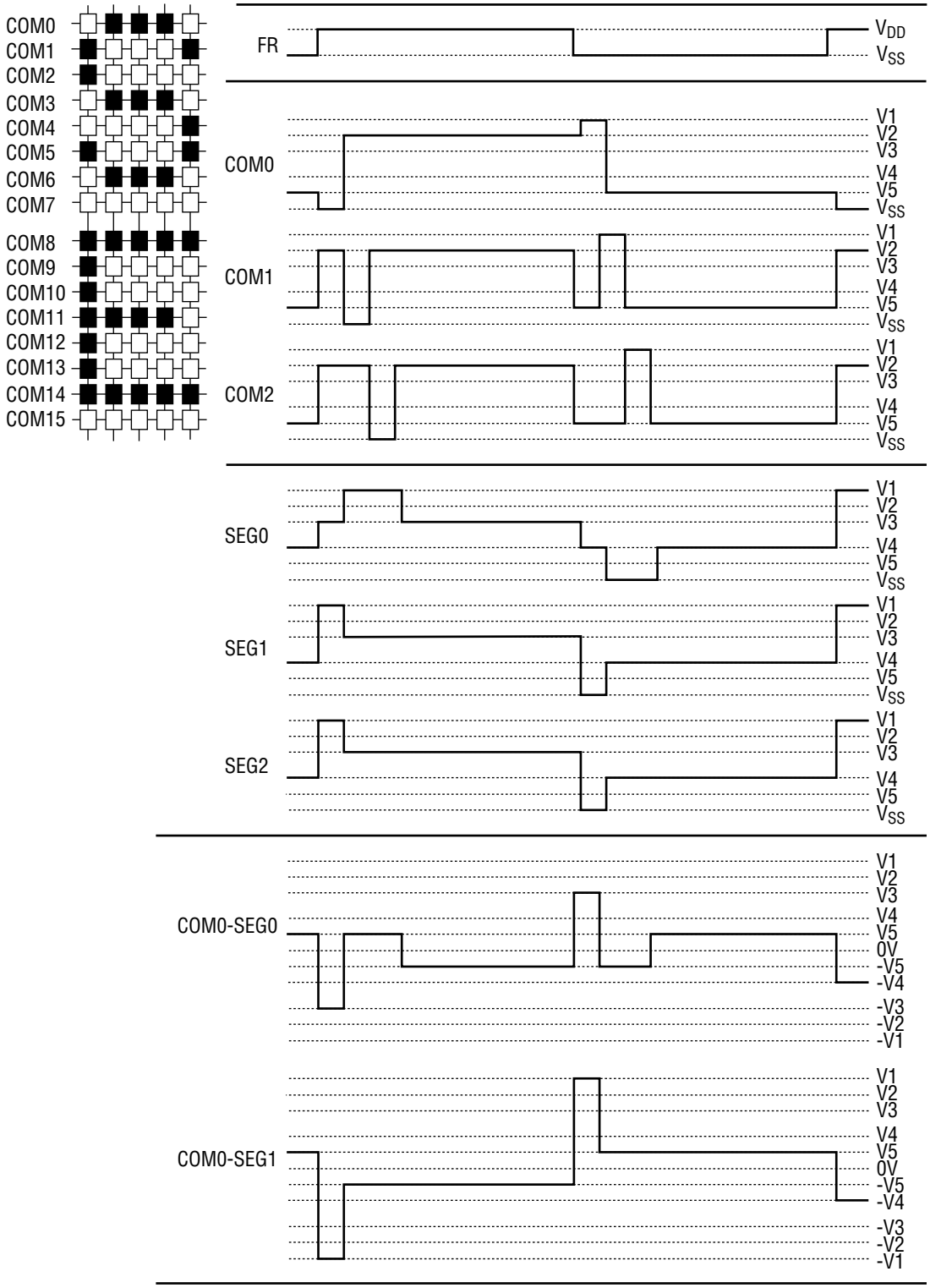

COM0
COM1
COM2
COM3
COM4
COM5
COM6
COM7
COM8
COM9
COM10
COM11
COM12
COM13
COM14
COM15
FR
VDD
VSS
COM0
COM1
COM2
SEG0
SEG1
SEG2
V1
V2
V3
V4
V5
VSS
COM0-SEG0
COM0-SEG1
0V
-V5
-V4
-V3
-V2
-V1

Fig. 6

Power supply circuit

This is the low power consumption type power supply circuit for generating the voltages necessary for driving LCD devices, and consists of voltage multiplier circuits, voltage adjustment circuits, and voltage follower circuits. In the power supply circuit, it is possible to control the ON/OFF of each of the circuits of the voltage multiplier, voltage adjustment circuits, and voltage follower circuits using the power control set command. As a result, it is also possible to use parts of the functions of both the external power supply and the internal power supply. Table 7 shows the functions controlled by the 3-bit data of the power control set command and Table 8 shows a sample combination.

Table 7 Details of functions controlled by the bits of the power control set command

Control bit	Function controlled by the bit
D2	Voltage multiplier circuit control bit
D1	Voltage adjustment circuit (V adjustment circuit) control bit
D0	Voltage follower circuit (V/F circuit) control bit

Table 8 Sample combination for reference

State used	D2	D1	D0	Circuit			External voltage input	Voltage multiplier pins *1
				Voltage multiplier	V Adjustment	V/F		
Only the internal power supply is used	1	1	1	○	○	○	V_{IN}	Used
Only V adjustment and V/F circuits are used	0	1	1	×	○	○	V_{OUT}	OPEN
Only V/F circuits are used	0	0	1	×	×	○	V1	OPEN
Only the external power supply is used	0	0	0	×	×	×	V1 to V5	OPEN

*1: The voltage multiplier pins are the pins VC1+, VS1-, VC2+, VS2-, VC3+, VC4+, VC5+, and VC6+.
If combinations other than the above are used, normal operation is not guaranteed.

• Voltage multiplier circuits

The connections for 2-times to 7-times voltage multiplier circuits are shown below.

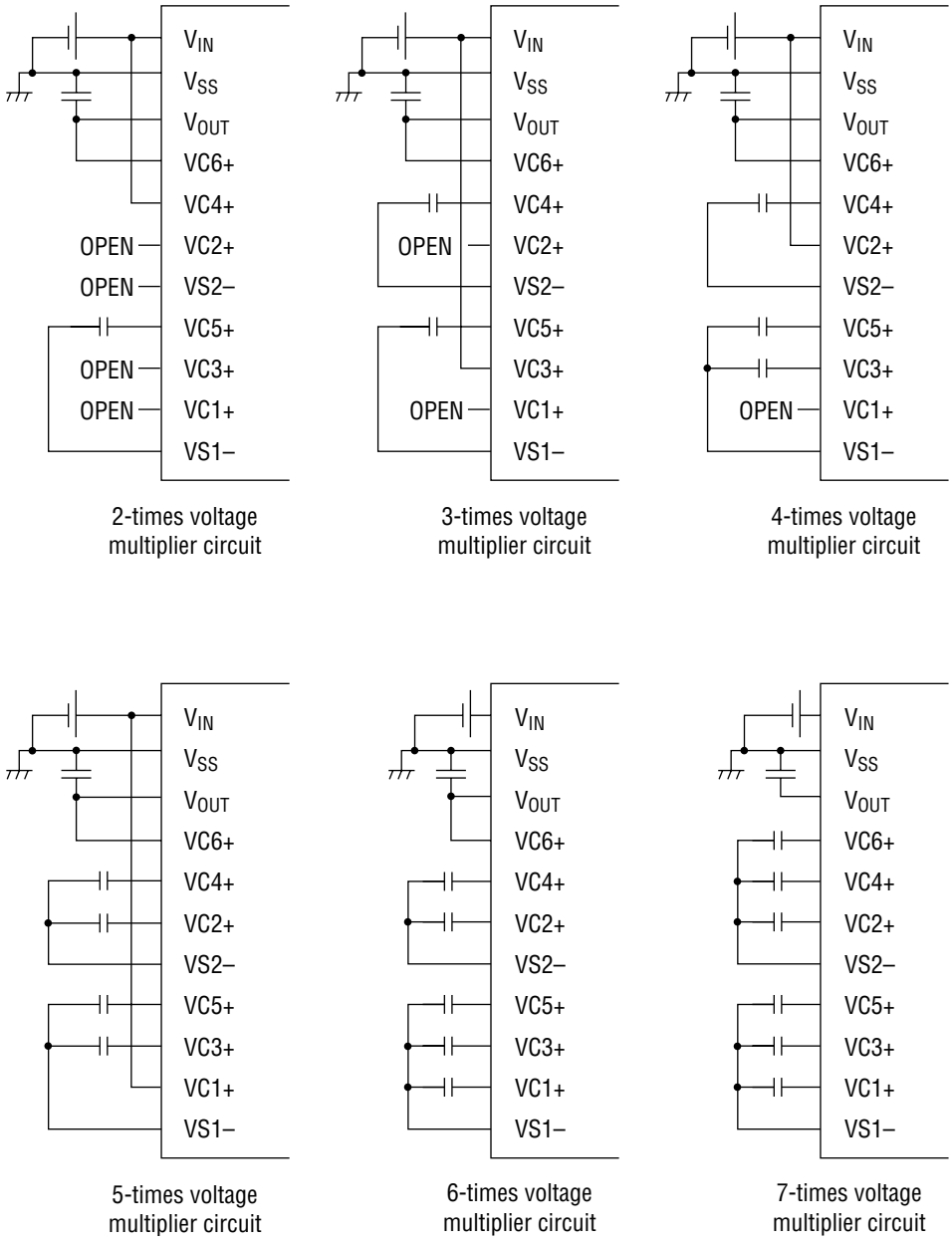
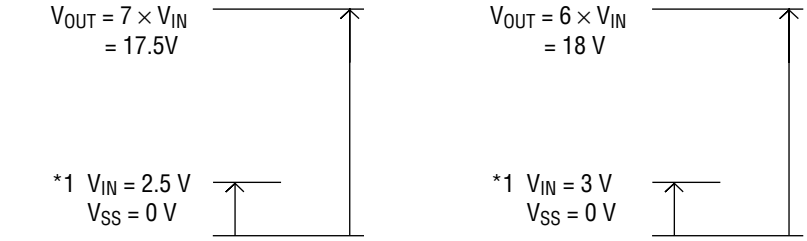


Fig. 7

The voltage relationships in voltage multiplication are shown in Fig. 8.



Voltage relationship in 7-times multiplication Voltage relationship in 6-times multiplication

Fig. 8

*1: The voltage range of V_{IN} should be set so that the voltage at the pin V_{OUT} does not exceed the absolute maximum rating.

• Voltage adjustment circuit

The voltage multiplier output VOUT produces the LCD drive voltage V1 via the voltage adjustment circuit. Since the ML9050/9051 incorporates a high accuracy constant voltage generator, a 64-level electronic potentiometer function, and also resistors for voltage V1 adjustment, it is possible to build a high accuracy voltage adjustment circuit with very few components. In addition, the ML9050/9051 is available in three models with the temperature gradients of - (1) about -0.05% / ˚C, (2) about -0.2% / ˚C, and (3) external input (input to pin VRS), as a VREG option.

(a) When the internal resistors for voltage V1 adjustment are used

It is possible to control the LCD power supply voltage V1 and adjust the intensity of LCD display using commands and without needing any external resistors, if the internal voltage V1 adjustment resistors and the electronic potentiometer function are used. The voltage V1 can be obtained by the following equation A-1 in the range of V1<VOUT.

$V1 = (1+(Rb/Ra)) \bullet VEV = (1+(Rb/Ra)) \bullet (1-(\alpha/324)) \bullet VREG$ (Eqn. A-1)

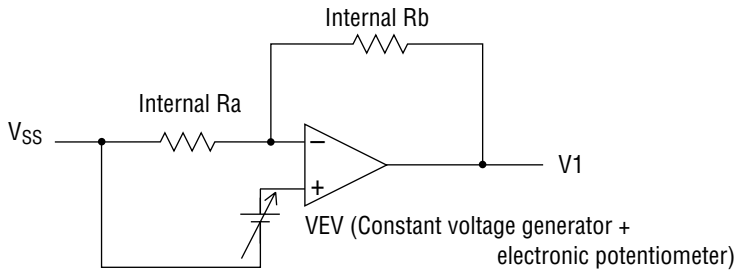


Fig. 9

VREG is a constant voltage generated inside the IC and its value is constant as given in Table 9 at Ta = 25˚C.

Table 9

Model	Temperature gradient	Unit	VREG	Unit
(1) Internal power supply	–0.05	[%/°C]	3.0	[V]
(2) Internal power supply	–0.2	[%/°C]	3.0	[V]
(3) External input	—	—	VRS	[V]

Here, α is the electronic potentiometer function which allows one level among 64 levels to be selected by merely setting the data in the 6-bit electronic potentiometer register. The values of α set by the electronic potentiometer register are shown in Table 10.

Table 10

α	D5	D4	D3	D2	D1	D0
63	0	0	0	0	0	0
62	0	0	0	0	0	1
61	0	0	0	0	1	0
⋮	⋮	⋮	⋮	⋮	⋮	
1	1	1	1	1	1	0
0	1	1	1	1	1	1

Rb/Ra is the voltage V1 adjustment internal resistor ratio and can be adjusted to one of 8 levels by the voltage V1 adjustment internal resistor ratio set command. The reference values of the ratio (1+Rb/Ra) according to the 3-bit data set in the voltage V1 adjustment internal resistor ratio setting register are listed in Table 11.

Table 11 Voltage V1 adjustment internal resistor ratio setting register values and the ratio (1+Rb/Ra) (For reference)

Register value			ML9050			ML9051		
			Temperature gradient of the model [unit: %/°C]			Temperature gradient of the model [unit: %/°C]		
D2	D1	D0	–0.05	–0.2	VREG *1	–0.05	–0.2	VREG *1
0	0	0	3.0	3.0	1.5	3.0	3.0	1.5
0	0	1	3.5	3.5	2.0	3.5	3.5	2.0
0	1	0	4.0	4.0	2.5	4.0	4.0	2.5
0	1	1	4.5	4.5	3.0	4.5	4.5	3.0
1	0	0	5.0	5.0	3.5	5.0	5.0	3.5
1	0	1	5.5	5.5	4.0	5.4	5.5	4.0
1	1	0	6.0	6.0	4.5	5.9	6.0	4.5
1	1	1	6.5	6.5	5.0	6.5	6.5	5.0

*1: VREG is the external input.

(b) When external resistors are used (voltage V1 adjustment internal resistors are not used) - Case 1

It is also possible to set the LCD drive power supply voltage V1 without using the internal resistors for voltage V1 adjustment but connecting external resistors (Ra' and Rb') between V_{SS} & VR and between VR & V1. Even in this case, it is possible to control the LCD power supply voltage V1 and adjust the intensity of LCD display using commands if the electronic potentiometer function is used.

The voltage V1 can be obtained by the following equation B-1 in the range of $V1<V_{OUT}$ by setting the external resistors Ra' and Rb' appropriately.

$V1 = (1+(Rb'/Ra')) \bullet VEV = (1+(Rb'/Ra')) \bullet (1-(\alpha/324)) \bullet VREG$ (Eqn. B-1)

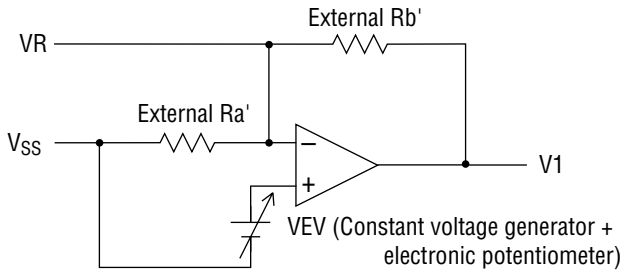


Fig. 10

Setting example: Setting V1 = 7 V at Ta = 25℃ using an ML9050/9051 of the model with a temperature gradient of -0.05%/℃.

When the electronic potentiometer register value is set to the middle value of (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0), the value of α will be 31 and that of VREG will be 3.0 V, and hence the equation B-1 becomes as follows:

$V1 = (1+(Rb'/Ra')) \bullet (1-(\alpha/324)) \bullet VREG$

$7 = (1+(Rb'/Ra')) \bullet (1-(31/324)) \bullet 3.0$ (Eqn. B-2)

Further, if the current flowing through Ra' and Rb' is set as 5μA, the value of Ra'+Rb' will be -

$Ra'+Rb' = 1.4M\Omega$ (Eqn. B-3)

and hence,

$Rb'/Ra' = 1.58$, $Ra' = 543k\Omega$, $Rb' = 857k\Omega$.

In this case, the variability range of voltage V1 using the electronic potentiometer function and the increment size will be as given in Table 12.

Table 12

V1	Min	Typ	Max	Unit
Variability range	6.24 (level 0)	7.0 (center value)	7.74 (level 63)	[V]
Increment size		24		[mV]

(c) When external resistors are used (voltage V1 adjustment internal resistors are not used) - Case 2

It is possible to set the LCD drive power supply voltage V1 using fine adjustment of Ra' and Rb' by adding a variable resistor to the case of using external resistors in the above case. Even in this case, it is possible to control the LCD power supply voltage V1 and adjust the intensity of LCD display using commands if the electronic potentiometer function is used.

The voltage V1 can be obtained by the following equation C-1 in the range of $V1<V_{OUT}$ by setting the external resistors R_1, R_2 (variable resistor), and R_3 appropriately and making fine adjustment of R_2 (ΔR_2).

$V1 = (1+(R_3+R_2-\Delta R_2)/(R_1+\Delta R_2)) \bullet VEV$

$= (1+(R_3+R_2-\Delta R_2)/(R_1+\Delta R_2)) \bullet (1-(\alpha/324)) \bullet VREG$ (Eqn. C-1)

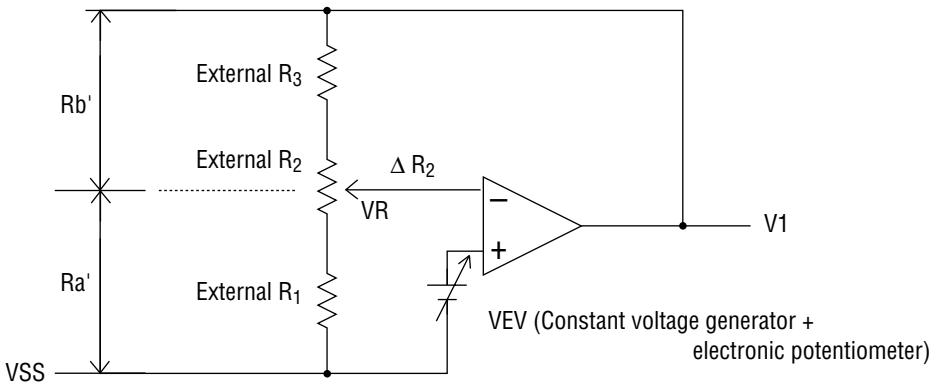


Fig. 11

Setting example: Setting V1 in the range 5 V to 9 V using R_2 at Ta = 25°C using an ML9050/9051 of the model with a temperature gradient of -0.05%/°C.

When the electronic potentiometer register value is set to the middle value of (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0), the value of α will be 31 and that of VREG will be 3.0 V, and hence in order to make V1 = 9 V when $\Delta R_2 = 0\Omega$, the equation C-1 becomes as follows:

$9 = (1+(R_3+R_2)/R_1) \bullet (1-(31/324)) \bullet (3.0)$ (Eqn. C-2)

In order to make V1 = 5 V when $\Delta R_2 = R_2$,

$5 = (1+R_3/(R_1+R_2)) \bullet (1-(31/324)) \bullet (3.0)$ (Eqn. C-3)

Further, if the current flowing between V_{SS} and V1 is set as 5 µA, the value of $R_1+R_2+R_3$ becomes-

$R_1+R_2+R_3 = 1.8M\Omega$ (Eqn. C-4)

and hence,

$R_1 = 542k\Omega$, $R_2 = 436k\Omega$, $R_3 = 822k\Omega$.

In this case, the variability range of voltage V1 using the electronic potentiometer function and the increment size will be as given in Table 13.

Table 13

V1	Min	Typ	Max	Unit
Variability range	4.45 (level 0)	7.0 (center value)	9.96 (level 63)	[V]
Increment size	17	24	31	[mV]

* When using the voltage V1 adjustment internal resistors or the electronic potentiometer function, it is necessary to set at least the voltage adjustment circuit and the voltage follower circuits both in the operating state using the power control setting command. Also, when the voltage multiplier circuit is OFF, it is necessary to supply a voltage externally to the VOUT pin.
* The pin VR is effective only when the voltage V1 adjustment internal resistors are not used (pin IRS = "L"). Leave this pin open when the voltage V1 adjustment internal resistors are being used (pin IRS = "H").
* Since the input impedance of the pin VR is high, it is necessary to take noise countermeasures such as using short wiring length or a shielded wire .

• LCD Drive voltage generator circuits

The voltage V1 is divided using resistors inside the IC to generate the voltages V2, V3, V4, and V5 that are necessary for driving the LCD. In addition, these voltages V2, V3, V4, and V5 are impedance transformed using voltage follower circuits and fed to the LCD drive circuits. The bias ratio of 1/9 or 1/7 can be selected in the ML9050 and the bias ratio of 1/8 or 1/6 can be selected in the ML9051, using the LCD bias setting command.

• High power mode

The power supply circuit incorporated in the ML9050/9051 has an extremely low power consumption.

[Normal mode: $\overline{HPM}$ = "H"]. Hence, in the case of an LCD device or panel with a large load, the display quality may become poorer. In such a case, setting the $\overline{HPM}$ pin to "L" (high power mode) can improve the quality of display. It is recommended to verify the display using an actual unit in order to decide whether or not to use this mode. Further, if the degree of display quality improvement is still not sufficient even after setting the high power mode, it is necessary to supply the LCD drive power supply from an external source.

• Command sequence for shutting off the internal power supply

When shutting off the internal power supply, it is recommended to use the procedure given in Fig. 11 of switching OFF the power after putting the LSI in the power save mode using the following command sequence.

Procedure	Description	Command address								
	(Command, status)	D7	D6	D5	D4	D3	D2	D1	D0	
Step1	Display OFF	1	0	1	0	1	1	1	0	Power save commands (multiple)
↓	↓									
Step2	Display all ON	1	0	1	0	0	1	0	1	
↓	↓									
End	Internal power supply OFF									

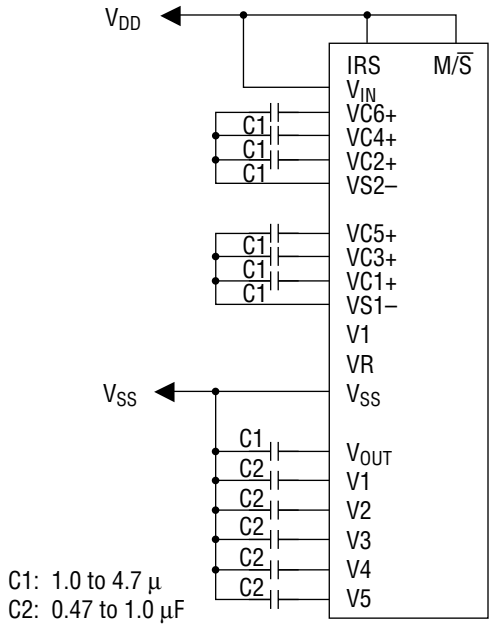
Fig. 12

• APPLICATION CIRCUITS

(1) When the voltage multiplier circuit, voltage adjustment circuit, and V/F circuits are all used

When using the voltage V1 adjustement internal resistors

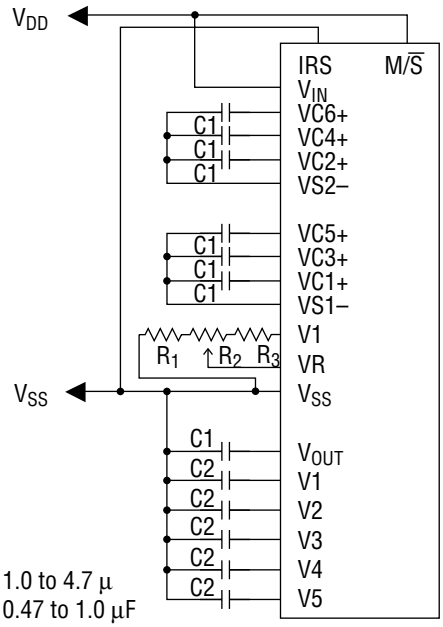
$V_{IN} = V_{DD}$ 7-Times voltage multiplication



(2) When the voltage multiplier circuit, voltage adjustment circuit, and V/F circuits are all used

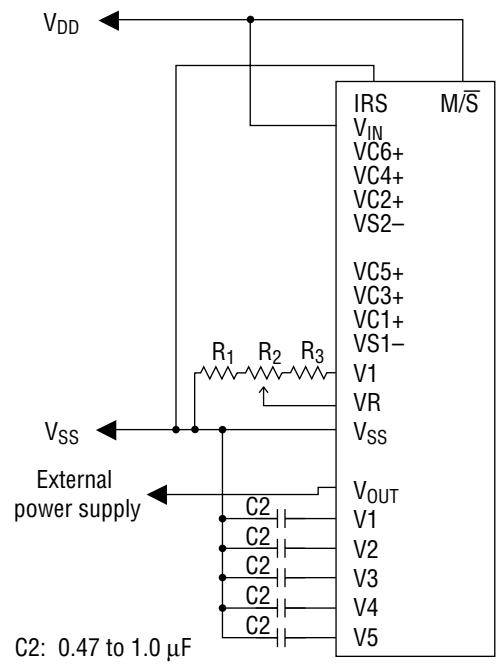
When not using the voltage V1 adjustement internal resistors

$V_{IN} = V_{DD}$ 7-Times voltage multiplication



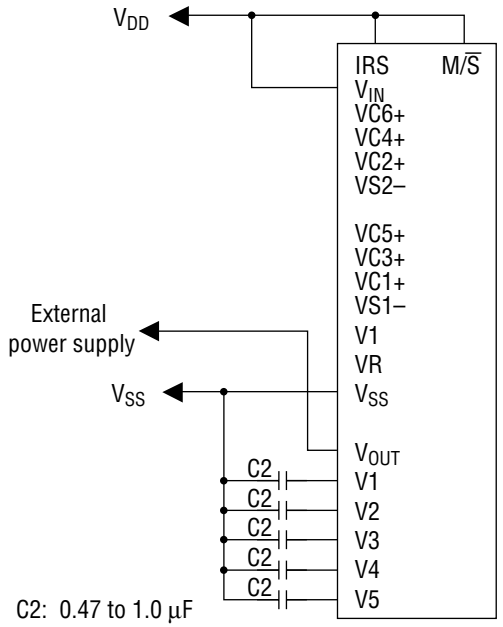
(3) When only the voltage adjustment circuit and the V/F circuits are used

When not using the voltage V1 adjustment internal resistors

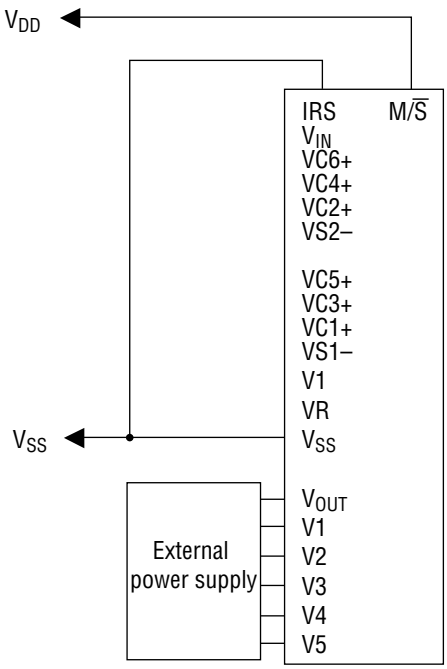


(4) When only the V/F circuits are used

When using the voltage V1 adjustment internal resistors



(5) When not using the internal power supply



• Reset circuit

This LSI goes into the initialized condition when the $\overline{RES}$ input goes to the "L" level. The initialized condition consists of the following conditions.

(1) Display OFF
(2) Normal display mode
(3) ADC Select: Incremented (ADC command D0 = "L")
(4) Power control register: (D2, D1, D0) = (0, 0, 0)
(5) The registers and data in the serial interface are cleared.
(6) LCD Power supply bias ratio: ML9050 ... 1/9 bias, ML9051 ... 1/8 bias
(7) Read-modify-write: OFF
(8) Static indicator: OFF
    Static indicator register: (D1, D2) = (0, 0)
(9) Line 1 is set as the display start line.
(10) The column address is set to address 0.
(11) The page address is set to 0.
(12) Common output state: Normal
(13) Voltage V1 adjustment internal resistor ratio register: (D2, D1, D0) = (1, 0, 0)
(14) The electronic potentiometer register set mode is released.
    Electronic potentiometer register: (D5, D4, D3, D2, D1, D0) = (1, 0, 0 ,0, 0, 0)
(15) The LCD drive method is set to the frame reversal method.
    Line reversal count register: (D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0)

On the other hand, when the reset command is used, only the conditions (7) to (15) above are set. As is shown in the "MPU Interface (example for reference)", the $\overline{RES}$ pin is connected to the Reset pin of the MPU and the initialization of this LSI is made simultaneously with the resetting of the MPU. This LSI always has to be reset using the $\overline{RES}$ pin at the time the power is switched ON. Also, excessive current can flow through this LSI when the control signal from the MPU is in the Hi-Z state. It is necessary to take measures to ensure that the input terminals of this LSI do not go into the Hi-Z state after the power has been switched ON. When the built-in LCD drive power supply circuit of the ML9050/9051 is not used, it is necessary that $\overline{RES}$ = "L" when the external LCD drive power supply goes ON. During the period when $\overline{RES}$ = "L", although the oscillator circuit is operating, the display timing generator would have stopped and the pins CL, FR, FRS, and $\overline{DOF}$ would have been tied to the "H" level. There is no effect on the pins D0 to D7.

COMMANDS

MPU Interface

MPU	Read mode	Write mode
80-Series	Pin $\overline{RD}$ = "L"	Pin $\overline{WR}$ = "L"
68-Series	Pin R/$\overline{W}$ = "H" Pin E = "H"	Pin R/$\overline{W}$ = "L" Pin E = "H"

In the case of the 80-series MPU interface, a command is started by inputting a Low pulse on the $\overline{RD}$ pin or the $\overline{WR}$ pin.
In the case of the 68-series MPU interface, a command is started by inputting a High pulse on the E pin.

Description of commands

• Display ON/OFF (Write)
This is the command for controlling the turning on or off the LCD panel. The LCD display is turned on when a "1" is written in bit D0 and is turned off when a "0" is written in this bit.

	A0	D7	D6	D5	D4	D3	D2	D1	D0
Display ON	0	1	0	1	0	1	1	1	1
Display OFF	0								0

• Display start line set (Write)
This command specifies the display starting line address in the display data RAM.
Normally, the topmost line in the display is specified using the display start line set command. It is possible to scroll the display screen by dynamically changing the address using the display start line set command.

Line address	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	0	0	0	0
1				0	0	0	0	0	1
2				0	0	0	0	1	0
⋮				⋮	⋮	⋮	⋮	⋮	⋮
62				1	1	1	1	1	0
63				1	1	1	1	1	1

• Page address set (Write)

This command specifies the page address which corresponds to the lower address when accessing the display data RAM from the MPU side.

It is possible to access any required bit in the display data RAM by specifying the page address and the column address.

Page address	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	1	0	0	0	0
1						0	0	0	1
2						0	0	1	0
⋮						⋮	⋮	⋮	⋮
7						0	1	1	1
8						1	0	0	0

• Column address set (Write)

This command specifies the column address of the display data RAM. The column address is specified by successively writing the upper 4 bits and the lower 4 bits. Since the column address is automatically incremented (by +1) every time the display data RAM is accessed, the MPU can read or write the display data continuously. The incrementing of the column address is stopped at the address 83H.

	A0	D7	D6	D5	D4	D3	D2	D1	D0
Upper bits	0	0	0	0	1	a7	a6	a5	a4
Lower bits					0	a3	a2	a1	a0

Column address	a7	a6	a5	a4	a3	a2	a1	a0
0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
130	1	0	0	0	0	0	1	0
131	1	0	0	0	0	0	1	1

• Status read (Read)

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY	When BUSY is '1', it indicates that the internal operations are being made or the LSI is being reset. Although no command is accepted until BUSY becomes '0', there is no need to check this bit if the cycle time can be satisfied.
ADC	This bit indicates the relationship between the column address and the segment driver. 0: SEG0 → SEG131; column address 0H → 83H 1: SEG131 → SEG0; column address 0H → 83H (Opposite to the polarity of the ADC command.)
ON/OFF	This bit indicates the ON/OFF state of the display. (Opposite to the polarity of the display ON/OFF command.) 0: Display ON 1: Display OFF
RESET	This bit indicates that the LSI is being reset due to the $\overline{RES}$ signal or the reset command. 0: Operating state 1: Being reset

• Display data write (Write)

This command writes an 8-bit data at the specified address of the display data RAM. Since the column address is automatically incremented (by +1) after writing the data, the MPU can write successive display data to the display data RAM.

A0	D7	D6	D5	D4	D3	D2	D1	D0
1	Write data							

• Display data read (Read)

This command read the 8-bit data from the specified address of the display data RAM. Since the column address is automatically incremented (by +1) after reading the data, the MPU can read successive display data from the display data RAM. Further, one dummy read operation is necessary immediately after setting the column data. The display data cannot be read out when the serial interface is being used.

A0	D7	D6	D5	D4	D3	D2	D1	D0
1	Read data							

• ADC Select (segment driver direction select) (Write)
Using this command it is possible to reverse the relationship of correspondence between the column address of the display data RAM and the segment driver output. It is possible to reverse the sequence of the segment driver output pin by the command.

	A0	D7	D6	D5	D4	D3	D2	D1	D0
Forward	0	1	0	1	0	0	0	0	0
Reverse									1

• Normal/reverse display mode (Write)
It is possible to toggle the display on and off condition without changing the contents of the display data RAM. In this case, the contents of the display data RAM will be retained.

	A0	D7	D6	D5	D4	D3	D2	D1	D0	RAM Data
Forward	0	1	0	1	0	0	1	1	0	LCD ON Voltage when "H"
Reverse									1	LCD ON Voltage when "L"

• Display all-on ON/OFF (Write)
Using this command, it is possible to forcibly turn ON all the dots in the display irrespective of the contents of the display data RAM. In this case, the contents of the display data RAM will be retained.
This command is given priority over the Normal/reverse display mode command.

	A0	D7	D6	D5	D4	D3	D2	D1	D0
Normal display state	0	1	0	1	0	0	1	0	0
All-on display									1

The power save mode will be entered into when the Display all-on ON command is executed in the display OFF condition.

• LCD Bias set (Write)
This command is used for selecting the bias ratio of the voltage necessary for driving the LCD device or panel.

ML9050	ML9051	A0	D7	D6	D5	D4	D3	D2	D1	D0
1/9 Bias	1/8 Bias	0	1	0	1	0	0	0	1	0
1/7 Bias	1/6 Bias									1

• Read-modify-write (Write)

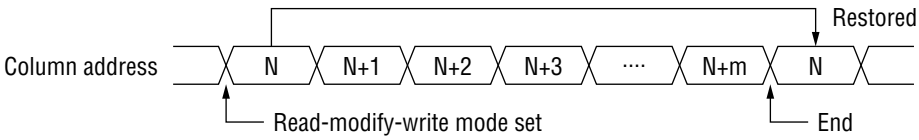
This command is used in combination with the End command. When this command is issued once, the column address is not changed when the Display data read command is issued, but is incremented (by +1) only when the Display data write command is issued. This condition is maintained until the End command is issued. When the End command is issued, the column address is restored to the address that was effective at the time the Read-modify-write command was issued last. Using this function, it is possible to reduce the overhead on the MPU when repeatedly changing the data in special display area such as a blinking cursor.

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	0	0	0	0	0

• End (Write)

This command releases the read-modify-write mode and restores the column address to the value at the beginning of the mode.

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	0	1	1	1	0



• Reset (Write)

This command initializes the display start line number, column address, page address, common output state, voltage V1 adjustment internal resistor ratio, electronic potentiometer function, and the static indicator function, and also releases the read-modify-write mode or the test mode. This command does not affect the contents of the display data RAM.

The reset operation is made after issuing the reset command.

The initialization after switching on the power is carried out by the reset signal input to the $\overline{RES}$ pin.

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	0	0	0	1	0

• Common output state select (Write)

This command is used for selecting the scanning direction of the COM output pins.

	ML9050	ML9051	A0	D7	D6	D5	D4	D3	D2	D1	D0
Forward	COM0 → COM63	COM0 → COM47	0	1	1	0	0	0	*	*	*
Reverse	COM63 → COM0	COM47 → COM0						1	*	*	*

*: Invalid bits

• Power control set (Write)
This command set the functions of the power supply circuits.

ML9050/9051	A0	D7	D6	D5	D4	D3	D2	D1	D0
Voltage multiplier circuit: OFF	0	0	0	1	0	1	0		
Voltage multiplier circuit: ON							1		
Voltage adjustment circuit: OFF								0	
Voltage adjustment circuit: ON								1	
Voltage follower circuits: OFF									0
Voltage follower circuits: ON									1

• Voltage V1 adjustment internal resistor ratio set
This command sets the ratios of the internal resistors for adjusting the voltage V1.

Resistor ratio	A0	D7	D6	D5	D4	D3	D2	D1	D0
Small	0	0	0	1	0	0	0	0	0
							0	0	1
							0	1	0
⋮							⋮	⋮	⋮
							1	1	0
Large							1	1	1

• Electronic potentiometer (2-Byte command)
This command is used for controlling the LCD drive voltage V1 output by the voltage adjustment circuit of the internal LCD power supply and for adjusting the intensity of the LCD display.
This is a two-byte command consisting of the Electronic potentiometer mode set command and the Electronic potentiometer register set command, both of which should always be issued successively as a pair.

• Electronic potentiometer mode set (Write)
When this command is issued, the electronic potentiometer register set command becomes effective.
Once the electronic potentiometer mode is set, it is not possible to issue any command other than the Electronic potentiometer register set command. This condition is released after data has been set in the register using the Electronic potentiometer register set command.

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	0	1

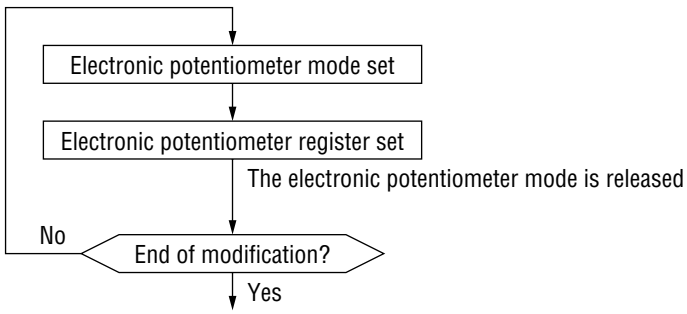
• Electronic potentiometer register set (Write)
By setting a 6-bit data in the electronic potentiometer register using this command, it is possible to set the LCD drive voltage V1 to one of the 64 voltage levels.
The electronic potentiometer mode is released after some data has been set in the electronic potentiometer register using this command.

V1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Small	0	*	*	0	0	0	0	0	1
				0	0	0	0	1	0
				0	0	0	0	1	1
⋮				⋮	⋮	⋮	⋮	⋮	⋮
				1	1	1	1	1	0
Large				1	1	1	1	1	1

*: Invalid bit

Set the data (*, *, 1, 0, 0, 0, 0, 0) when not using the electronic potentiometer function.

Sequence of setting the electronic potentiometer register:



• Static indicator (2-Byte command)
This command is used for controlling the static drive type indicator display.
Static indicator display is controlled only by this command and is independent of all other display control commands. One of the electrodes for driving the static indicator LCD is connected to the pin FR and the other pin is connected to the pin FRS. It is recommended to place the wiring pattern for the electrodes for static indicators far from those of the electrodes for dynamic drive. If these interconnection patterns are too close to each other, they may cause deterioration of the LCD device and the electrodes.

Since the Static indicator ON command is a two-byte command used in combination with the static indictor register set command, these two commands should always be used together.
(The Static indicator OFF command is a single byte command.)

• Static indicator ON/OFF (Write)
When the Static indicator ON command is issued, the Static indicator register set command becomes effective. Once the Static indicator ON command is issued, it is not possible to issue any command other than the Static indicator register set command. This condition is released only after some data is written into the register using the static indicator register set command.

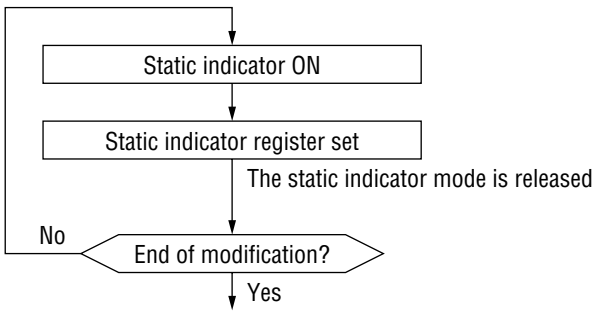
Static indicator	A0	D7	D6	D5	D4	D3	D2	D1	D0
OFF	0	1	0	1	0	1	1	0	0
ON									1

• Static indicator register set (Write)
This command is used to set data in the 2-bit static indicator register thereby setting the blinking state of the static indicator.

Indicator	A0	D7	D6	D5	D4	D3	D2	D1	D0
OFF	0	*	*	*	*	*	*	0	0
ON (Blinking at about 1sec intervals)								0	1
ON (Blinking at about 0.5sec intervals)								1	0
ON (Continuously ON)								1	1

*: Invalid bits

Sequence of setting the static indicator register:



• Line reversal drive (2-byte command) / frame reversal drive selection
It is possible to select the LCD driving method between the line reversal drive method and the frame reversal drive methods. When the line reversal method is selected, the command should be used as a two-byte command in combination with the Line reversal number set command and hence these two commands should always be issued successively.

• LCD Drive method set (Write)

This command sets the LCD driving method.

Once the line reversal method has been set, no command other than the Line reversal number set command is accepted. This state is released only after some data is set in the register using the Line reversal number set command.

The frame reversal set command is a single byte command.

	A0	D7	D6	D5	D4	D3	D2	D1	D0
Frame reversal	0	1	1	0	1	0	*	*	*
Line reversal						1	*	*	*

*: Invalid bits

• Line reversal number set (Write)

When the line reversal method has been set using the LCD drive method set command, it is necessary to set immediately the number of reversed lines.

Number of reversed lines	A0	D7	D6	D5	D4	D3	D2	D1	D0
1	0	*	*	*	0	0	0	0	0
2					0	0	0	0	1
⋮					⋮	⋮	⋮	⋮	⋮
31					1	1	1	1	0
32					1	1	1	1	1

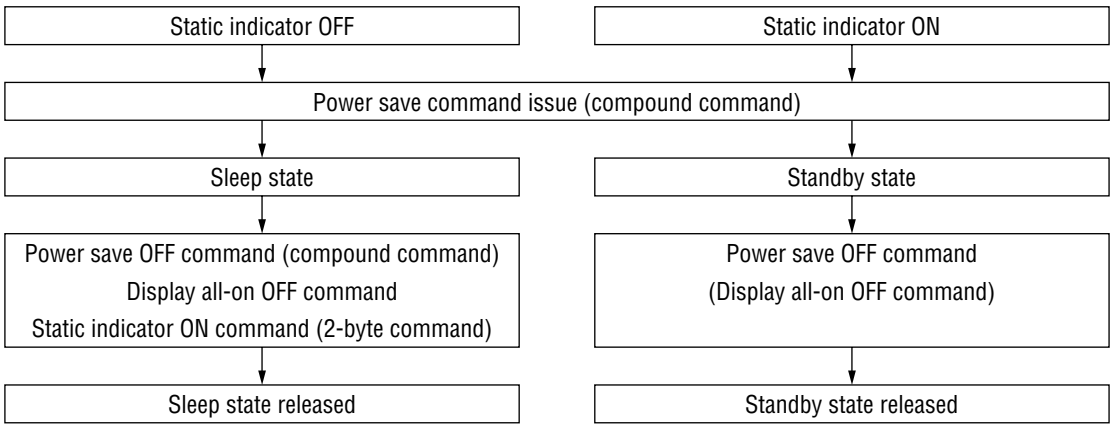
*: Invalid bits

• Power save (Compound command)

The LSI goes into the power save state when the Display all-on ON command is issued when the LSI is in the display OFF state, and it is possible to greatly reduce the current consumption in this state. The power save state is of two types, namely, the sleep state and the standby state, and the LSI goes into the standby state when the static indicator has been made ON.

The display data and the operating mode just before entering the power save mode are retained in both the sleep state and the standby state, and also the MPU can access the display data RAM in these states.

The power save mode is released by issuing the Display all-on OFF command.



• Sleep state

In this state, all the operations of the LCD display system are stopped and it is possible to reduce the current consumption to a level near the idle state current consumption unless there are accesses from the MPU. The internal conditions in the sleep state are as follows:

(1) The oscillator circuit and the LCD power supply are stopped.

(2) All the LCD drive circuits are stopped and the segment and common driver outputs will be at the V_{SS} level.

• Standby state

All operations of the dynamic LCD display section are stopped, only the static display circuits for the indicators operate and hence the current consumption will be the minimum necessary for static drive. The internal conditions in the standby state are as follows:

(1) The power supply circuit for LCD drive is stopped. The oscillator circuit will be operating.

(2) The LCD drive circuits for dynamic display are stopped and the segment and common driver outputs will be at the VSS level. The static display section will be operating.

When a reset command is issued in the standby state, the LSI goes into the sleep state.

• NOP (Write)

This is a No Operation command.

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	0	0	0	1	1

• Test (Write)

This is a command for testing the IC chip. Do not use this command. When the test command is issued by mistake, this state can be released by issuing a NOP command. This command will be ineffective if the TEST0 pin is open or at the "L" level.

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	1	*	*	*	*

*: Invalid bits

LIST OF COMMANDS

No	Operation	Dn	A0	RD	WR	Comment
		7 6 5 4 3 2 1 0				
1	Display OFF	1 0 1 0 1 1 1 0	0	1	0	LCD Display:
	Display ON	1	0	1	0	OFF When D0 = 0 ON When D0 = 1
2	Display start line set	01Address	0	1	0	The display starting line address in the display RAM is set.
3	Page address set	1011Address	0	1	0	The page address in the display RAM is set.
4	Column address set (upper bits)	0001Address (upper)	0	1	0	The upper 4 bits of the column address in the display RAM is set.
	Column address set (lower bits)	0000Address (lower)	0	1	0	The lower 4 bits of the column address in the display RAM is set.
5	Status read	Status0000	0	0	1	The status information is read out from the upper 4 bits.
6	Display data write	Write data	1	1	0	Writes data to the display data RAM.
7	Display data read	Read data	1	0	1	Reads data from the display data RAM.
8	ADC Select Forward	1 0 1 0 0 0 0 0	0	1	0	Correspondence between the display data
	Reverse	1	0	1	0	RAM address and SEG output. Forward when D0 = 0; reverse when D0 = 1
9	Normal display	1 0 1 0 0 1 1 0	0	1	0	Normal or reverse LCD display mode.
	Reverse display	1	0	1	0	Normal mode when D0 = 0; reverse when D0 = 1
10	LCD Normal display	1 0 1 0 0 1 0 0	0	1	0	LCD
	All-on display	1	0	1	0	Normal display when D0 = 0; all-on display when D0 = 1
11	LCD Bias set	1 0 1 0 0 0 1 0	0	1	0	Sets the LCD drive voltage bias ratio.
		1	0	1	0	ML9050: 1/9 when D0 = 0 and 1/7 when D0 = 1 ML9051: 1/8 when D0 = 0 and 1/6 when D0 = 1
12	Read-modify-write	1 1 1 0 0 0 0 0	0	1	0	Incrementing column address During a write: +1; during a read: 0
13	End	1 1 1 0 1 1 1 0	0	1	0	Releases the read-modify-write state.
14	Reset	1 1 1 0 0 0 1 0	0	1	0	Internal reset
15	Common output state select	1 1 0 0 0 * * *	0	1	0	Selects the COM output scanning direction.
		1 * * *	0	1	0	Forward when D3 = 0; reverse when D3 = 1
16	Power control set	0 0 1 0 1 Operating state	0	1	0	Selects the operating state of the internal power supply.
17	Voltage V1 adjustment internal resistor ratio set	0 0 1 0 0 Resistor ratio setting	0	1	0	Selects the internal resistor ratio.

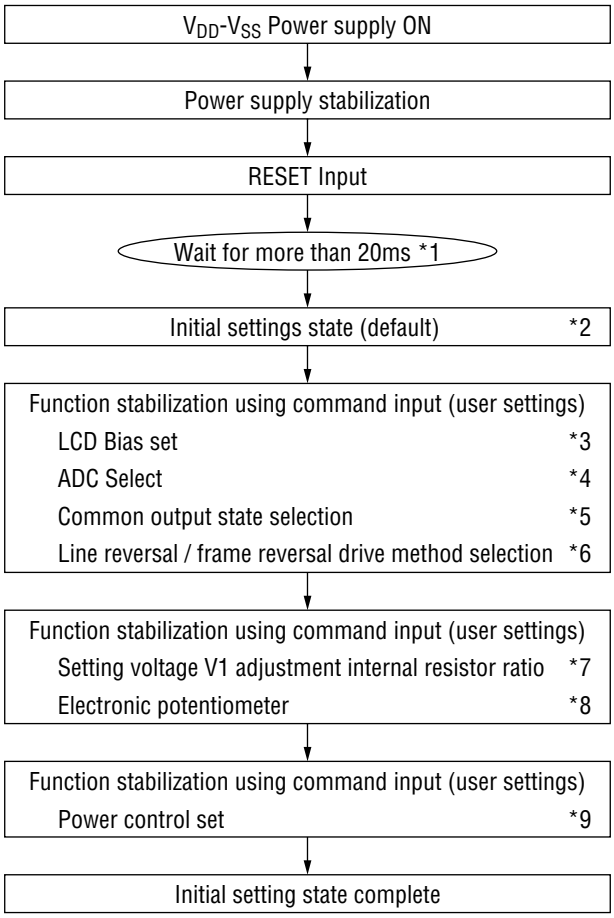
No	Operation	Dn				Comment
		7 6 5 4 3 2 1 0	A0	$\overline{RD}$	$\overline{WR}$	
18	Electronic potentiometer mode set	1 0 0 0 0 0 0 1	0	1	0	Sets the V1 output voltage in the electronic potentiometer register.
	External potentiometer register set	**Electronic potentiometer value	0	1	0	
19	Static indicator	1 0 1 0 1 1 0 0	0	1	0	OFF When D0 = 0
	ON/OFF	1	0	1	0	ON When D0 = 1
	Static indicator register set	******State	0	1	0	Sets the blinking state.
20	LCD Drive method set	1 1 0 1 0 * * *	0	1	0	Frame reversal when D3 = 0.
		1 * * *	0	1	0	Line reversal when D3 = 1.
	Line reversal number set	***Line number	0	1	0	Sets the number of lines ireversed.
21	Power save					Compound command of Display OFF and Display all-on.
22	NOP	1 1 1 0 0 0 1 1	0	1	0	The "No Operation" command.
23	Test	1 1 1 1 * * * *	0	1	0	The command for factory testing of the IC chip.

*: Invalid bits

DESCRIPTION OF COMMANDS

Examples of settings for the instructions (reference examples)

• Initial setting



Notes: Sections to be referred to

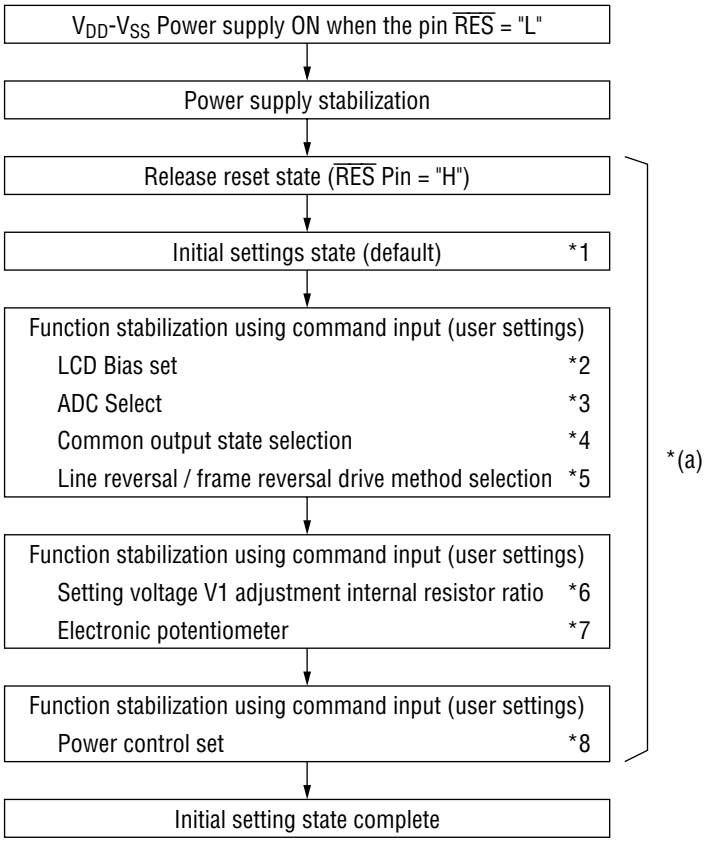
*1: Stabilization time of the internal oscillator
*2: Function description "Reset circuit"
*3: Command description "LCD Bias set"
*4: Command description "ADC Select"
*5: Command description "Common output state select"
*6: Command description "Line reversal/frame reversal drive select"
*7: Function description "Power supply circuit", Command description "Voltage V1 adjustment internal resistor ratio set"
*8: Function description "Power supply circuit", Command description "Electronic potentiometer"
*9: Function description "Power supply circuit", Command description "Power control set"

Examples of settings for the instructions (reference examples)

• Initial setting

Note: After the power is switched ON, this LSI outputs at the LCD drive output pins SEG and COM the V_{SS} potential. If any charge is remaining on the smoothing capacitors connected between the V_{OUT} pin and the pins for the LCD drive voltage outputs (V1 to V5), there may be some abnormality in the display such as temporary blacking out of the display screen when the power is switched ON.
The following procedure is recommended for avoiding such abnormalities at the time the power is switched ON.

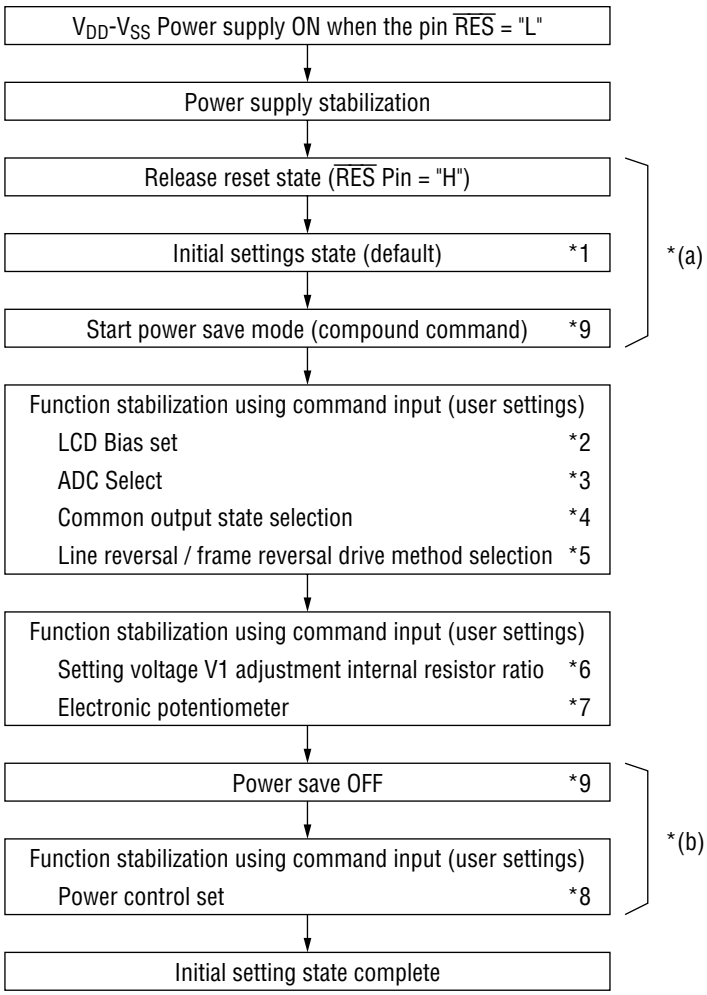
• When using the internal power supply immediately after power-on



*(a): Carry out power control set within 5ms after releasing the reset state.
The 5ms duration changes depending on the panel characteristics and the value of the smoothing capacitor. We recommend verification of operation using an actual unit.

Notes: Sections to be referred to
*1: Function description "Reset circuit"
*2: Command description "LCD Bias set"
*3: Command description "ADC Select"
*4: Command description "Common output state select"
*5: Command description "Line reversal/frame reversal drive select"
*6: Function description "Power supply circuit", Command description "Voltage V1 adjustment internal resistor ratio set"
*7: Function description "Power supply circuit", Command description "Electronic potentiometer"
*8: Function description "Power supply circuit", Command description "Power control set"

• When not using the internal power supply immediately after power-on



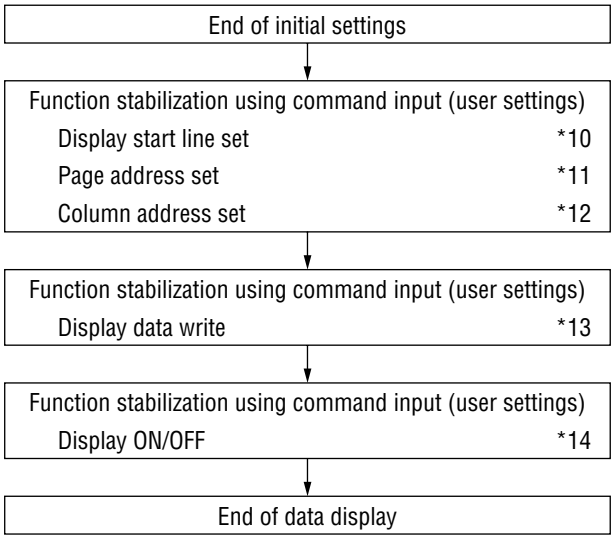
*(a): Enter the power save state within 5ms after releasing the reset state.

*(b): Carry out power control set within 5ms after releasing the power save state.
The 5ms duration in *(a) and *(b) changes depending on the panel characteristics and the value of the smoothing capacitor. We recommend verification of operation using an actual unit.

Notes: Sections to be referred to

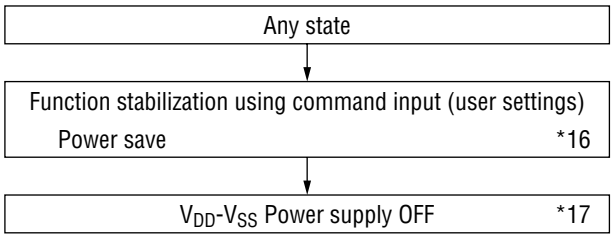
*1: Function description "Reset circuit"
*2: Command description "LCD Bias set"
*3: Command description "ADC Select"
*4: Command description "Common output state select"
*5: Command description "Line reversal/frame reversal drive select"
*6: Function description "Power supply circuit", Command description "Voltage V1 adjustment internal resistor ratio set"
*7: Function description "Power supply circuit", Command description "Electronic potentiometer"
*8: Function description "Power supply circuit", Command description "Power control set"
*9: The power save state can be either the sleep state or the standby state.
Command description "Power save (compound command)"

• Data display



Notes: Sections to be referred to
*10: Command description "Display start line set"
*11: Command description "Page address set"
*12: Command description "Column address set"
*13: Command description "Display data write"
*14: Command description "Display ON/OFF"

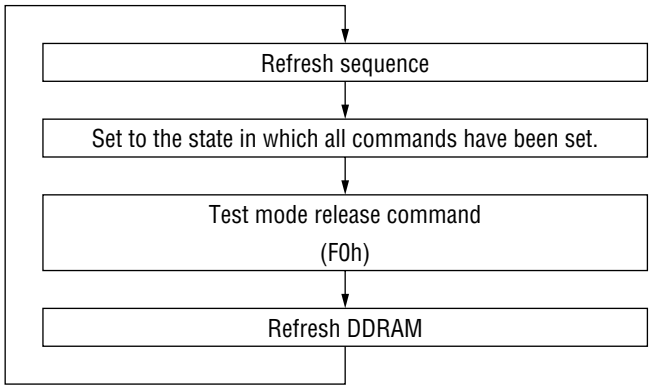
• Power supply OFF (*15)



Notes: Sections to be referred to
*15: The power supply of this LSI is switched OFF after switching OFF the internal power supply. Function description "Power supply circuit"
If the power supply of this LSI is switched OFF when the internal power supply is still ON, since the state of supplying power to the built-in LCD drive circuits continues for a short duration, it may affect the display quality of the LCD panel. Always follow the power supply switching OFF sequence.
*16: Command description "Power save"
*17: Do not enter Reset when switching the power supply OFF.

• Refresh

Use the refresh sequence at regular intervals.



ABSOLUTE MAXIMUM RATINGS

V_{SS} = 0 V

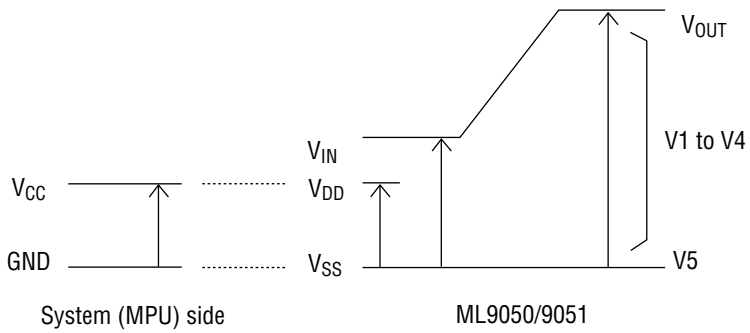
Parameter	Symbol	Condition	Rated value	Unit	Applicable pins
Power supply voltage	V_{DD}	Ta = 25°C	–0.3 to +7	V	V_{DD}, V_{SS}
Bias voltage	V_{BI}	Ta = 25°C	–0.3 to +20	V	V_{OUT}, V1 to V5
Voltage multiplier reference voltage	V_{IN}	6-Times multiplication 7-Times multiplication	–0.3 to +3.3 –0.3 to +2.8	V	VIN, VSS
Input voltage	V_I	Ta = 25°C	–0.3 to VDD+0.3	V	All inputs
Storage temperature range	T_{stg}	TCP Chip	–55 to +100 –55 to +125	°C	—

Ta: Ambient temperature

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Rated value	Unit	Applicable pins
Power supply voltage	V_{DD}	—	1.8 to 5.5	V	V_{DD}, V_{SS}
Bias voltage	V_{BI}	—	6 to 18	V	V_{OUT}, V1 to V5
Voltage multiplier reference voltage	V_{IN}	6-Times multiplication 7-Times multiplication	1.8 to 3 1.8 to 2.5	V	VIN, VSS
Voltage multiplier output voltage	V_{OUT}		18	V	VOUT
Reference voltage	V_{REG0} V_{REG1}	–0.05%/°C *1 –0.2%/°C *1	(3.0)	V	—
Operating temperature range	T_{op}		–40 to +85	°C	—

*1: Ta = 25°C



Note 1: The voltages V_{DD}, V1 to V5, and V_{OUT} are values taking V_{SS} = 0 V as the reference.
Note 2: The highest bias potential is V1 and the lowest is V_{SS}.
Note 3: Always maintain the relationship V1 ≥ V2 ≥ V3 ≥ V4 ≥ V5 ≥ V_{SS} among these voltages.

ELECTRICAL CHARACTERISTICS

DC Characteristics

[Ta = –40 to +85°C]

Parameter		Symbol	Condition	Min	Typ	Max	Unit	Applicable pins
"H" Input voltage "L" Input voltage		V_{IH} V_{IL}		0.8 × VDD VSS		VDD 0.2 × VDD	V	*1
"H" Output voltage "L" Output voltage		V_{OH} V_{OL}	IOH = –0.5mA IOL = 0.5mA	0.8 × VDD VSS		VDD 0.2 × VDD	V	*2
"H" Input current "L" Input current		I_{IH} I_{IL}	VI = VDD VI = 0 V	–1.0 –3.0		1.0 3.0	µA	*3 *4
LCD Driver ON resistance		R_{ON}	Io = ±50 µA			10	kΩ	SEG1 to 132 COM1 to 97
Current consumption		I_{DDS}	Standby			5	µA	V_{DD}
Input pin capacitance		C_{IN}	Ta = 25°C, f = 1MHz		5	8	PF	
Oscillator frequency	Internal oscillation		Ta = 25°C	18	22	26	kHz	*6
	External input		ML9050	18	22	26	kHz	CL*6
	Internal oscillation		Ta = 25°C	27	33	39	kHz	*6
	External input		ML9051	14	17	20	kHz	CL*6

*1: A0, D0 to D5, D6 (SCL), D7 (SI), $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, CLS, CL, FR, M/$\overline{S}$, C86, P/$\overline{S}$, $\overline{DOF}$, $\overline{RES}$, IRS, $\overline{HPM}$ Pins

*2: D0 to D7, FR, FRS, $\overline{DOF}$, CL Pins
$\overline{DOF}$, $\overline{RES}$, IRS, $\overline{HPM}$ Pins

*3: A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, CLS, M/$\overline{S}$, C86, P/$\overline{S}$, $\overline{RES}$, IRS, $\overline{HPM}$ Pins

*4: Applicable to the pins D0 to D5, D6 (SCL), D7 (SI), CL, FR, $\overline{DOF}$ in the high impedance state.

*5: COM1 to COM65 in the ML9050, COM1 to COM65 in the ML9051.

*6: See Table 24 for the relationship between the oscillator frequency and the frame frequency.

Table 24. Relationship among the oscillator frequency (f_{OSC}), display clock frequency (f_{LCDCK}), and LCD frame frequency (f_{FR})

	Parameter	Display clock frequency (f_{LCDCK})	LCD frame frequency (f_{FR})
ML9050	When the internal oscillator is used	$f_{OSC}/4$	$f_{OSC}/4 \times 65$
	When the internal oscillator is not used	External input (f_{LCDCK})	$f_{LCDCK}/260$
ML9051	When the internal oscillator is used	$f_{OSC}/8$	$f_{OSC}/8 \times 49$
	When the internal oscillator is not used	External input (f_{LCDCK})	$f_{LCDCK}/196$

• Operating current consumption value (Ta = 25°C)
(1) During display operation, internal power supply OFF (The current consumption of the entire IC when an external power supply is used)
Display mode: All-white

Model	Symbol	Condition	Rated value			Unit	Remarks
			Min	Typ	Max		
ML9050	I_{DD}	V_{DD} = 5 V, V1-V_{SS} = 11 V		(18)		µA	
		V_{DD} = 3 V, V1-V_{SS} = 11 V		(16)			
ML9051		V_{DD} = 3 V, V1-V_{SS} = 11 V		(13)			
		V_{DD} = 5 V, V1-V_{SS} = 8 V		(11)			
		V_{DD} = 3 V, V1-V_{SS} = 8 V		(9)			

Display mode: Checker pattern

Model	Symbol	Condition	Rated value			Unit	Remarks
			Min	Typ	Max		
ML9050	I_{DD}	V_{DD} = 5 V, V1-V_{SS} = 11 V		TBD		µA	
		V_{DD} = 3 V, V1-V_{SS} = 11 V		TBD			
ML9051		V_{DD} = 3 V, V1-V_{SS} = 11 V		TBD			
		V_{DD} = 5 V, V1-V_{SS} = 8 V		TBD			
		V_{DD} = 3 V, V1-V_{SS} = 8 V		TBD			

(2) During display operation, internal power supply ON
Display mode: All-white

Model	Symbol	Condition		Rated value			Unit	Remarks
				Min	Typ	Max		
ML9050	I_{DD}	V_{DD} = 5 V, 3-times voltage multiplication, V1-V_{SS} = 11 V	Normal mode		(67)		µA	
			High power mode		TBD			
		V_{DD} = 3 V, 4-times voltage multiplication, V1-V_{SS} = 11 V	Normal mode		(81)			
			High power mode		TBD			
ML9051		V_{DD} = 5 V, 3-times voltage multiplication, V1-V_{SS} = 8 V	Normal mode		(35)			
			High power mode		TBD			
		V_{DD} = 3 V, 4-times voltage multiplication, V1-V_{SS} = 8 V	Normal mode		(43)			
			High power mode		TBD			
		V_{DD} = 3 V, 4-times voltage multiplication, V1-V_{SS} = 11 V	Normal mode		(72)			
			High power mode		TBD			

Display mode: Checker pattern

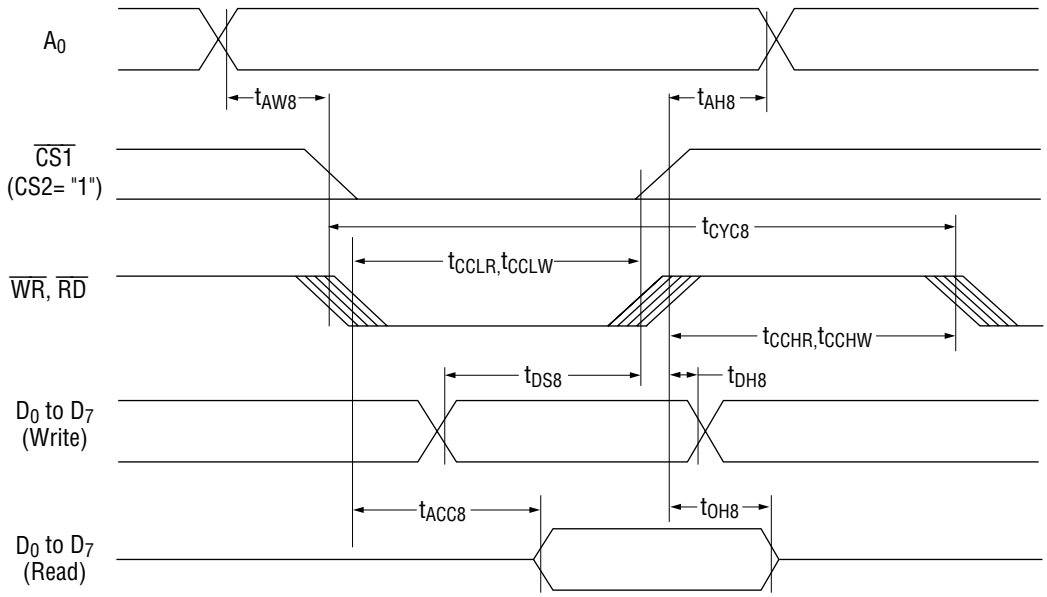
Model	Symbol	Condition		Rated value			Unit	Remarks
				Min	Typ	Max		
ML9050	I_{DD}	V_{DD} = 5 V, 6-times voltage multiplication, V1-V_{SS} = 11 V	Normal mode		TBD		µA	
			High power mode		TBD			
		V_{DD} = 3 V, 7-times voltage multiplication, V1-V_{SS} = 11 V	Normal mode		TBD			
			High power mode		TBD			
ML9051		V_{DD} = 5 V, 6-times voltage multiplication, V1-V_{SS} = 8 V	Normal mode		TBD			
			High power mode		TBD			
		V_{DD} = 3 V, 7-times voltage multiplication, V1-V_{SS} = 8 V	Normal mode		TBD			
			High power mode		TBD			
		V_{DD} = 3 V, 7-times voltage multiplication, V1-V_{SS} = 11 V	Normal mode		TBD			
			High power mode		TBD			

• Power save mode current consumption, VSS = 0 V, VDD = 3 V±10%

Parameter	Symbol	Condition	Rated value			Unit	Remarks
			Min	Typ	Max		
ML9050 Sleep state	I_{DDS1}			(0.1)		µA	
ML9050 Standby state	I_{DDS2}			(4)			
ML9051 Sleep state	I_{DDS1}			(0.1)			
ML9051 Standby state	I_{DDS2}			(4)			

Timing Characteristics

• System bus read/write characteristics 1 (80-series MPU)



[V_{DD} = 4.5 V to 5.5 V, Ta = –40 to +85°C]

Parameter	Applicable pins	Symbol	Condition	Rated value		Unit
				Min	Max	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System cycle time	A0	t_{CYC8}		166	—	
Control L pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		30	—	
Control L pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		70	—	
Control H pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		30	—	
Control H pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		30	—	
Data setup time	D0 to D7	t_{DS8}		30	—	
Data hold time		t_{DH8}		10	—	
$\overline{RD}$ Access time		t_{ACC8}	CL = 100pF	—	70	
Output disable time		t_{OH8}		5	50	

[V_{DD} = 2.7 V to 4.5 V, Ta = –40 to +85°C]

Parameter	Applicable pins	Symbol	Condition	Rated value		Unit
				Min	Max	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System cycle time	A0	t_{CYC8}		300	—	
Control L pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		60	—	
Control L pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		120	—	
Control H pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		60	—	
Control H pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		60	—	
Data setup time	D0 to D7	t_{DS8}		40	—	
Data hold time		t_{DH8}		15	—	
$\overline{RD}$ Access time		t_{ACC8}	CL = 100pF	—	140	
Output disable time		t_{OH8}		10	100	

[V_{DD} = 1.8 V to 2.7 V, Ta = –40 to +85°C]

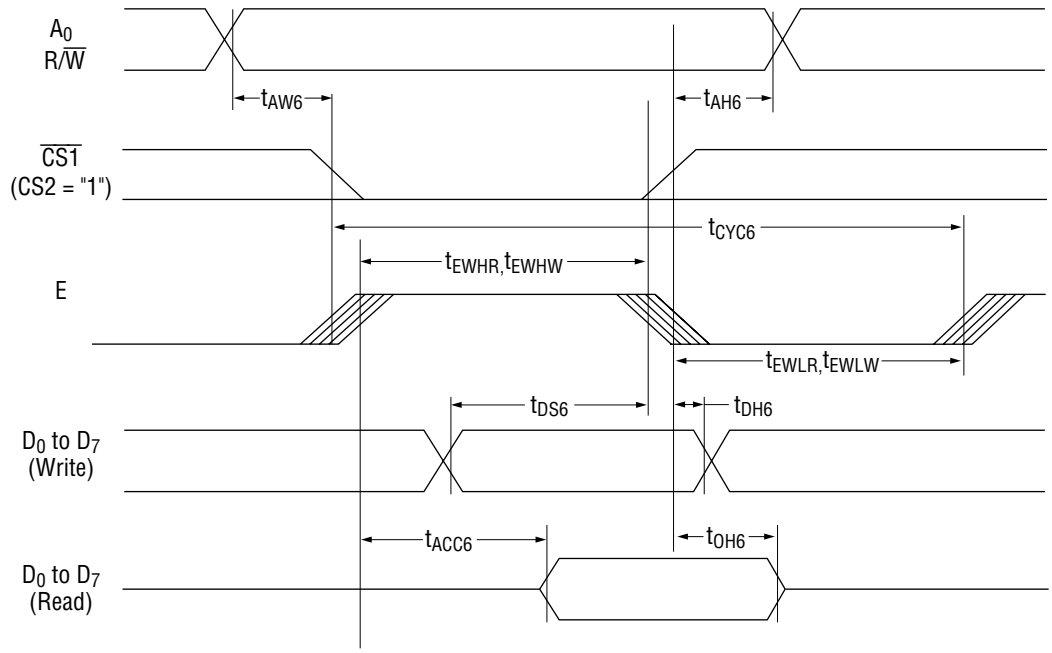
Parameter	Applicable pins	Symbol	Condition	Rated value		Unit
				Min	Max	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System cycle time	A0	t_{CYC8}		1000	—	
Control L pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		120	—	
Control L pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		240	—	
Control H pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		120	—	
Control H pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		120	—	
Data setup time	D0 to D7	t_{DS8}		80	—	
Data hold time		t_{DH8}		30	—	
$\overline{RD}$ Access time		t_{ACC8}	CL = 100pF	—	280	
Output disable time		t_{OH8}		10	200	

Note 1: The input signal rise and fall times are specified as 15ns or less.
When using the system cycle time for fast speed, the specified values are (tr+tf) ≤ (t_{CYC8}-t_{CCLW}-t_{CCHW}) or (tr+tf) ≤ (t_{CYC8}-t_{CCLR}-t_{CCHR}).

Note 2: All timings are specified taking the levels of 20% and 80% of VDD as the reference.

Note 3: The values of t_{CCLW} and t_{CCLR} are specified during the overlapping period of $\overline{CS1}$ at "L" (CS2 = "H") and the "L" levels of $\overline{WR}$ and $\overline{RD}$, respectively.

• System bus read/write characteristics 2 (68-series MPU)



[V_{DD} = 4.5 V to 5.5 V, Ta = –40 to +85°C]

Parameter		Applicable pins	Symbol	Condition	Rated value		Unit
					Min	Max	
Address hold time		A0	t_{AH6}		0	—	ns
Address setup time			t_{AW6}		0	—	
System cycle time		A0	t_{CYC6}		166	—	
Data setup time		D0 to D7	t_{DS6}		30	—	
Data hold time			t_{DH6}		10	—	
Access time			t_{ACC6}	CL = 100pF	—	70	
Output disable time			t_{OH6}		10	50	
Enable H pulse width	Read	E	t_{EWHR}		70	—	
	Write		t_{EWHW}		30	—	
Enable L pulse width	Read	E	t_{EWLR}		30	—	
	Write		t_{EWLW}		30	—	

[V_{DD} = 2.7 V to 4.5 V, Ta = –40 to +85°C]

Parameter		Applicable pins	Symbol	Condition	Rated value		Unit
					Min	Max	
Address hold time		A0	t_{AH6}		0	—	ns
Address setup time			t_{AW6}		0	—	
System cycle time		A0	t_{CYC6}		300	—	
Data setup time		D0 to D7	t_{DS6}		40	—	
Data hold time			t_{DH6}		15	—	
Access time			t_{ACC6}	CL = 100pF	—	140	
Output disable time			t_{OH6}		10	100	
Enable H pulse width	Read	E	t_{EWHR}		120	—	
	Write		t_{EWHW}		60	—	
Enable L pulse width	Read	E	t_{EWLR}		60	—	
	Write		t_{EWLW}		60	—	

[V_{DD} = 1.8 V to 2.7 V, Ta = –40 to +85°C]

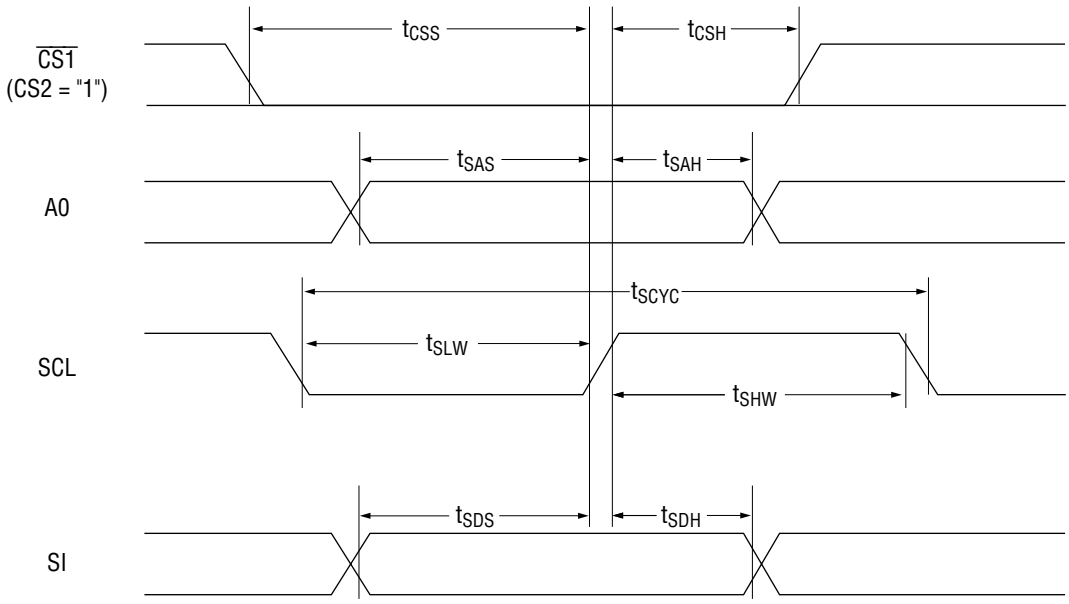
Parameter		Applicable pins	Symbol	Condition	Rated value		Unit
					Min	Max	
Address hold time		A0	t_{AH6}		0	—	ns
Address setup time			t_{AW6}		0	—	
System cycle time		A0	t_{CYC6}		1000	—	
Data setup time		D0 to D7	t_{DS6}		80	—	
Data hold time			t_{DH6}		30	—	
Access time			t_{ACC6}	CL = 100pF	—	280	
Output disable time			t_{OH6}		10	200	
Enable H pulse width	Read	E	t_{EWHR}		240	—	
	Write		t_{EWHW}		120	—	
Enable L pulse width	Read	E	t_{EWLR}		120	—	
	Write		t_{EWLW}		120	—	

Note 1: The input signal rise and fall times are specified as 15ns or less.
When using the system cycle time for fast speed, the specified values are (tr+tf) ≤ (t_{CYC6}-t_{EWLW}-t_{EWHW}) or (tr+tf) ≤ (t_{CYC6}-t_{EWLR}-t_{EWHR}).

Note 2: All timings are specified taking the levels of 20% and 80% of VDD as the reference.

Note 3: The values of t_{EWLW} and t_{EWLR} are specified during the overlapping period of $\overline{CS1}$ at "L" (CS2 = "H") and the "H" level of E.

• Serial interface



[V_{DD} = 4.5 V to 5.5 V, Ta = –40 to +85°C]

Parameter	Applicable pins	Symbol	Condition	Rated value		Unit
				Min	Max	
Serial clock period	SCL	t_{SCYC}		200	—	ns
SCL "H" Pulse width		t_{SHW}		75	—	
SCL "L" Pulse width		t_{SLW}		75	—	
Address setup time	A0	t_{SAS}		50	—	
Address hold time		t_{SAH}		100	—	
Data setup time	SI	t_{SDS}		50	—	
Data hold time		t_{SDH}		50	—	
CS-SCL Time	CS	t_{CSS}		100	—	
		t_{CSH}		100	—	

[V_{DD} = 2.7 V to 4.5 V, Ta = –40 to +85°C]

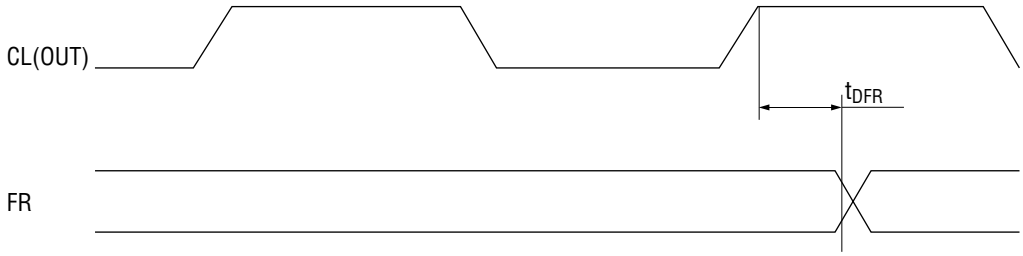
Parameter	Applicable pins	Symbol	Condition	Rated value		Unit
				Min	Max	
Serial clock period	SCL	t_{SCYC}		250	—	ns
SCL "H" Pulse width		t_{SHW}		100	—	
SCL "L" Pulse width		t_{SLW}		100	—	
Address setup time	A0	t_{SAS}		150	—	
Address hold time		t_{SAH}		150	—	
Data setup time	SI	t_{SDS}		100	—	
Data hold time		t_{SDH}		100	—	
CS-SCL Time	CS	t_{CSS}		150	—	
		t_{CSH}		150	—	

[V_{DD} = 1.8 V to 2.7 V, Ta = –40 to +85°C]

Parameter	Applicable pins	Symbol	Condition	Rated value		Unit
				Min	Max	
Serial clock period	SCL	t_{SCYC}		400	—	ns
SCL "H" Pulse width		t_{SHW}		150	—	
SCL "L" Pulse width		t_{SLW}		150	—	
Address setup time	A0	t_{SAS}		250	—	
Address hold time		t_{SAH}		250	—	
Data setup time	SI	t_{SDS}		150	—	
Data hold time		t_{SDH}		150	—	
CS-SCL Time	CS	t_{CSS}		250	—	
		t_{CSH}		250	—	

Note 1: The input signal rise and fall times are specified as 15ns or less.
Note 2: All timings are specified taking the levels of 20% and 80% of V_{DD} as the reference.

• Display control output timing



[V_{DD} = 4.5 V to 5.5 V, Ta = –40 to +85˚C]

Parameter	Applicable pins	Symbol	Condition	Rated value			Unit
				Min	Typ	Max	
FR Delay time	FR	t_{DFR}	CL = 50pF	—	10	40	ns

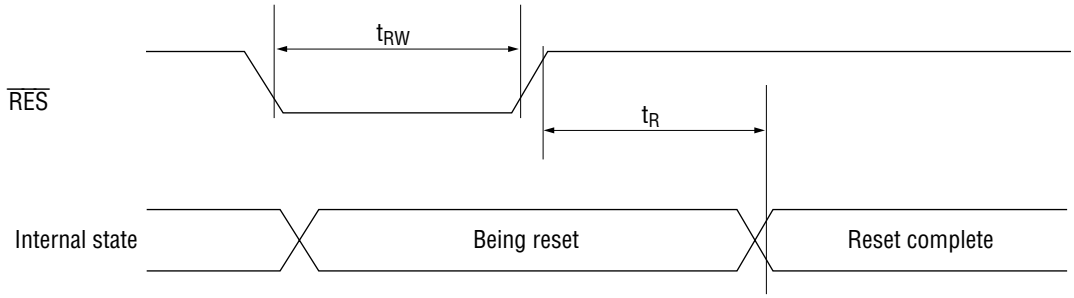
[V_{DD} = 2.7 V to 4.5 V, Ta = –40 to +85˚C]

Parameter	Applicable pins	Symbol	Condition	Rated value			Unit
				Min	Typ	Max	
FR Delay time	FR	t_{DFR}	CL = 50pF	—	20	80	ns

[V_{DD} = 1.8 V to 2.7 V, Ta = –40 to +85˚C]

Parameter	Applicable pins	Symbol	Condition	Rated value			Unit
				Min	Typ	Max	
FR Delay time	FR	t_{DFR}	CL = 50pF	—	50	200	ns

• Reset input timing



[V_{DD} = 4.5 V to 5.5 V, Ta = –40 to +85°C]

Parameter	Applicable pins	Symbol	Condition	Rated value			Unit
				Min	Typ	Max	
Reset time	—	t_R		—	—	0.5	µs
Reset "L" pulse width	$\overline{RES}$	t_{RW}		0.5	—	—	

[V_{DD} = 2.7 V to 4.5 V, Ta = –40 to +85°C]

Parameter	Applicable pins	Symbol	Condition	Rated value			Unit
				Min	Typ	Max	
Reset time	—	t_R		—	—	1	µs
Reset "L" pulse width	$\overline{RES}$	t_{RW}		1	—	—	

[V_{DD} = 1.8 V to 2.7 V, Ta = –40 to +85°C]

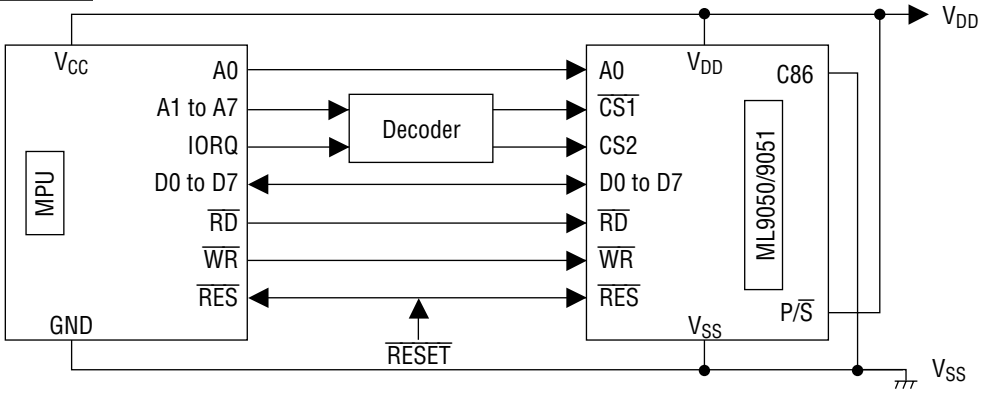
Parameter	Applicable pins	Symbol	Condition	Rated value			Unit
				Min	Typ	Max	
Reset time	—	t_R		—	—	1.5	µs
Reset "L" pulse width	$\overline{RES}$	t_{RW}		1.5	—	—	

Note 1: All timings are specified taking the levels of 20% and 80% of V_{DD} as the reference.

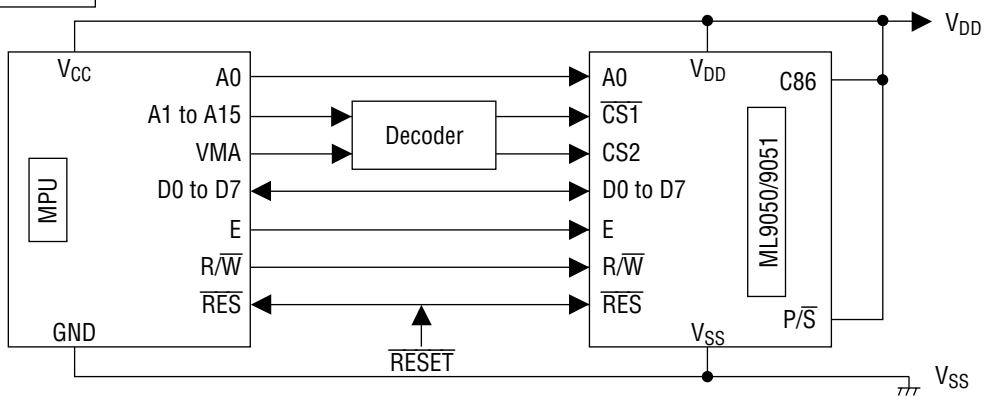
MPU INTERFACE

The ML9050/9051 series ICs can be connected directly to the 80-series and 68-series MPUs. Further, by using the serial interface, it is possible to operate the LSI with a minimum number of signal lines.
In addition, it is possible to expand the display area by using the ML9050/9051 series LSIs in a multiple chip configuration. In this case, it is possible to select the individual LSI to be accessed using the chip select signals.

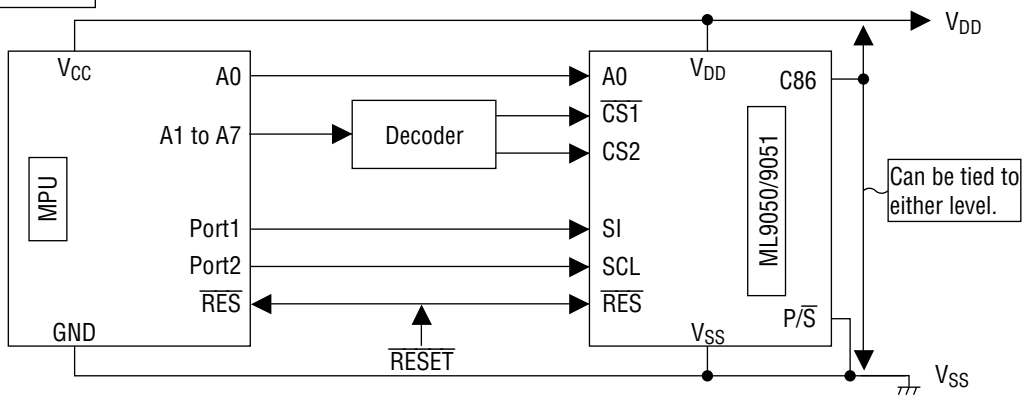
• 80-Series MPU



• 68-Series MPU



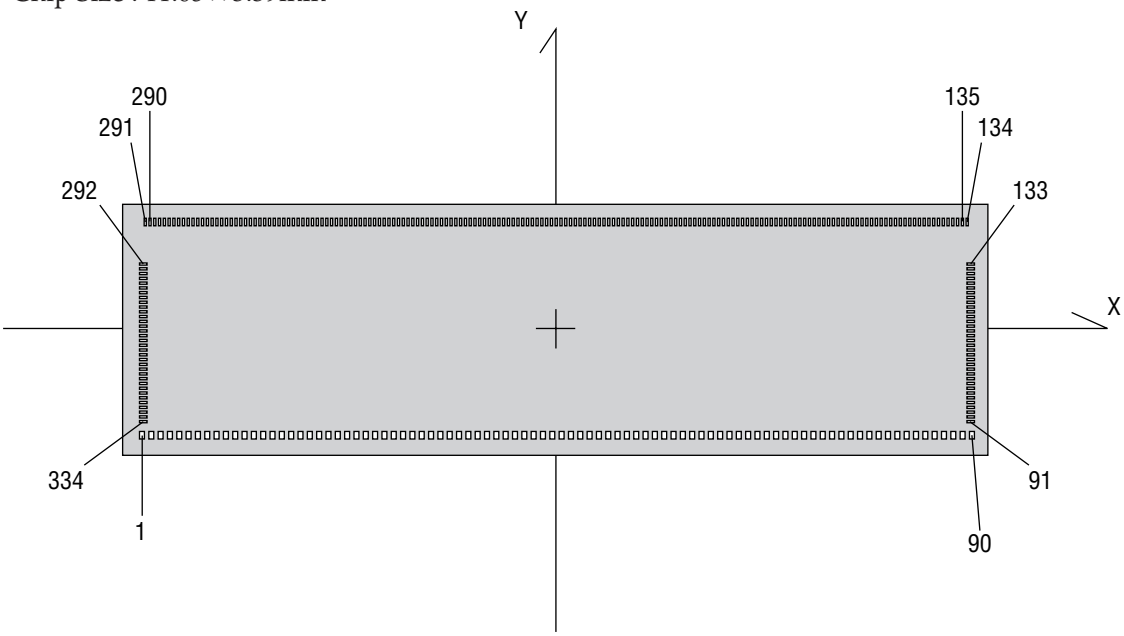
• Serial interface



PAD CONFIGURATION

Pad Layout ; ML9050

Chip Size : 11.05 × 3.39mm



Pad Coordinates

Pad No.	Pad Name	X (μm)	Y (μm)
1	DUMMY	–5000	–1550
2	DUMMY	–4888	–1550
3	DUMMY	–4776	–1550
4	DUMMY	–4664	–1550
5	FRS	–4552	–1550
6	FR	–4440	–1550
7	CL	–4328	–1550
8	$\overline{DOF}$	–4216	–1550
9	TEST0	–4104	–1550
10	GND	–3992	–1550
11	$\overline{CS1}$	–3880	–1550
12	CS2	–3768	–1550
13	V_{DD}	–3656	–1550
14	$\overline{RES}$	–3544	–1550
15	A0	–3432	–1550
16	GND	–3320	–1550
17	$\overline{WR}$	–3208	–1550
18	$\overline{RD}$	–3096	–1550
19	V_{DD}	–2984	–1550
20	DB0	–2872	–1550

Pad No.	Pad Name	X (μm)	Y (μm)
21	DB1	–2760	–1550
22	DB2	–2648	–1550
23	DB3	–2536	–1550
24	DB4	–2424	–1550
25	DB5	–2312	–1550
26	DB6	–2200	–1550
27	DB7	–2088	–1550
28	V_{DD}	–1976	–1550
29	V_{DD}	–1896	–1550
30	V_{DD}	–1816	–1550
31	V_{DD}	–1736	–1550
32	V_{IN}	–1656	–1550
33	V_{IN}	–1576	–1550
34	V_{IN}	–1496	–1550
35	V_{IN}	–1416	–1550
36	GND	–1336	–1550
37	GND	–1256	–1550
38	GND	–1176	–1550
39	V_{OUT}	–1076	–1550
40	V_{OUT}	–951	–1550

Pad No.	Pad Name	X (μm)	Y (μm)
41	VC2+	–826	–1550
42	VC2+	–701	–1550
43	VC4+	–576	–1550
44	VC4+	–451	–1550
45	VC6+	–326	–1550
46	VC6+	–201	–1550
47	VS2–	–76	–1550
48	VS2–	49	–1550
49	VS1–	174	–1550
50	VS1–	299	–1550
51	VC5+	424	–1550
52	VC5+	549	–1550
53	VC3+	674	–1550
54	VC3+	799	–1550
55	VC1+	924	–1550
56	VC1+	1049	–1550
57	GND	1174	–1550
58	GND	1299	–1550
59	VRS	1424	–1550
60	VRS	1549	–1550
61	V_{DD}	1674	–1550
62	V_{DD}	1799	–1550
63	V1	1924	–1550
64	V1	2049	–1550
65	V2	2174	–1550
66	V2	2299	–1550
67	V3	2424	–1550
68	V3	2549	–1550
69	V4	2674	–1550
70	V4	2799	–1550
71	V5	2924	–1550
72	V5	3049	–1550
73	VR	3174	–1550
74	VR	3299	–1550
75	V_{DD}	3424	–1550
76	V_{DD}	3549	–1550
77	TEST1	3674	–1550
78	V_{DD}	3786	–1550
79	MS	3898	–1550
80	CLS	4010	–1550

Pad No.	Pad Name	X (μm)	Y (μm)
81	GND	4122	–1550
82	C86	4234	–1550
83	PS	4346	–1550
84	V_{DD}	4458	–1550
85	HPM	4570	–1550
86	GND	4682	–1550
87	IRS	4794	–1550
88	V_{DD}	4906	–1550
89	DUMMY	5018	–1550
90	DUMMY	5130	–1550
91	DUMMY	5340	–1363.2
92	DUMMY	5340	–1298.2
93	DUMMY	5340	–1233.2
94	DUMMY	5340	–1168.2
95	DUMMY	5340	–1103.2
96	DUMMY	5340	–1038.2
97	DUMMY	5340	–973.2
98	COM31	5340	–908.2
99	COM30	5340	–843.2
100	COM29	5340	–778.2
101	COM28	5340	–713.2
102	COM27	5340	–648.2
103	COM26	5340	–583.2
104	COM25	5340	–518.2
105	COM24	5340	–453.2
106	COM23	5340	–388.2
107	COM22	5340	–323.2
108	COM21	5340	–258.2
109	COM20	5340	–193.2
110	COM19	5340	–128.2
111	COM18	5340	–63.2
112	COM17	5340	1.8
113	COM16	5340	66.8
114	COM15	5340	131.8
115	COM14	5340	196.8
116	COM13	5340	261.8
117	COM12	5340	326.8
118	COM11	5340	391.8
119	COM10	5340	456.8
120	COM9	5340	521.8

Pad No.	Pad Name	X (μm)	Y (μm)
121	COM8	5340	586.8
122	COM7	5340	651.8
123	COM6	5340	716.8
124	COM5	5340	781.8
125	COM4	5340	846.8
126	COM3	5340	911.8
127	COM2	5340	976.8
128	COM1	5340	1041.8
129	COM0	5340	1106.8
130	COMS1	5340	1171.8
131	DUMMY	5340	1236.8
132	DUMMY	5340	1301.8
133	DUMMY	5340	1366.8
134	DUMMY	5037.5	1545
135	DUMMY	4972.5	1545
136	DUMMY	4907.5	1545
137	DUMMY	4842.5	1545
138	DUMMY	4777.5	1545
139	DUMMY	4712.5	1545
140	DUMMY	4647.5	1545
141	DUMMY	4582.5	1545
142	DUMMY	4517.5	1545
143	DUMMY	4452.5	1545
144	DUMMY	4387.5	1545
145	DUMMY	4322.5	1545
146	SEG0	4257.5	1545
147	SEG1	4192.5	1545
148	SEG2	4127.5	1545
149	SEG3	4062.5	1545
150	SEG4	3997.5	1545
151	SEG5	3932.5	1545
152	SEG6	3867.5	1545
153	SEG7	3802.5	1545
154	SEG8	3737.5	1545
155	SEG9	3672.5	1545
156	SEG10	3607.5	1545
157	SEG11	3542.5	1545
158	SEG12	3477.5	1545
159	SEG13	3412.5	1545
160	SEG14	3347.5	1545

Pad No.	Pad Name	X (μm)	Y (μm)
161	SEG15	3282.5	1545
162	SEG16	3217.5	1545
163	SEG17	3152.5	1545
164	SEG18	3087.5	1545
165	SEG19	3022.5	1545
166	SEG20	2957.5	1545
167	SEG21	2892.5	1545
168	SEG22	2827.5	1545
169	SEG23	2762.5	1545
170	SEG24	2697.5	1545
171	SEG25	2632.5	1545
172	SEG26	2567.5	1545
173	SEG27	2502.5	1545
174	SEG28	2437.5	1545
175	SEG29	2372.5	1545
176	SEG30	2307.5	1545
177	SEG31	2242.5	1545
178	SEG32	2177.5	1545
179	SEG33	2112.5	1545
180	SEG34	2047.5	1545
181	SEG35	1982.5	1545
182	SEG36	1917.5	1545
183	SEG37	1852.5	1545
184	SEG38	1787.5	1545
185	SEG39	1722.5	1545
186	SEG40	1657.5	1545
187	SEG41	1592.5	1545
188	SEG42	1527.5	1545
189	SEG43	1462.5	1545
190	SEG44	1397.5	1545
191	SEG45	1332.5	1545
192	SEG46	1267.5	1545
193	SEG47	1202.5	1545
194	SEG48	1137.5	1545
195	SEG49	1072.5	1545
196	SEG50	1007.5	1545
197	SEG51	942.5	1545
198	SEG52	877.5	1545
199	SEG53	812.5	1545
200	SEG54	747.5	1545

Pad No.	Pad Name	X (μm)	Y (μm)
201	SEG55	682.5	1545
202	SEG56	617.5	1545
203	SEG57	552.5	1545
204	SEG58	487.5	1545
205	SEG59	422.5	1545
206	SEG60	357.5	1545
207	SEG61	292.5	1545
208	SEG62	227.5	1545
209	SEG63	162.5	1545
210	SEG64	97.5	1545
211	SEG65	32.5	1545
212	SEG66	–32.5	1545
213	SEG67	–97.5	1545
214	SEG68	–162.5	1545
215	SEG69	–227.5	1545
216	SEG70	–292.5	1545
217	SEG71	–357.5	1545
218	SEG72	–422.5	1545
219	SEG73	–487.5	1545
220	SEG74	–552.5	1545
221	SEG75	–617.5	1545
222	SEG76	–682.5	1545
223	SEG77	–747.5	1545
224	SEG78	–812.5	1545
225	SEG79	–877.5	1545
226	SEG80	–942.5	1545
227	SEG81	–1007.5	1545
228	SEG82	–1072.5	1545
229	SEG83	–1137.5	1545
230	SEG84	–1202.5	1545
231	SEG85	–1267.5	1545
232	SEG86	–1332.5	1545
233	SEG87	–1397.5	1545
234	SEG88	–1462.5	1545
235	SEG89	–1527.5	1545
236	SEG90	–1592.5	1545
237	SEG91	–1657.5	1545
238	SEG92	–1722.5	1545
239	SEG93	–1787.5	1545
240	SEG94	–1852.5	1545
241	SEG95	–1917.5	1545
242	SEG96	–1982.5	1545
243	SEG97	–2047.5	1545
244	SEG98	–2112.5	1545
245	SEG99	–2177.5	1545
246	SEG100	–2242.5	1545
247	SEG101	–2307.5	1545
248	SEG102	–2372.5	1545
249	SEG103	–2437.5	1545
250	SEG104	–2502.5	1545
251	SEG105	–2567.5	1545
252	SEG106	–2632.5	1545
253	SEG107	–2697.5	1545
254	SEG108	–2762.5	1545
255	SEG109	–2827.5	1545
256	SEG110	–2892.5	1545
257	SEG111	–2957.5	1545
258	SEG112	–3022.5	1545
259	SEG113	–3087.5	1545
260	SEG114	–3152.5	1545
261	SEG115	–3217.5	1545
262	SEG116	–3282.5	1545
263	SEG117	–3347.5	1545
264	SEG118	–3412.5	1545
265	SEG119	–3477.5	1545
266	SEG120	–3542.5	1545
267	SEG121	–3607.5	1545
268	SEG122	–3672.5	1545
269	SEG123	–3737.5	1545
270	SEG124	–3802.5	1545
271	SEG125	–3867.5	1545
272	SEG126	–3932.5	1545
273	SEG127	–3997.5	1545
274	SEG128	–4062.5	1545
275	SEG129	–4127.5	1545
276	SEG130	–4192.5	1545
277	SEG131	–4257.5	1545
278	DUMMY	–4322.5	1545
279	DUMMY	–4387.5	1545
280	DUMMY	–4452.5	1545

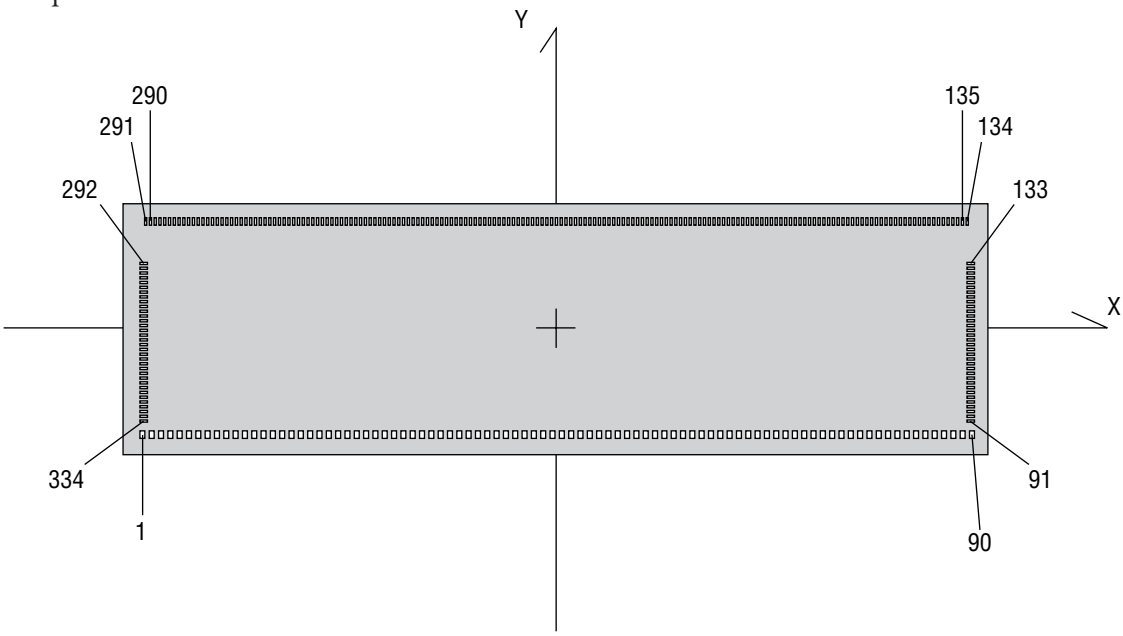
Pad No.	Pad Name	X (μm)	Y (μm)
281	DUMMY	–4517.5	1545
282	DUMMY	–4582.5	1545
283	DUMMY	–4647.5	1545
284	DUMMY	–4712.5	1545
285	DUMMY	–4777.5	1545
286	DUMMY	–4842.5	1545
287	DUMMY	–4907.5	1545
288	DUMMY	–4972.5	1545
289	DUMMY	–5037.5	1545
290	DUMMY	–5102.5	1545
291	DUMMY	–5167.5	1545
292	DUMMY	–5340	1366.8
293	DUMMY	–5340	1301.8
294	DUMMY	–5340	1236.8
295	COM32	–5340	1171.8
296	COM33	–5340	1106.8
297	COM34	–5340	1041.8
298	COM35	–5340	976.8
299	COM36	–5340	911.8
300	COM37	–5340	846.8
301	COM38	–5340	781.8
302	COM39	–5340	716.8
303	COM40	–5340	651.8
304	COM41	–5340	586.8
305	COM42	–5340	521.8
306	COM43	–5340	456.8
307	COM44	–5340	391.8

Pad No.	Pad Name	X (μm)	Y (μm)
308	COM45	–5340	326.8
309	COM46	–5340	261.8
310	COM47	–5340	196.8
311	COM48	–5340	131.8
312	COM49	–5340	66.8
313	COM50	–5340	1.8
314	COM51	–5340	–63.2
315	COM52	–5340	–128.2
316	COM53	–5340	–193.2
317	COM54	–5340	–258.2
318	COM55	–5340	–323.2
319	COM56	–5340	–388.2
320	COM57	–5340	–453.2
321	COM58	–5340	–518.2
322	COM59	–5340	–583.2
323	COM60	–5340	–648.2
324	COM61	–5340	–713.2
325	COM62	–5340	–778.2
326	COM63	–5340	–843.2
327	COMS0	–5340	–908.2
328	DUMMY	–5340	–973.2
329	DUMMY	–5340	–1038.2
330	DUMMY	–5340	–1103.2
331	DUMMY	–5340	–1168.2
332	DUMMY	–5340	–1233.2
333	DUMMY	–5340	–1298.2
334	DUMMY	–5340	–1363.2

PAD CONFIGURATION

Pad Layout ; ML9051

Chip Size : 11.05 × 3.39mm



Pad Coordinates

Pad No.	Pad Name	X (μm)	Y (μm)
1	DUMMY	–5000	–1550
2	DUMMY	–4888	–1550
3	DUMMY	–4776	–1550
4	DUMMY	–4664	–1550
5	FRS	–4552	–1550
6	FR	–4440	–1550
7	CL	–4328	–1550
8	$\overline{DOF}$	–4216	–1550
9	TEST0	–4104	–1550
10	GND	–3992	–1550
11	$\overline{CS1}$	–3880	–1550
12	CS2	–3768	–1550
13	V_{DD}	–3656	–1550
14	$\overline{RES}$	–3544	–1550
15	A0	–3432	–1550
16	GND	–3320	–1550
17	$\overline{WR}$	–3208	–1550
18	$\overline{RD}$	–3096	–1550
19	V_{DD}	–2984	–1550
20	DB0	–2872	–1550

Pad No.	Pad Name	X (μm)	Y (μm)
21	DB1	–2760	–1550
22	DB2	–2648	–1550
23	DB3	–2536	–1550
24	DB4	–2424	–1550
25	DB5	–2312	–1550
26	DB6	–2200	–1550
27	DB7	–2088	–1550
28	V_{DD}	–1976	–1550
29	V_{DD}	–1896	–1550
30	V_{DD}	–1816	–1550
31	V_{DD}	–1736	–1550
32	V_{IN}	–1656	–1550
33	V_{IN}	–1576	–1550
34	V_{IN}	–1496	–1550
35	V_{IN}	–1416	–1550
36	GND	–1336	–1550
37	GND	–1256	–1550
38	GND	–1176	–1550
39	V_{OUT}	–1076	–1550
40	V_{OUT}	–951	–1550

Pad No.	Pad Name	X (μm)	Y (μm)
41	VC2+	–826	–1550
42	VC2+	–701	–1550
43	VC4+	–576	–1550
44	VC4+	–451	–1550
45	VC6+	–326	–1550
46	VC6+	–201	–1550
47	VS2–	–76	–1550
48	VS2–	49	–1550
49	VS1–	174	–1550
50	VS1–	299	–1550
51	VC5+	424	–1550
52	VC5+	549	–1550
53	VC3+	674	–1550
54	VC3+	799	–1550
55	VC1+	924	–1550
56	VC1+	1049	–1550
57	GND	1174	–1550
58	GND	1299	–1550
59	VRS	1424	–1550
60	VRS	1549	–1550
61	V_{DD}	1674	–1550
62	V_{DD}	1799	–1550
63	V1	1924	–1550
64	V1	2049	–1550
65	V2	2174	–1550
66	V2	2299	–1550
67	V3	2424	–1550
68	V3	2549	–1550
69	V4	2674	–1550
70	V4	2799	–1550
71	V5	2924	–1550
72	V5	3049	–1550
73	VR	3174	–1550
74	VR	3299	–1550
75	V_{DD}	3424	–1550
76	V_{DD}	3549	–1550
77	TEST1	3674	–1550
78	V_{DD}	3786	–1550
79	MS	3898	–1550
80	CLS	4010	–1550

Pad No.	Pad Name	X (μm)	Y (μm)
81	GND	4122	–1550
82	C86	4234	–1550
83	PS	4346	–1550
84	V_{DD}	4458	–1550
85	HPM	4570	–1550
86	GND	4682	–1550
87	IRS	4794	–1550
88	V_{DD}	4906	–1550
89	DUMMY	5018	–1550
90	DUMMY	5130	–1550
91	DUMMY	5340	–1363.2
92	DUMMY	5340	–1298.2
93	DUMMY	5340	–1233.2
94	DUMMY	5340	–1168.2
95	DUMMY	5340	–1103.2
96	DUMMY	5340	–1038.2
97	DUMMY	5340	–973.2
98	DUMMY	5340	–908.2
99	DUMMY	5340	–843.2
100	DUMMY	5340	–778.2
101	DUMMY	5340	–713.2
102	DUMMY	5340	–648.2
103	DUMMY	5340	–583.2
104	DUMMY	5340	–518.2
105	DUMMY	5340	–453.2
106	COM23	5340	–388.2
107	COM22	5340	–323.2
108	COM21	5340	–258.2
109	COM20	5340	–193.2
110	COM19	5340	–128.2
111	COM18	5340	–63.2
112	COM17	5340	1.8
113	COM16	5340	66.8
114	COM15	5340	131.8
115	COM14	5340	196.8
116	COM13	5340	261.8
117	COM12	5340	326.8
118	COM11	5340	391.8
119	COM10	5340	456.8
120	COM9	5340	521.8

Pad No.	Pad Name	X (μm)	Y (μm)
121	COM8	5340	586.8
122	COM7	5340	651.8
123	COM6	5340	716.8
124	COM5	5340	781.8
125	COM4	5340	846.8
126	COM3	5340	911.8
127	COM2	5340	976.8
128	COM1	5340	1041.8
129	COM0	5340	1106.8
130	COMS1	5340	1171.8
131	DUMMY	5340	1236.8
132	DUMMY	5340	1301.8
133	DUMMY	5340	1366.8
134	DUMMY	5037.5	1545
135	DUMMY	4972.5	1545
136	DUMMY	4907.5	1545
137	DUMMY	4842.5	1545
138	DUMMY	4777.5	1545
139	DUMMY	4712.5	1545
140	DUMMY	4647.5	1545
141	DUMMY	4582.5	1545
142	DUMMY	4517.5	1545
143	DUMMY	4452.5	1545
144	DUMMY	4387.5	1545
145	DUMMY	4322.5	1545
146	SEG0	4257.5	1545
147	SEG1	4192.5	1545
148	SEG2	4127.5	1545
149	SEG3	4062.5	1545
150	SEG4	3997.5	1545
151	SEG5	3932.5	1545
152	SEG6	3867.5	1545
153	SEG7	3802.5	1545
154	SEG8	3737.5	1545
155	SEG9	3672.5	1545
156	SEG10	3607.5	1545
157	SEG11	3542.5	1545
158	SEG12	3477.5	1545
159	SEG13	3412.5	1545
160	SEG14	3347.5	1545

Pad No.	Pad Name	X (μm)	Y (μm)
161	SEG15	3282.5	1545
162	SEG16	3217.5	1545
163	SEG17	3152.5	1545
164	SEG18	3087.5	1545
165	SEG19	3022.5	1545
166	SEG20	2957.5	1545
167	SEG21	2892.5	1545
168	SEG22	2827.5	1545
169	SEG23	2762.5	1545
170	SEG24	2697.5	1545
171	SEG25	2632.5	1545
172	SEG26	2567.5	1545
173	SEG27	2502.5	1545
174	SEG28	2437.5	1545
175	SEG29	2372.5	1545
176	SEG30	2307.5	1545
177	SEG31	2242.5	1545
178	SEG32	2177.5	1545
179	SEG33	2112.5	1545
180	SEG34	2047.5	1545
181	SEG35	1982.5	1545
182	SEG36	1917.5	1545
183	SEG37	1852.5	1545
184	SEG38	1787.5	1545
185	SEG39	1722.5	1545
186	SEG40	1657.5	1545
187	SEG41	1592.5	1545
188	SEG42	1527.5	1545
189	SEG43	1462.5	1545
190	SEG44	1397.5	1545
191	SEG45	1332.5	1545
192	SEG46	1267.5	1545
193	SEG47	1202.5	1545
194	SEG48	1137.5	1545
195	SEG49	1072.5	1545
196	SEG50	1007.5	1545
197	SEG51	942.5	1545
198	SEG52	877.5	1545
199	SEG53	812.5	1545
200	SEG54	747.5	1545

Pad No.	Pad Name	X (μm)	Y (μm)
201	SEG55	682.5	1545
202	SEG56	617.5	1545
203	SEG57	552.5	1545
204	SEG58	487.5	1545
205	SEG59	422.5	1545
206	SEG60	357.5	1545
207	SEG61	292.5	1545
208	SEG62	227.5	1545
209	SEG63	162.5	1545
210	SEG64	97.5	1545
211	SEG65	32.5	1545
212	SEG66	–32.5	1545
213	SEG67	–97.5	1545
214	SEG68	–162.5	1545
215	SEG69	–227.5	1545
216	SEG70	–292.5	1545
217	SEG71	–357.5	1545
218	SEG72	–422.5	1545
219	SEG73	–487.5	1545
220	SEG74	–552.5	1545
221	SEG75	–617.5	1545
222	SEG76	–682.5	1545
223	SEG77	–747.5	1545
224	SEG78	–812.5	1545
225	SEG79	–877.5	1545
226	SEG80	–942.5	1545
227	SEG81	–1007.5	1545
228	SEG82	–1072.5	1545
229	SEG83	–1137.5	1545
230	SEG84	–1202.5	1545
231	SEG85	–1267.5	1545
232	SEG86	–1332.5	1545
233	SEG87	–1397.5	1545
234	SEG88	–1462.5	1545
235	SEG89	–1527.5	1545
236	SEG90	–1592.5	1545
237	SEG91	–1657.5	1545
238	SEG92	–1722.5	1545
239	SEG93	–1787.5	1545
240	SEG94	–1852.5	1545
241	SEG95	–1917.5	1545
242	SEG96	–1982.5	1545
243	SEG97	–2047.5	1545
244	SEG98	–2112.5	1545
245	SEG99	–2177.5	1545
246	SEG100	–2242.5	1545
247	SEG101	–2307.5	1545
248	SEG102	–2372.5	1545
249	SEG103	–2437.5	1545
250	SEG104	–2502.5	1545
251	SEG105	–2567.5	1545
252	SEG106	–2632.5	1545
253	SEG107	–2697.5	1545
254	SEG108	–2762.5	1545
255	SEG109	–2827.5	1545
256	SEG110	–2892.5	1545
257	SEG111	–2957.5	1545
258	SEG112	–3022.5	1545
259	SEG113	–3087.5	1545
260	SEG114	–3152.5	1545
261	SEG115	–3217.5	1545
262	SEG116	–3282.5	1545
263	SEG117	–3347.5	1545
264	SEG118	–3412.5	1545
265	SEG119	–3477.5	1545
266	SEG120	–3542.5	1545
267	SEG121	–3607.5	1545
268	SEG122	–3672.5	1545
269	SEG123	–3737.5	1545
270	SEG124	–3802.5	1545
271	SEG125	–3867.5	1545
272	SEG126	–3932.5	1545
273	SEG127	–3997.5	1545
274	SEG128	–4062.5	1545
275	SEG129	–4127.5	1545
276	SEG130	–4192.5	1545
277	SEG131	–4257.5	1545
278	DUMMY	–4322.5	1545
279	DUMMY	–4387.5	1545
280	DUMMY	–4452.5	1545

Pad No.	Pad Name	X (μm)	Y (μm)
281	DUMMY	–4517.5	1545
282	DUMMY	–4582.5	1545
283	DUMMY	–4647.5	1545
284	DUMMY	–4712.5	1545
285	DUMMY	–4777.5	1545
286	DUMMY	–4842.5	1545
287	DUMMY	–4907.5	1545
288	DUMMY	–4972.5	1545
289	DUMMY	–5037.5	1545
290	DUMMY	–5102.5	1545
291	DUMMY	–5167.5	1545
292	DUMMY	–5340	1366.8
293	DUMMY	–5340	1301.8
294	DUMMY	–5340	1236.8
295	COM24	–5340	1171.8
296	COM25	–5340	1106.8
297	COM26	–5340	1041.8
298	COM27	–5340	976.8
299	COM28	–5340	911.8
300	COM29	–5340	846.8
301	COM30	–5340	781.8
302	COM31	–5340	716.8
303	COM32	–5340	651.8
304	COM33	–5340	586.8
305	COM34	–5340	521.8
306	COM35	–5340	456.8
307	COM36	–5340	391.8

Pad No.	Pad Name	X (μm)	Y (μm)
308	COM37	–5340	326.8
309	COM38	–5340	261.8
310	COM39	–5340	196.8
311	COM40	–5340	131.8
312	COM41	–5340	66.8
313	COM42	–5340	1.8
314	COM43	–5340	–63.2
315	COM44	–5340	–128.2
316	COM45	–5340	–193.2
317	COM46	–5340	–258.2
318	COM47	–5340	–323.2
319	COMS0	–5340	–388.2
320	DUMMY	–5340	–453.2
321	DUMMY	–5340	–518.2
322	DUMMY	–5340	–583.2
323	DUMMY	–5340	–648.2
324	DUMMY	–5340	–713.2
325	DUMMY	–5340	–778.2
326	DUMMY	–5340	–843.2
327	DUMMY	–5340	–908.2
328	DUMMY	–5340	–973.2
329	DUMMY	–5340	–1038.2
330	DUMMY	–5340	–1103.2
331	DUMMY	–5340	–1168.2
332	DUMMY	–5340	–1233.2
333	DUMMY	–5340	–1298.2
334	DUMMY	–5340	–1363.2

NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

4. Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.

5. Neither indemnity against nor license of a third party's industrial and intellectual property right, etc. is granted by us in connection with the use of the product and/or the information and drawings contained herein. No responsibility is assumed by us for any infringement of a third party's right which may result from the use thereof.

6. The products listed in this document are intended for use in general electronics equipment for commercial applications (e.g., office automation, communication equipment, measurement equipment, consumer electronics, etc.). These products are not authorized for use in any system or application that requires special or enhanced quality and reliability characteristics nor in any system or application where the failure of such system or application may result in the loss or damage of property, or death or injury to humans. Such applications include, but are not limited to, traffic and automotive equipment, safety devices, aerospace equipment, nuclear power control, medical equipment, and life-support systems.

7. Certain products in this document may need government approval before they can be exported to particular countries. The purchaser assumes the responsibility of determining the legality of export of these products and will take appropriate and necessary steps at their own expense for these.

8. No part of the contents contained herein may be reprinted or reproduced without our prior permission.

9. MS-DOS is a registered trademark of Microsoft Corporation.

Printed in Japan