ML7022 Evaluation Board

Single Rail Dual Channel PCM/Linear CODEC

This board is used to evaluate an ML7022 device (Single rail dual channel PCM /Linear CODEC). The evaluation board is provided with peripherals needed to operate the LSI, having the capability to evaluate its characteristics easily.
For details of specifications and functions of the ML7022, refer to the data sheet.

1. CONFIGURATION OF EVALUATION BOARD

- Evaluation board 1
- Attached power cord 1
- Female connector components for the flat cable ..... 1 set

2. CIRCUIT DIAGRAMS OF EVALUATION BOARD

The circuit diagrams of the evaluation board are attached herewith. Refer to these circuit diagrams when setting jumper wires and connecting the board to an external circuit.

3. INFORMATION FOR USING EVALUATION BOARD

3.1 Power Supply

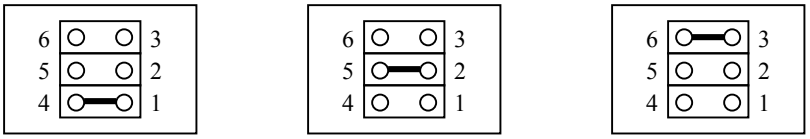
Supply the power to the evaluation board using the attached power cord. The red wire and the brown wire are for +5V, the black wire is to the ground, and the green wire is for –5V.

3.2 Explanation of Jumper Wire

The jumpers marked with JP1 to JP6 on the board are terminals used to connect the ML7022 signal to the flat cable connector, BNC terminals, or FPGA.

- When setting the jumpers as the Figure 1. (a), the ML7022 signal are output at the BNC terminals via the FPGA on the board. In this case, it use PCM CODEC TESTER (ex. MS369B of Anritsu Corporation) to evaluate.
- When setting the jumpers as the Figure 1. (b), the ML7022 signals are directly output at the BNC terminals on the board.
- When setting the jumpers as the Figure 1. (c), the ML7022 signals are connected to the external board with the flat cable connector.

Refer to the Figure 4. (a) the circuit diagrams of the evaluation board for the circuits in each connection setting.



(a) When connecting to the FPGA

(b) When connecting to the BNC terminal

(c) When connecting to the flat cable connector

Figure 1. Jumper setting

3.3 Explanation of Board Switch

Table 1. Explanation of Board Swich

Switch		Function
SW1 ~SW3	BCLK1 ~BCLK3	**Transmit data speed.** This is selected by combination of BCLK3, BCLK2, and BCLK1 (see the following Table 2.). BCLK is available to select 256,512,1024,2048, or 4096KHz.
SW4 ~SW7	C1B~C3B, CPD2	**Channel-2 control bit.** These are used to enter control signal (each channel 4 bits) added to PCM signal (each channel 8 bits). (see the Figure 3.).
SW8 ~SW11	C1A~C3A, CPD1	**Channel-1 control bit.** The same as above.
SW12	CH1/CH2	**Channel-1 / Channel-2 select.** Set the switch to 1 to select Channel 1, and set to 0 to select Channel 2. This selects channel of PCM signal that inputted into CODEC Tester, or channel of PCM signal that inputted into ML7022.
SW13	SHORT	**Long Frame Sync Mode / Short Frame Sync Mode select.** Set to 0 to select Long Frame Sync mode, set to 1 to select Short Frame Sync mode.
SW14	LIN	**PCM Mode / Linear Mode Select.** Set to 0 to select PCM mode, set to 1 to select Linear mode.
SW15 ~SW17	PDN2,PDN1, PDN	**Power Down Control.** Set to 0 to select power-off, set to 1 to select power-on.
SW18	OPT	**Receive Filter Option.** Set to 0 to use ML7022-01.
SW19	ALAW	**PCM interface recommendation rule.** Set to 0 to select μ-law, set to 1 to select A-law.

Table2. Setting of the Transmit Data Speed

BCLK3	BCLK2	BCLK1	BCLK
0	0	0	4096KHz
0	0	1	2048KHz
0	1	0	1024KHz
0	1	1	512KHz
1	0	0	256KHz

3.4 Explanation of FPGA Interface

This evaluation board is used Programmable Logic Device –ALTERA FLEX8000 to generate the signal that control the ML7022. FLEX8000 is a SRAM process, and need an EPROM to store the configuration data.
This FPGA on the board perform a clock generator for the transmission clocks, synchronizing signal and FIFO function.

3.4.1 Pin Descriptions

Table 3. Pin Descriptions

Symbol	Type	Description
PDNO	O	Power Down Control
PDN1O	O	Channel-1 Power Down Control
PDN2O	O	Channel-2 Power Down Control
PDNI	I	Power Down Control
PDN1I	I	Channel-1 Power Down Control
PDN2I	I	Channel-2 Power Down Control
LIN	I	PCM Mode / Linear Mode Select
SHORT	I	Long Frame Sync Mode / Short Frame Sync Mode Select
CH1/2	I	Channel-1 / Channel-2 Select
CPD1	I	Channel-1 Power Down control bit
C3A	I	Channel-1 Control bit
C2A	I	Channel-1 Control bit
C1A	I	Channel-1 Control bit
CPD2	I	Channel-2 Power Down control bit
C3B	I	Channel-2 Control bit
C2B	I	Channel-2 Control bit
C1B	I	Channel-2 Control bit
BCLK3	I	Shift Clock Select bit
BCLK2	I	Shift Clock Select bit
BCLK1	I	Shift Clock Select bit
PCMIN	I	PCM Data Input
PCMOUT	O	PCM Data Output
LMFRM	O	Level Meter Frame
OSCFRM	O	Oscillator Frame
MCKI	I	Master Clock (4.096MHz)
RSYNC	O	Transmit Synchronizing Signal
XSYNC	O	Receive Synchronizing Signal
DOUT	I	Data Input from ML7022
DIN	O	Data Output to ML7022
BCLK	O	Shift Clock for the DIN and DOUT
MCKO	O	Master Clock (4.096MHz)

3.4.2 Timing Diagram

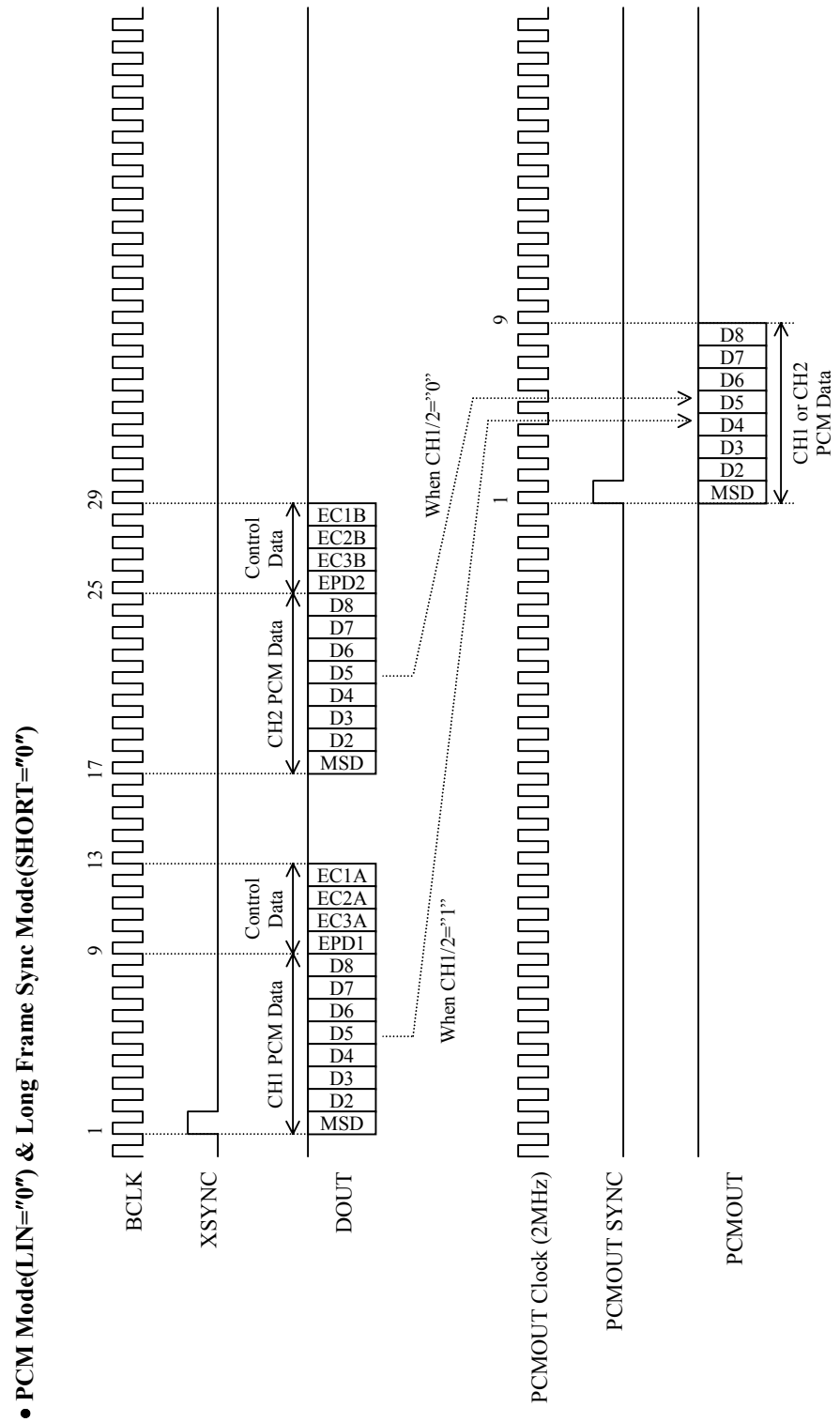


Figure 2. (a) PCMOUT Signal Bit Configuration 1

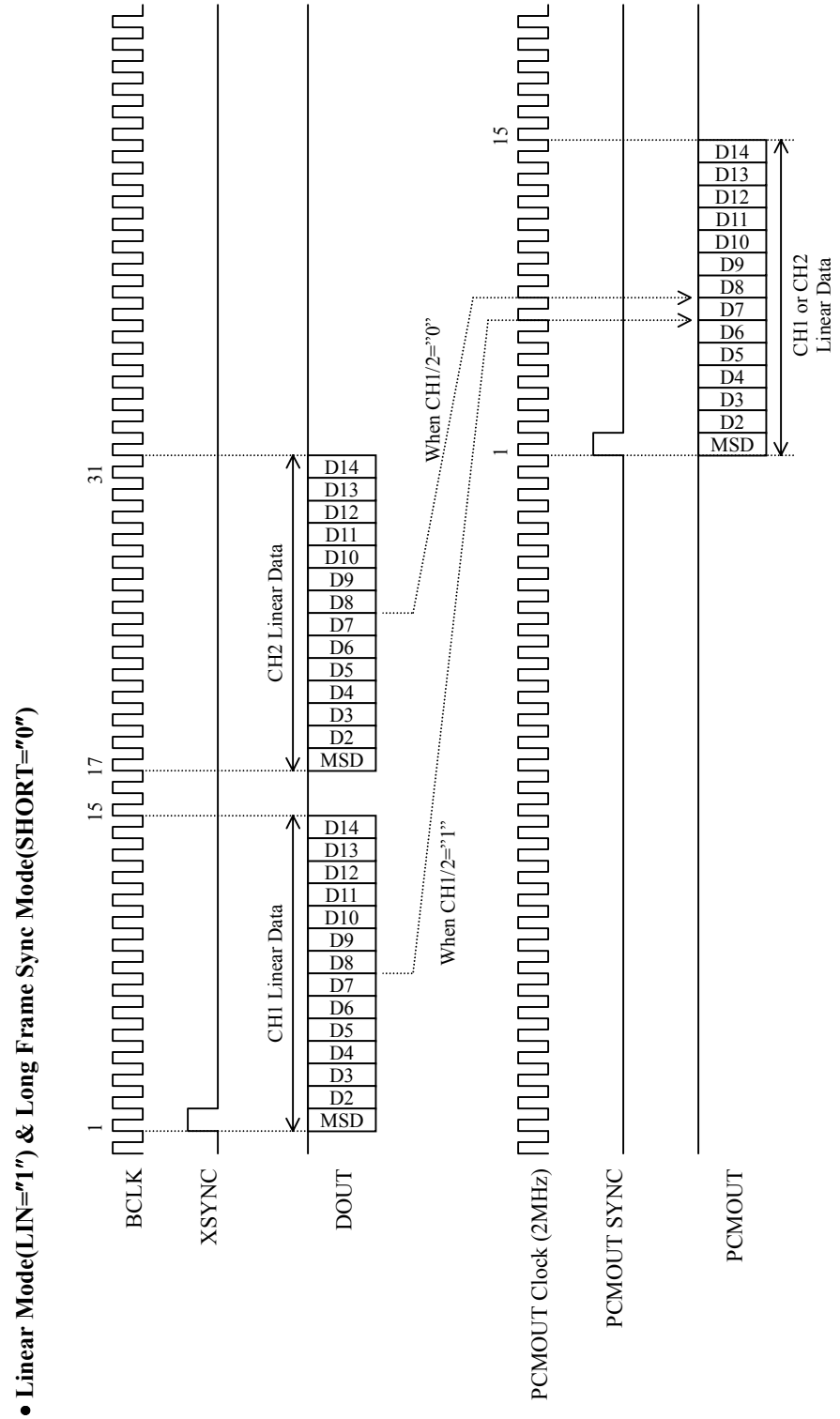


Figure 2. (b) PCMOUT Signal Bit Configuration 2

• **PCM Mode(LIN="0") & Short Frame Sync Mode(SHORT="1")**

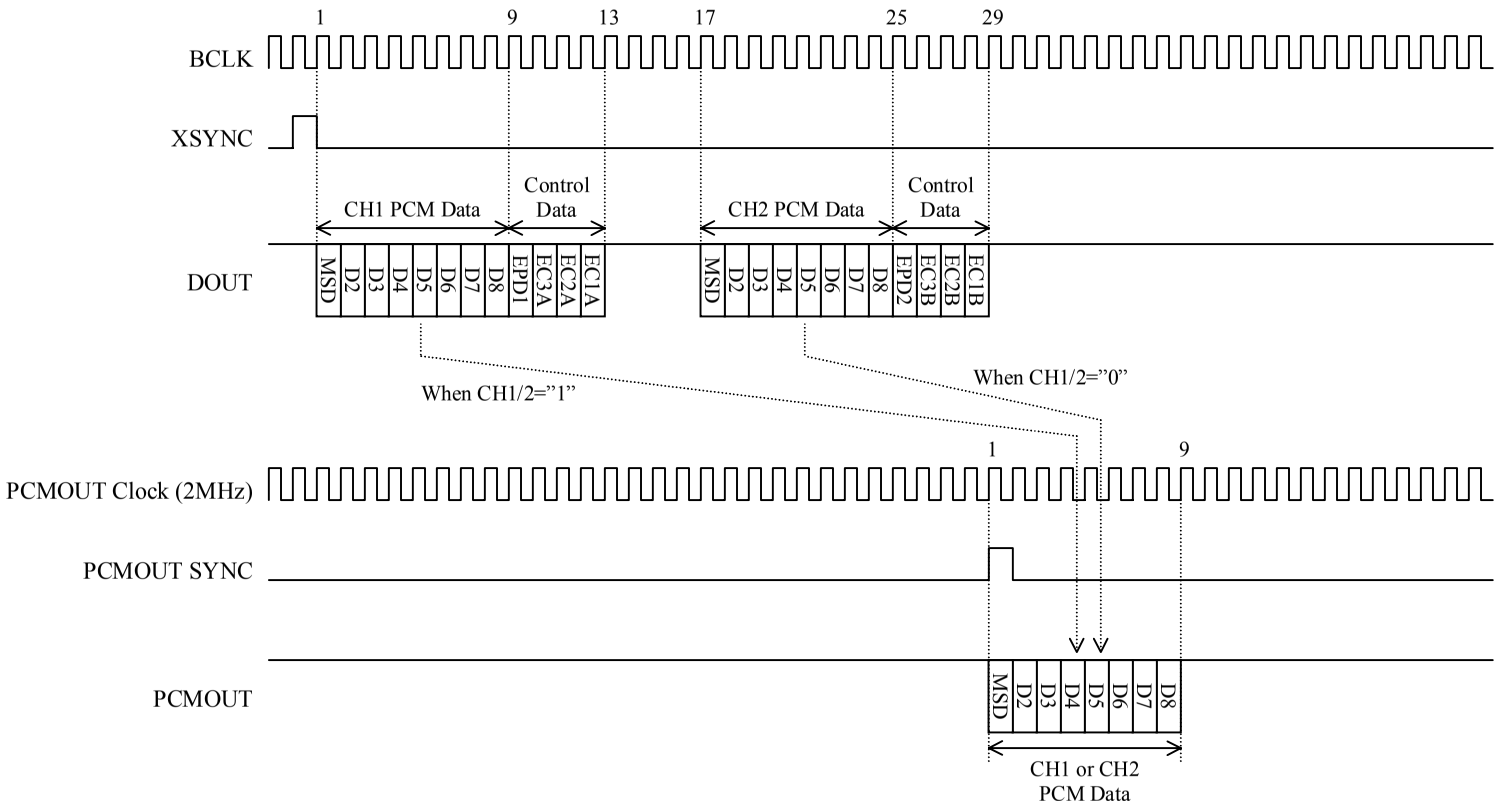


Figure 2. (c) PCMOUT Signal Bit Configuration 3

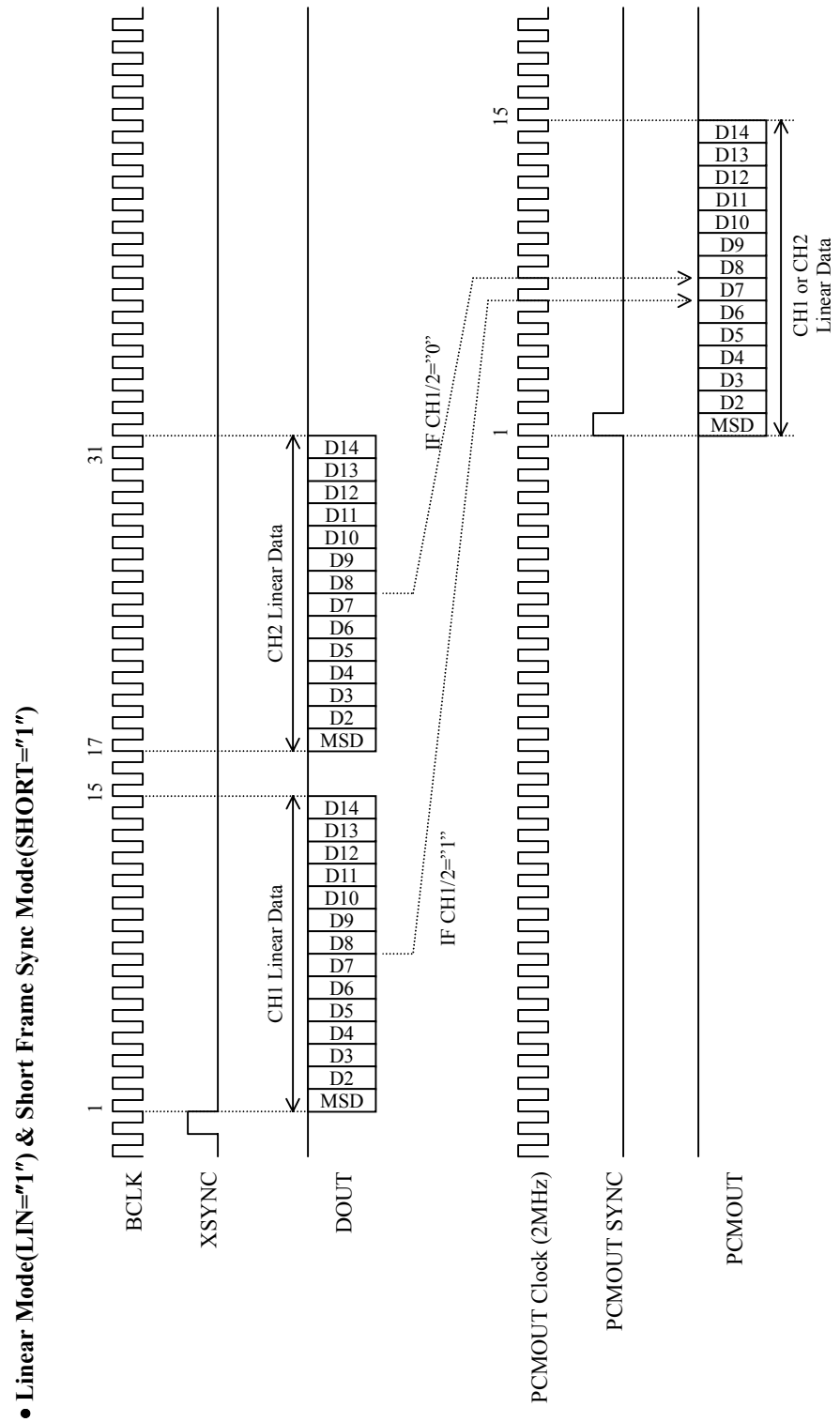


Figure 2. (d) PCMOUT Signal Bit Configuration 4

• **PCM Mode(LIN="0") & Long Frame Sync Mode(SHORT="0")**

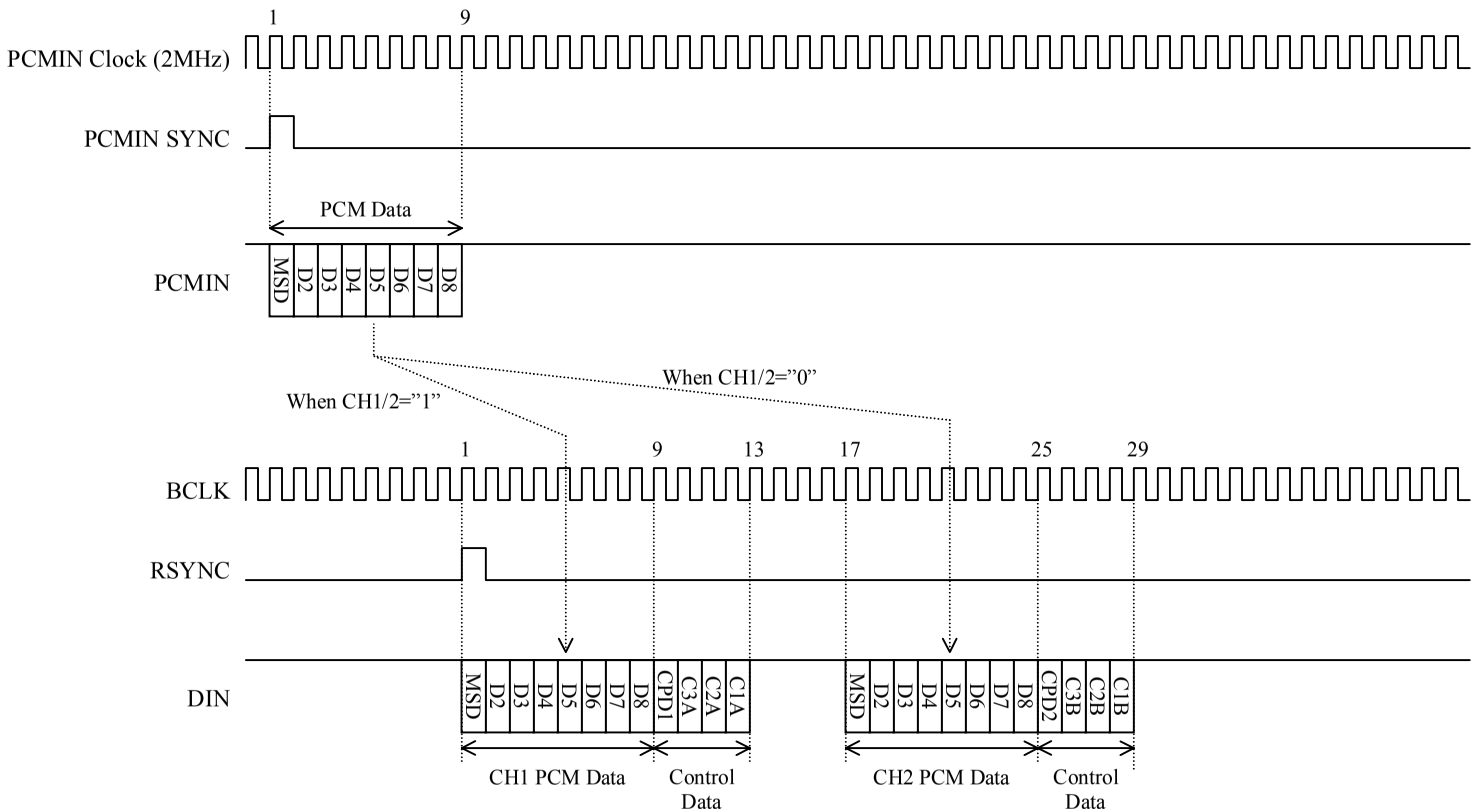


Figure 3. (a) PCMIN Signal Bit Configuration 1

• **PCM Mode(LIN="0") & Short Frame Sync Mode(SHORT="1")**

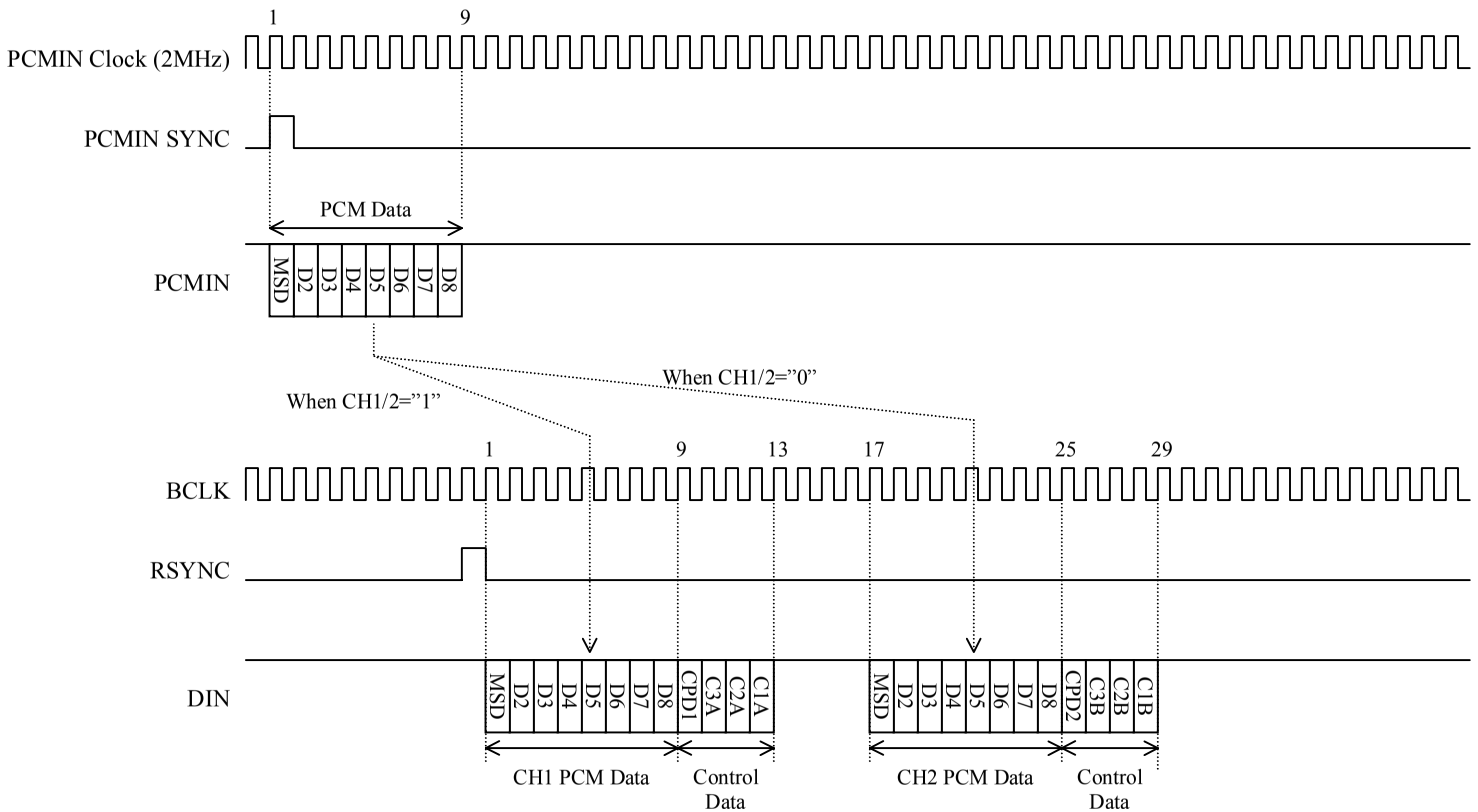


Figure 3. (b) PCMIN Signal Bit Configuration 2

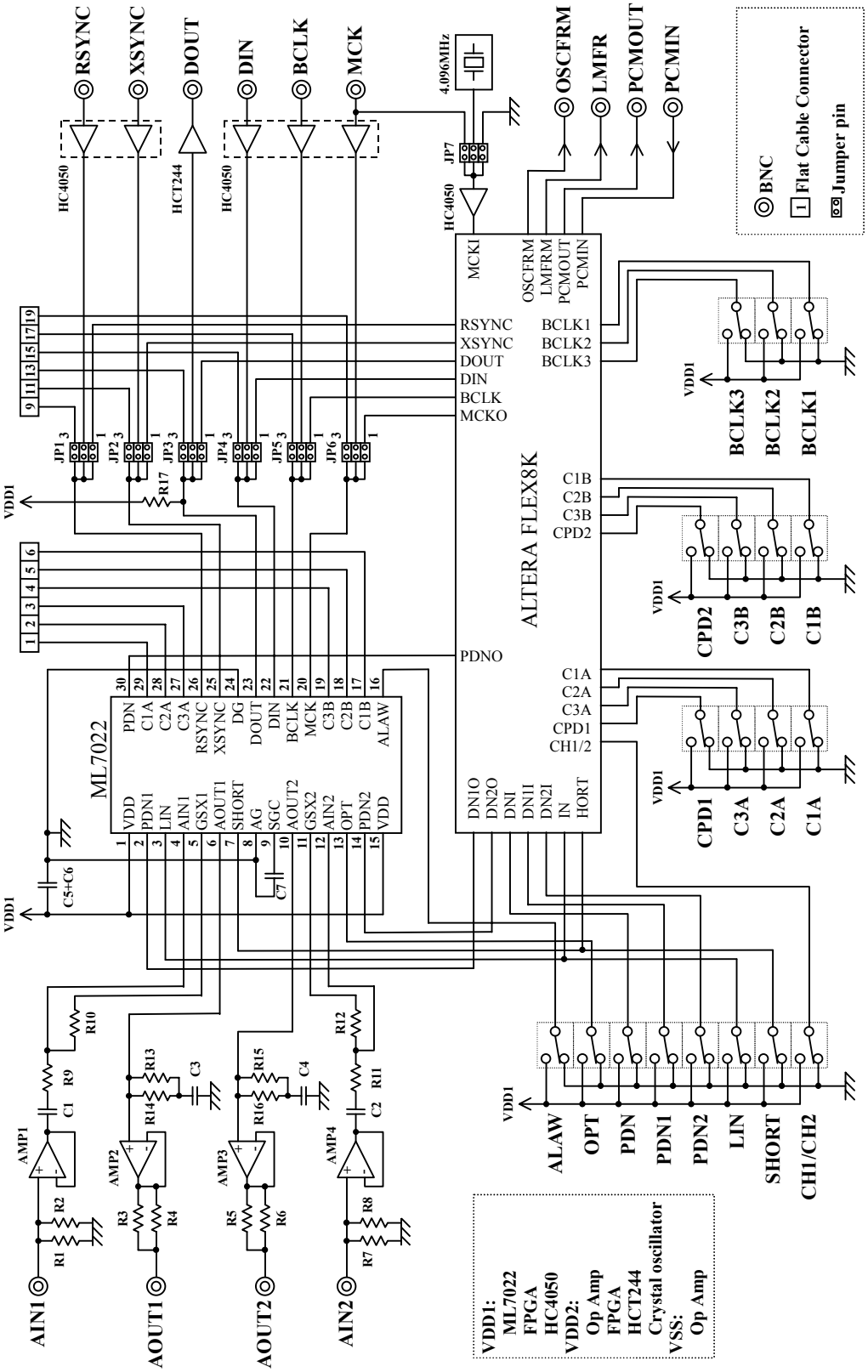


Figure 4. (a) ML7022 Evaluation Board Circuit Diagram

Register		Capacitor	
Number	Value (Ω)	Number	Value (F)
R1	1.2k	C1	1µ
R2	1.2k	C2	1µ
R3	1.2k	C3	1µ
R4	1.2k	C4	1µ
R5	1.2k	C5	0.1µ
R6	1.2k	C6	10µ
R7	1.2k	C7	0.1µ
R8	1.2k		
R9	10k		
R10	10k	Op Amp	
R11	10k	Number	Product
R12	10k	AMP1,2	HA17458
R13	1.2k	AMP3,4	HA17458
R14	1.2k		
R15	1.2k		
R16	1.2k		
R17	510		

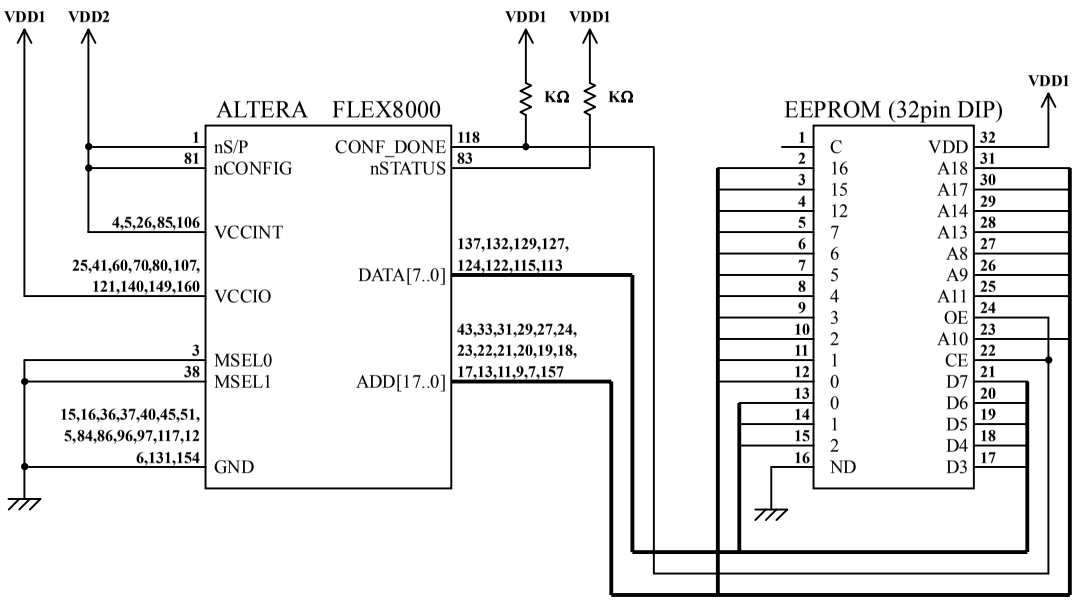


Figure 4. (b) ML7022 Evaluation Board Circuit Diagram

NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.
2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit and assembly designs.
3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.
4. OKI assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum rating or operation outside the specified operating range.
5. Neither indemnity against nor license of a third party's industrial and intellectual property right, etc. is granted by us in connection with the use of the product and/or information and drawings contained herein. No responsibility is assumed by us for any infringement of a third party's right which may result from the use thereof.
6. The products listed in this document are intended for use in general electronics equipment for commercial applications (e.g., office automation, communication equipment, measurement equipment, consumer electronics, etc.). These products are not authorized for use in any system or application that requires special or enhanced quality and reliability characteristics nor in any system or application where the failure of such system or application may result in the loss or damage of property, or death or injury to humans. Such applications include, but are not limited to : traffic control, automotive, safety, aerospace, nuclear power control, and medical, including lift support and maintenance.
7. Certain products in this document may need government approval before they can be exported to particular countries. The purchaser assumes the responsibility of determining the legality of export of these products and will take appropriate and necessary steps at their own expense for these.
8. No part of the contents contained herein may be reprinted or reproduced without our prior permission.