OKI Semiconductor

MK31VT464-10YE

4,194,304 Word x 64 Bit SYNCHRONOUS DYNAMIC RAM MODULE (1BANK):

DESCRIPTION

The Oki MK31VT464-10YE is a fully decoded, 4,194,304 x 64bit synchronous dynamic random access memory composed of four 64Mb DRAMs (4Mx16) in TSOP packages mounted with decoupling capacitors on a 144-pin glass epoxy Small-outline Dual-in-Line Package supports any application where high density and large capacity of storage memory are required, like for example Mobile PC or PDAs.

FEATURES

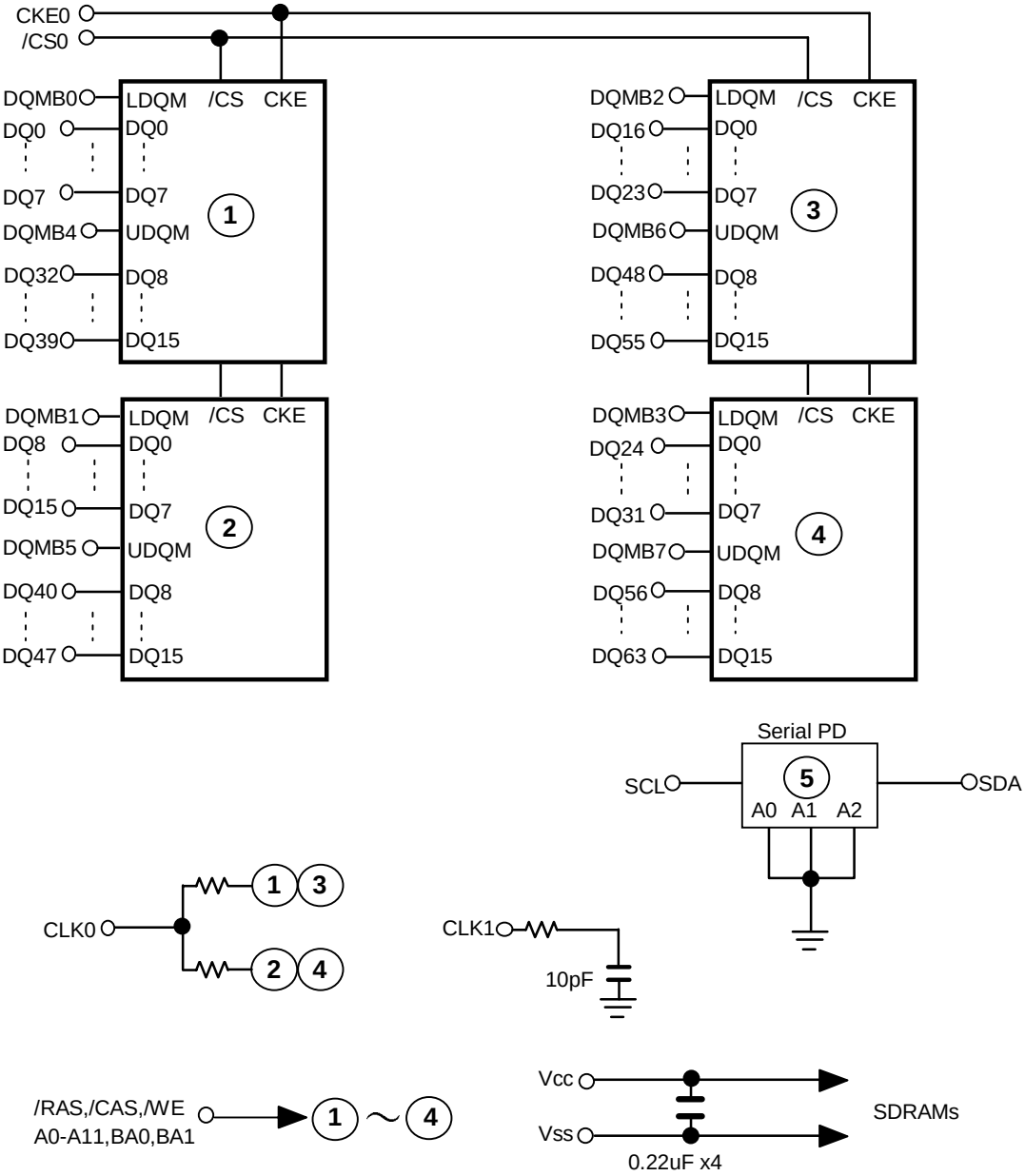
- 4-Meg Word x 64-bit (1Bank 8Byte) organization
- 144-pin Small-Outline Dual Inline Memory Module
- Single 3.3V power supply, ±0.3V tolerance
- Input :LVTTL compatible
- Output :LVTTL compatible
- Refresh : 4,096 cycles / 64 ms
- Programmable data transfer mode
  - /CAS latency (2, 3)
  - Burst length (2, 4, 8)
  - Data scramble (sequential, interleave)
- /CAS before /RAS auto-refresh, Self-refresh capability
- Serial Presence Detect (SPD) With EEPROM

PRODUCT ORGANIZATION

Product Name	Operation Frequency (Max.)	Access Time (Max.)	
		t_{AC2}	t_{AC3}
MK31VT464-10YE	**100 MHz**	**9.0ns**	**9.0ns**

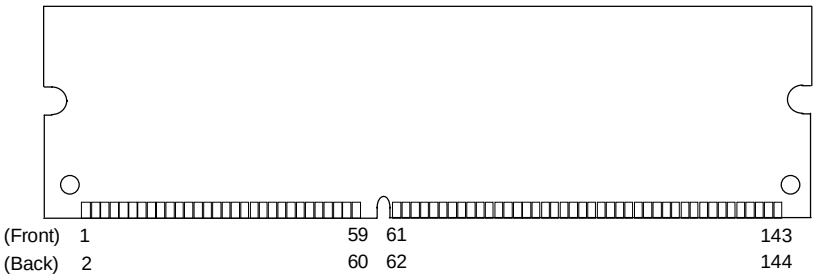
Note. Specification are subject to change without notice.

BLOCK DIAGRAM



Note. The Value of all resistors is 10Ω.

MODULE OUTLINE



PIN CONFIGURATION

Front		Back side	
Pin No.	Pin name	Pin No.	Pin name
1	Vss	2	Vss
3	DQ0	4	DQ32
5	DQ1	6	DQ33
7	DQ2	8	DQ34
9	DQ3	10	DQ35
11	Vcc	12	Vcc
13	DQ4	14	DQ36
15	DQ5	16	DQ37
17	DQ6	18	DQ38
19	DQ7	20	DQ39
21	Vss	22	Vss
23	DQMB0	24	DQMB4
25	DQMB1	26	DQMB5
27	Vcc	28	Vcc
29	A0	30	A3
31	A1	32	A4
33	A2	34	A5
35	Vss	36	Vss
37	DQ8	38	DQ40
39	DQ9	40	DQ41
41	DQ10	42	DQ42
43	DQ11	44	DQ43
45	Vcc	46	Vcc
47	DQ12	48	DQ44
49	DQ13	50	DQ45
51	DQ14	52	DQ46
53	DQ15	54	DQ47
55	Vss	56	Vss
57	N.C	58	N.C
59	N.C	60	N.C
61	CLK0	62	CKE0
63	Vcc	64	Vcc
65	/RAS	66	/CAS
67	/WE	68	N.C
69	/CS0	70	N.C
71	N.C	72	N.C

Front side		Back side	
Pin No.	Pin name	Pin No.	Pin name
73	N.C	74	CLK1
75	Vss	76	Vss
77	N.C	78	N.C
79	N.C	80	N.C
81	Vcc	82	Vcc
83	DQ16	84	DQ48
85	DQ17	86	DQ49
87	DQ18	88	DQ50
89	DQ19	90	DQ51
91	Vss	92	Vss
93	DQ20	94	DQ52
95	DQ21	96	DQ53
97	DQ22	98	DQ54
99	DQ23	100	DQ55
101	Vcc	102	Vcc
103	A6	104	A7
105	A8	106	BA0
107	Vss	108	Vss
109	A9	110	BA1
111	A10	112	A11
113	Vcc	114	Vcc
115	DQMB2	116	DQMB6
117	DQMB3	118	DQMB7
119	Vss	120	Vss
121	DQ24	122	DQ56
123	DQ25	124	DQ57
125	DQ26	126	DQ58
127	DQ27	128	DQ59
129	Vcc	130	Vcc
131	DQ28	132	DQ60
133	DQ29	134	DQ61
135	DQ30	136	DQ62
137	DQ31	138	DQ63
139	Vss	140	Vss
141	SDA	142	SCL
143	Vcc	144	Vcc

Pin Name	Function	Pin Name	Function
Vcc	Power Supply (3.3V)	/RAS	Row Address Strobe
Vss	Ground (0V)	/CAS	Column Address Strobe
CLK#	System Clock	/WE	Write Enable
/CS#	Chip Select	DQMB#	Data Input / Output Mask
CKE#	Clock Enable	DQ#	Data Input / Output
A0-A11	Address	SDA	Data I/O for SPD
BA0,BA1	Bank Select Address	SCL	CLK input for SPD
		N.C	No Connection

SERIAL PRESENCE DETECT

Byte No.	SPD Hex Value	Remark	Notes
0	80	Defines the number of bytes written into SPD memory	128 byte
1	08	Total number of bytes of SPD memory	256 byte
2	04	Fundamental memory type	SDRAM
3	0C	Number of rows	12 rows
4	08	Number of columns	8 columns
5	01	Number of module banks	2 bank
6	40	Data width of this assembly	64 bits
7	00	... Data width continuation	0 bits
8	01	Voltage interface level	LVTTL
9	A0	Cycle time (CL=3)	CL=3 t_{CC}=10ns
10	90	Access time from CLK (CL=3)	CL=3 t_{AC3}=9ns
11	00	DIMM configuration type	Non Parity
12	80	Refresh rate / type	Normal / Self
13	10	Primary SDRAM width	x16
14	00	Error checking SDRAM width	
15	01	Minimum CLK delay	t_{CCD}: 1 CLK
16	0E	Burst lengths supported	2,4,8
17	04	Number of banks on each SDRAM	4 banks
18	06	/CAS latency	2,3
19	01	/CS latency	0
20	01	/WE latency	0
21	00	SDRAM module attributes	
22	06	SDRAM device attributes : General	
23	F0	Cycle time (CL=2)	CL=2 t_{CC2}=15ns
24	90	Access time from CLK (CL=2)	CL=2 t_{AC2}=9ns
25	00	Cycle time (CL=1)	Not support
26	00	Access time from CLK (CL=1)	Not support
27	1E	Minimum ROW pulse width	t_{RP}=30ns
28	14	/RAS to /RAS bank delay	t_{RRD}=20ns
29	1E	/RAS to /CAS delay	t_{RCD}=30ns
30	3C	Minimum /RAS precharge time	t_{RAS}=60ns
31	08	Density of each bank on module	32MB
32	30	Command and Address Signal Input Setup Time	3ns
33	10	Command and Address Signal Input Hold Time	1ns
34	30	Data Signal Input Setup Time	3ns
35	10	Data Signal Input Hold Time	1ns
36-61	00-00		R.F.U
62	02	SPD data revision code	0.2
63	59	Checksum for byte 0-62	
64-71	41,45,20,20,20,20,20,20	Manufacturer's JEDEC ID code	
72	01 / 06	Manufacturing location	
73-90	4D,4B,33,31,56,54,34,36,34, 2D,31,30,59,45,20,20,20,20	Manufacturer's part number	MK31VT464-10YE
91,92	20,20	Revision code	
93-125	00-00	R.F.U	
126	66	Intel specification frequency	66MHz
127	06	Intel specification /CAS latency	CL=2, 3
128-255	FF-FF	Unused storage locations	

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.5 to Vcc + 0.5	V
Vcc supply voltage	Vcc, VccQ	-0.5 to 4.6	V
Storage temperature	T_{stg}	- 55 to 125	°C
Power dissipation	P_{D*}	4	W
Short circuit current	I_{OS}	50	mA
Operating temperature	T_{opr}	0 to 70	°C

*: Ta=25°C

Recommended Operating Conditions

(Voltages referenced to Vss = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	Vcc, VccQ	3.0	3.3	3.6	V
Input high voltage	V_{IH}	2.0	-	Vcc + 0.3	V
Input low voltage	V_{IL}	-0.3	-	0.8	V

Capacitance

(Vcc = 3.3V ± 0.3 V , Ta = 25°C f = 1MHz)

Parameter	Symbol	Max.	Unit
Input capacitance(A0-A11, BA0, BA1)	C_{IN1}	20	pF
Input capacitance(/CS0, /RAS, /CAS, /WE, CKE0, UDQM, LDQM)	C_{IN2}	20	pF
I/O capacitance(DQ0 - DQ63)	$C_{I/O}$	28	pF

DC CHARACTERISTICS

(Vcc = 3.3V ± 0.3V, Ta = 0 to 70°C)

Parameter	Symbol	Condition		Module Spec.		Unit	Note
		CKE	Others	Min.	Max.		
Output High Voltage	V_{OH}	-	I_{OH} = -2.0mA	2.4	-	V	
Output Low Voltage	V_{OL}	-	I_{OL} = 2.0mA	-	0.4	V	
Input Leakage Current	I_{LI}	-	-	-40	40	µA	
Output Leakage Current	I_{LO}	-	-	-20	20	µA	
Average Power Supply Current (Operating)	I_{CC1}	CKE ≥ V_{IH}	t_{CC}=min. t_{RC}=min. No Burst	-	580	mA	1, 2
Power Supply Current (Stand by)	I_{CC2}	CKE ≥ V_{IH}	t_{CC}=min.	-	160	mA	3
Average Power Supply Current (Clock Suspension)	I_{CC3S}	CKE ≤ V_{IL}	t_{CC}=min.	-	60	mA	2
Average Power Supply Current (Active Stand by)	I_{CC3}	CKE ≥ V_{IH}, /CS ≥ V_{IH}	t_{CC}=min.	-	380	mA	3
Power Supply Current (Burst)	I_{CC4}	CKE ≥ V_{IH}	t_{CC}=min.	-	840	mA	1, 2
Power Supply Current (Auto-Refresh)	I_{CC5}	CKE ≥ V_{IH}	t_{CC}=min. t_{RC}=min.	-	740	mA	2
Average Power Supply Current (Self-Refresh)	I_{CC6}	CKE ≤ 0.2V	t_{CC}=min.	-	8	mA	
Average Power Supply Current (Power down)	I_{CC7}	CKE ≤ V_{IL}	t_{CC}=min.	-	328	mA	

Notes: 1. Measured with the output open.
2. Address and data can be changed once or not be changed during one cycle.
3. Address and data can be changed once or not be changed during two cycle.

MODE SET ADDRESS KEYS

/CAS Latency				Burst Type		Burst Length				
A6	A5	A4	CL	A3	BT	A2	A1	A0	BT=0	BT=1
0	0	0	Reserved	0	Sequential	0	0	0	Reserved	Reserved
0	0	1	Reserved	1	Interleave	0	0	1	2	2
0	1	0	2			0	1	0	4	4
0	1	1	3			0	1	1	8	8
1	0	0	Reserved			1	0	0	Reserved	Reserved
1	0	1	Reserved			1	0	1	Reserved	Reserved
1	1	0	Reserved			1	1	0	Reserved	Reserved
1	1	1	Reserved			1	1	1	Reserved	Reserved

Note: A7, A8, A9, A10, A11, BA0, BA1 and All should stay "L" during mode set cycle.

POWER ON SEQUENCE

1. With inputs in NOP state, turn on the power supply and enter the system clock.
2. After the Vcc voltage has reached the specified level, take a pause of 200μs or more with the input being NOP.
3. Enter the precharge all bank command.
4. Apply CBR auto-refresh eight or more times.
5. Enter the mode register setting command.

AC CHARACTERISTIC

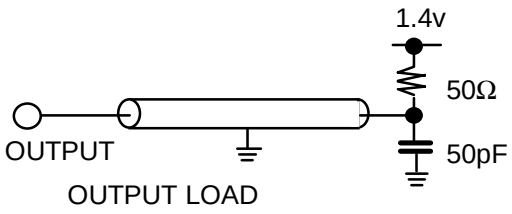
(V_{CC} = 3.3V ± 0.3V, Ta = 0 ~ 70°C)

NOTE 1, 2

Parameter		Symbol	Module Spec.		Unit	Note
			Min.	Max.		
Clock Cycle Time	CL=3	t_{CC}	10	-	ns	
	CL=2		15	-	ns	
Access Time from Clock	CL=3	t_{AC}	-	9	ns	3, 4
	CL=2		-	9	ns	3, 4
Clock "H" Pulse Time		t_{CH}	3	-	ns	
Clock "L" Pulse Time		t_{CL}	3	-	ns	
Input Setup Time		t_{SI}	3	-	ns	
Input Hold Time		t_{HI}	1	-	ns	
Output Low Impedance Time from Clock		t_{OLZ}	3	-	ns	
Output High Impedance Time from Clock		t_{OHZ}	-	8	ns	
Output Hold from Clock		t_{OH}	3	-	ns	3
/RAS Cycle Time		t_{RC}	90	-	ns	
/RAS Precharge Time		t_{RP}	30	-	ns	
/RAS Active Time		t_{RAS}	60	1,000,000	ns	
/RAS to /CAS Delay Time		t_{RCD}	30	-	ns	
Write Recovery Time		t_{WR}	15	-	ns	
/RAS to /RAS Bank Active Delay Time		t_{RRD}	20	-	ns	
Refresh Time		t_{REF}	-	64	ms	
Power-down Exit Set-up Time		t_{PDE}	t_{SI}+1CLK	-	ns	
Input Level Transition Time		t_T	-	3	ns	
/CAS to /CAS Delay Time (Min)		I_{CCD}	1		Cycle	
Clock Disable Time from CKE		I_{CKE}	1		Cycle	
Data Output High Impedance Time from		I_{DOZ}	2		Cycle	
Data Input Mask Time from DQMB		I_{DOD}	0		Cycle	
Data Input Time from Write Command		I_{DWD}	0		Cycle	
Data Output High InpedanceTime from Precharge Command		I_{ROH}	2		Cycle	
Active Command Input Time from MODE		I_{MRD}	3		Cycle	
Write Command Input Time from Output		I_{OWD}	2		Cycle	

NOTES:

1) AC measurements assume t_T=1ns.
2) The reference level for timing of input signals is 1.4V.
3) This parameter is measured with a load circuit equivalent to 1 TTL load and 50pF (R_{Load} is 50ohm).
4) An access time is measured at 1.4V.
5) If t_T is longer than 1ns, the reference level for timing of input signals are V_{IH} and V_{IL}.



OUTPUT LOAD

FUNCTION TRUTH TABLE (Table1) (1/2)

Current State	/CS	/RAS	/CAS	/WE	BA	ADDR	Action
Idle	H	X	X	X	X	X	NOP
	L	H	H	H	X	X	NOP
	L	H	H	L	BA	X	ILLEGAL [2]
	L	H	L	X	BA	CA	ILLEGAL [2]
	L	L	H	H	BA	RA	Row Active
	L	L	H	L	BA	A10	NOP [4]
	L	L	L	H	X	X	Auto-Refresh or Self-Refresh [5]
	L	L	L	L	L	OP Code	Mode Register write
Row Active	H	X	X	X	X	X	NOP
	L	H	H	X	X	X	NOP
	L	H	L	H	BA	CA, A10	Read
	L	H	L	L	BA	CA, A10	Write
	L	L	H	H	BA	RA	ILLEGAL [2]
	L	L	H	L	BA	A10	Precharge
	L	L	L	X	X	X	ILLEGAL
Read	H	X	X	X	X	X	NOP (Continue Row Active after Burst ends)
	L	H	H	H	X	X	NOP (Continue Row Active after Burst ends)
	L	H	H	L	BA	X	Burst Stop
	L	H	L	H	BA	CA, A10	Term Burst, start new Burst Read [3]
	L	H	L	L	BA	CA, A10	Term Burst, start new Burst Write [3]
	L	L	H	H	BA	RA	ILLEGAL [2]
	L	L	H	L	BA	A10	Term Burst, execute Row Precharge
	L	L	L	X	X	X	ILLEGAL
Write	H	X	X	X	X	X	NOP (Continue Row Active after Burst ends)
	L	H	H	H	X	X	NOP (Continue Row Active after Burst ends)
	L	H	H	L	BA	X	Burst Stop
	L	H	L	H	BA	CA, A10	Term Burst, start new Burst Read [3]
	L	H	L	L	BA	CA, A10	Term Burst, start new Burst Write [3]
	L	L	H	H	BA	RA	ILLEGAL [2]
	L	L	H	L	BA	A10	Term Burst, execute Row Precharge [3]
	L	L	L	X	X	X	ILLEGAL
Read with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End and enter Row Precharge)
	L	H	H	H	X	X	NOP (Continue Burst to End and enter Row Precharge)
	L	H	H	L	BA	X	ILLEGAL [2]
	L	H	L	H	BA	CA, A10	ILLEGAL [2]
	L	H	L	L	X	X	ILLEGAL
	L	L	H	X	BA	RA, A10	ILLEGAL [2]
	L	L	L	X	X	X	ILLEGAL
Write with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End and enter Row Precharge)
	L	H	H	H	X	X	NOP (Continue Burst to End and enter Row Precharge)
	L	H	H	L	BA	X	ILLEGAL [2]
	L	H	L	H	BA	CA, A10	ILLEGAL [2]
	L	H	L	L	X	X	ILLEGAL
	L	L	H	X	BA	RA, A10	ILLEGAL [2]
	L	L	L	X	X	X	ILLEGAL

FUNCTION TRUTH TABLE (Table1) (2/2)

Current State	/CS	/RAS	/CAS	/WE	BA	ADDR	Action
Precharge	H	X	X	X	X	X	NOP → Idle after t_{RP}
	L	H	H	H	X	X	NOP → Idle after t_{RP}
	L	H	H	L	BA	X	ILLEGAL [2]
	L	H	L	X	BA	CA	ILLEGAL [2]
	L	L	H	H	BA	RA	ILLEGAL [2]
	L	L	H	L	BA	A10	NOP [4]
	L	L	L	X	X	X	ILLEGAL
Write Recovery	H	X	X	X	X	X	NOP
	L	H	H	H	X	X	NOP
	L	H	H	L	BA	X	ILLEGAL [2]
	L	H	L	X	BA	CA	ILLEGAL [2]
	L	L	H	H	BA	RA	ILLEGAL [2]
	L	L	H	L	BA	A10	ILLEGAL [2]
	L	L	L	X	X	X	ILLEGAL
Row Active	H	X	X	X	X	X	NOP Row Active after t_{RCD}
	L	H	H	H	X	X	NOP Row Active after t_{RCD}
	L	H	H	L	BA	X	ILLEGAL [2]
	L	H	L	X	BA	CA	ILLEGAL [2]
	L	L	H	H	BA	RA	ILLEGAL [2]
	L	L	H	L	BA	A10	ILLEGAL [2]
	L	L	L	X	X	X	ILLEGAL
Refresh	H	X	X	X	X	X	NOP → Idle after t_{RC}
	L	H	H	X	X	X	NOP → Idle after t_{RC}
	L	H	L	X	X	X	ILLEGAL
	L	L	H	X	X	X	ILLEGAL
	L	L	L	X	X	X	ILLEGAL
Auto Resister Access	H	X	X	X	X	X	NOP
	L	H	H	H	X	X	NOP
	L	H	H	L	X	X	ILLEGAL
	L	H	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	ILLEGAL

ABBREVIATIONS

RA = Row Address BA = Bank Address NOP = No Operation command
CA = Column Address AP = Auto Precharge

Notes:

1. All inputs will be enabled when CKE is set high for at least 1 cycle prior to the inputs.
2. Illegal to bank in specified state, but may be legal in some cases depending on the state of bank selection.
3. Satisfy the timing of t_{CCD} and t_{WR} to prevent bus contention.
4. NOP to bank precharging or in idle state. Precharges activated bank by BA or A10.
5. Illegal if any bank is not idle.

FUNCTION TRUTH TABLE (CKE) (Table2)

Current State(n)	CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	ADDR	Action
Self Refresh	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Self Refresh → ABI
	L	H	L	H	H	H	X	Exit Self Refresh → ABI
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Self Refresh)
Power Down	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Power Down → ABI
	L	H	L	H	H	H	X	Exit Power Down → ABI
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	X	X	X	X	ILLEGAL [6]
	L	L	X	X	X	X	X	NOP (Continue power down mode)
All Banks idle [6] (ABI)	H	H	X	X	X	X	X	Refer to Table 1
	H	L	H	X	X	X	X	Enter Power Down
	H	L	L	H	H	H	X	Enter Power Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	H	L	X	ILLEGAL
	H	L	L	L	L	H	X	Enter Self Refresh
	H	L	L	L	L	L	X	ILLEGAL
	L	L	X	X	X	X	X	NOP
Any State Other than Listed Above	H	H	X	X	X	X	X	Refer to Operations in Table 1
	H	L	X	X	X	X	X	Begin Clock Suspend Next Cycle
	L	H	X	X	X	X	X	Enable Clock of Next Cycle
	L	L	X	X	X	X	X	Continue Clock Suspension

Notes:

6. Power-down and self refresh can be entered only when all the banks are in an idle state.