OKI Electronic Components

This version: Dec. 2000

KGL4201/KGL4201C **Preliminary**

10Gb/s/ 12.5Gb/s 8:1 Multiplexer

GENERAL DESCRIPTION

The KGL4201/KGL4201C converts low-speed 8bit parallel data streams into high-speed serial data stream up to 10Gb/s/ 12.5Gb/s. Parallel input data loading is synchronized with the internal 1/8 clock generated from an input clock on chip. Serial output data are synchronized with the input clock. The device is ideal for use in the 10Gb/s/ 12.5Gb/s optical communication systems.

FEATURES

- High speed operation : 10Gb/s for KGL4201
  12.5Gb/s for KGL4201C
- Single power supply voltage : 2 V
- Low power dissipation : 2.4 W
- Rise/Fall time : 30 ps
- Complementary serial data outputs
- Package : 40 pin QFP

ABSOLUTE MAXIMUM RATINGS

No.	Item	Symbol	Min.	Max.	Unit
1	Supply Voltage for Internal Logic	V_{DD}	−0.3	2.3	V
2	Supply Voltage for Output Buffer	V_B	−0.3	2.3	V
3	Clock Input	CK	−0.3	1.5	V
4	Data Inputs	D0 to 7	−0.3	1.5	V
6	Temperature at Package Base under Bias	T_s	−45	100	°C
7	Storage Temperature	T_{st}	−45	125	°C

FUNCTIONAL BLOCK DIAGRAM
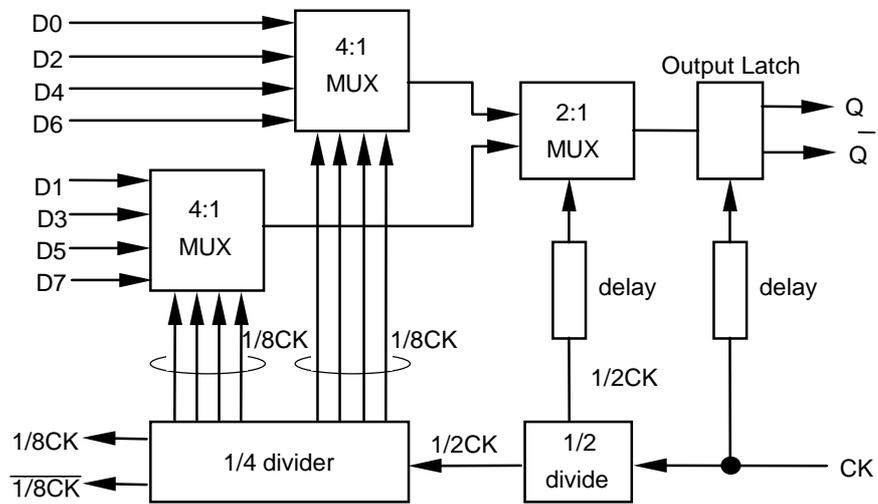
TIME CHART
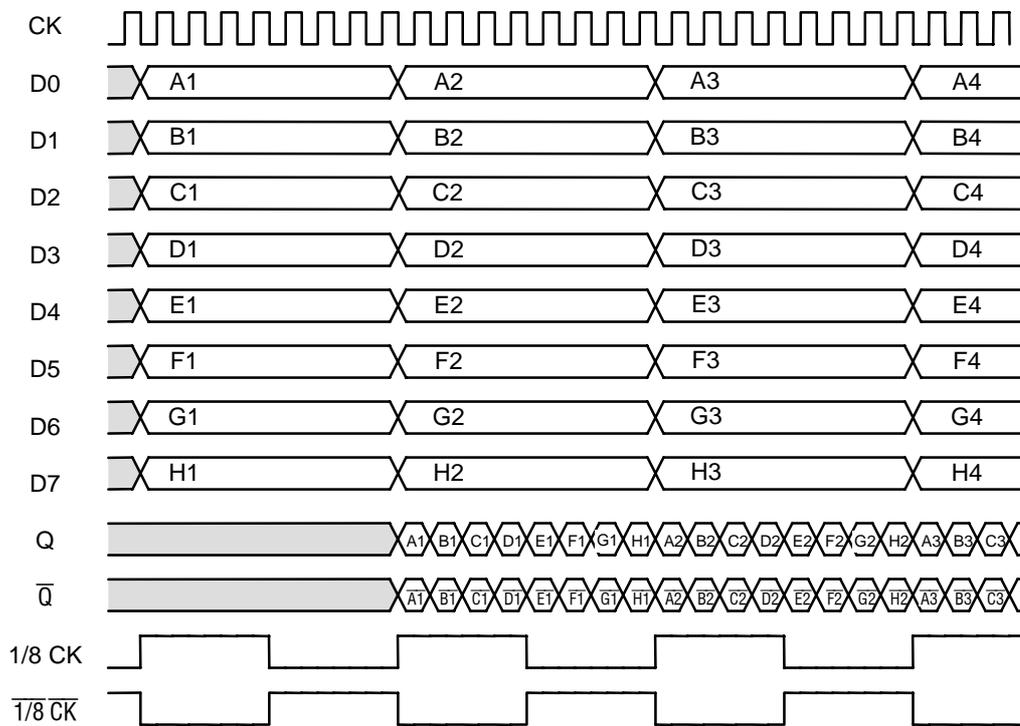
RECOMMENDED OPERATING CONDITIONS

Item	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage for Internal Logic	V_{DD}	1.9	2.0	2.1	V
Power Supply Voltage for Output Buffer	V_B	1.9	2.0	2.1	V
Operating Temperature Range at Package Base	T_s	0		70	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics

$V_{DD} = 2$ V, $V_B = 2$ V , Ts = 25 °C

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power Dissipation	P		—	2.4	3.0	W
High-level 1/8CK Output Voltage	V_{OH}		0.85		1.3	V
Low-level 1/8CK Output Voltage	V_{OL}		0		0.3	V
Data Output Voltage Swing	V_{OD}	50 Ω Load	0.7		1.2	Vp-p
Clock Input Voltage Swing	V_{CK}	Capacitive Coupling	0.5		0.9	Vp-p
High-level Data Input Voltage	V_{IDH}		0.8		1.3	V
Low-level Data Input Voltage	V_{IDL}		0		0.3	V

AC Characteristics

$V_{DD} = 2$ V, $V_B = 2$ V, Ts = 25°C

Item		Symbol	Test Condition	Min.	Typ.	Max.	Unit
Maximum Operating	KGL4201	fo		10	—	—	GHz
Clock Frequency	KGL4201C			12.5	—	—	
Set-up Time (Data to 1/8CK ↓)		t_{DS}		450	500	550	ps
Hold Time (1/8CK ↓ to Data)		t_{DH}		−400	−350	−300	ps
CK-D0 to 7	KGL4201	Δt_M	fo = 10 GHz	550	650		ps
Phase Margin	KGL4201C		fo = 12.5 GHz	400	500		
Rise Time (Q,$\overline{Q}$) (20 to 80%)		tr		20	30	40	ps
Fall Time (Q,$\overline{Q}$) (20 to 80%)		tf		20	30	40	ps

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WAVEFORMS

CK

Δt_C

D0
to D7   Valid Δt_M Valid

t_{DH}

t_{DS}

1/8CK

$\overline{1/8CK}$

$\Delta t_C = 1/fo$

RISE AND FALL TIME

100%
80%

20%
0%

tr   tf

MARKING

INDEX

PRODUCTION NAME

COMPANY LOGO

1   31

KGL4201

OKI

JAPAN

XXX C

21

11

COUNTRY

GRADE   KGL4201   : BLANK
         KGL4201C : C

MONTHLY LOT NUMBER
PRODUCTION MONTH   LOT NUMBER
PRODUCTION YEAR
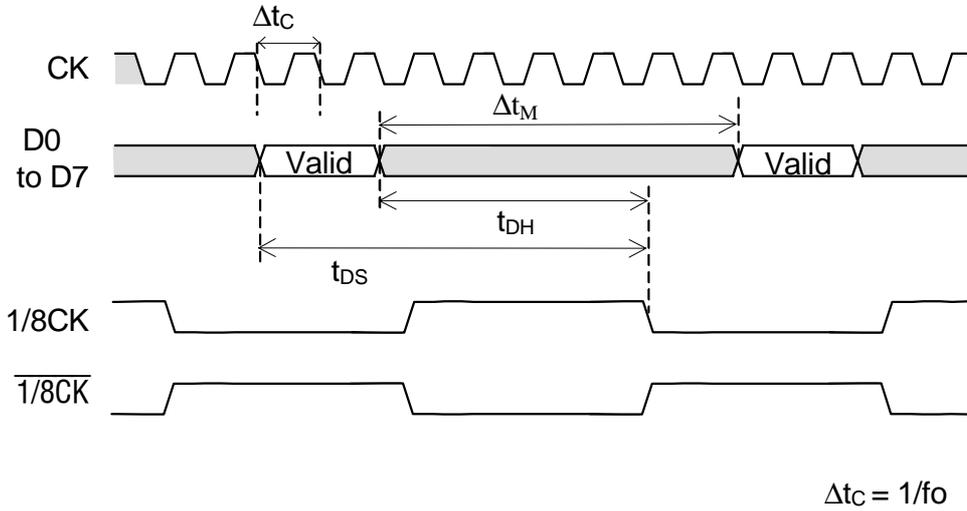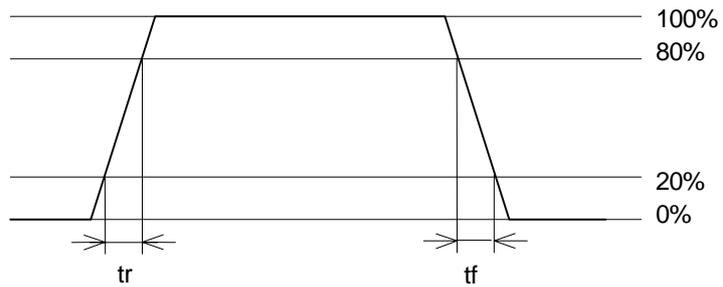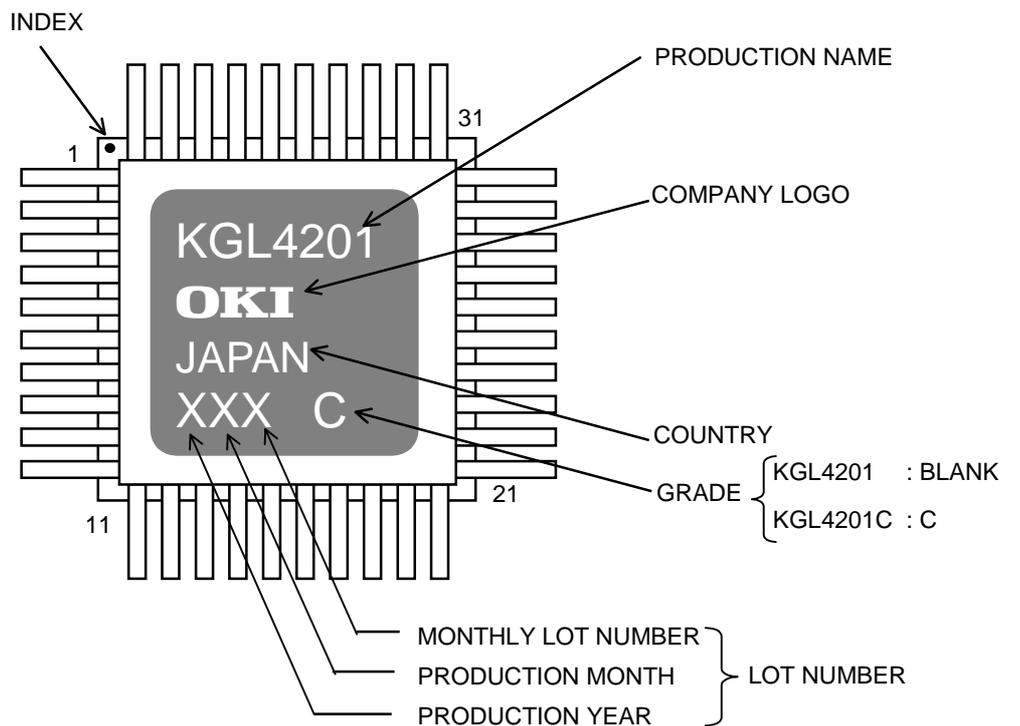
PACKAGE INFORMATION
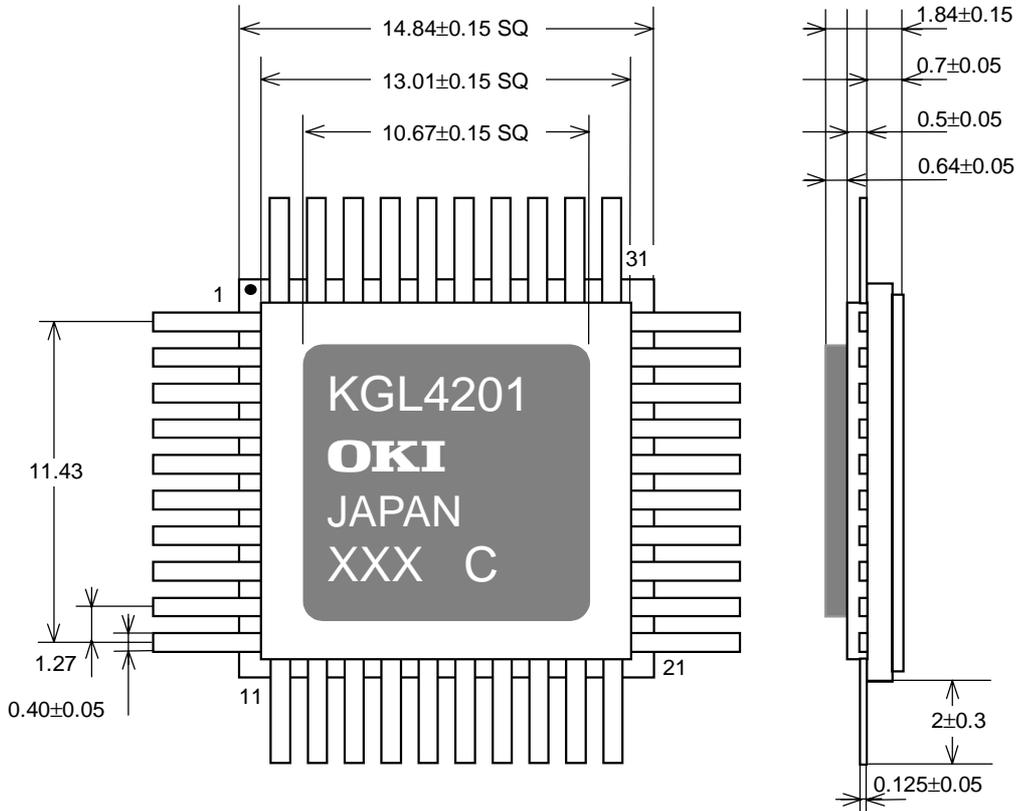
Top View

unit : mm

Pin Assignment

Pin	Symbol	Description	Pin	Symbol	Description
1	G	Ground	21	V_{DD}	Power Supply (Logic)
2	Q	Data Output(Pos.)	22	G	Ground
3	G	Ground	23	G	Ground
4	$\overline{Q}$	Data Output(Neg.)	24	CK	Clock Input
5	G	Ground	25	G	Ground
6	G	Ground	26	G	Ground
7	1/8CK	1/8 Clock Output	27	RCK	Clock Reference Bias
8	G	Ground	28	G	Ground
9	$\overline{1/8CK}$	$\overline{1/8\ Clock}$ Output	29	G	Ground
10	V_B	Power Supply (Buffer)	30	G	Ground
11	G	Ground	31	G	Ground
12	V_{DD}	Power Supply (Logic)	32	V_{DD}	Power Supply (Logic)
13	D0	Data Input 0	33	D7	Data Input 7
14	G	Ground	34	G	Ground
15	D2	Data Input 2	35	D5	Data Input 5
16	D4	Data Input 4	36	D3	Data Input 3
17	G	Ground	37	G	Ground
18	D6	Data Input 6	38	D1	Data Input 1
19	G	Ground	39	V_B	Power Supply (Buffer)
20	G	Ground	40	V_{DD}	Power Supply (Logic)

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TYPICAL INTERFACE CONFIGURATION

VIDH = 0.8 V, VIDL = 0.2 V

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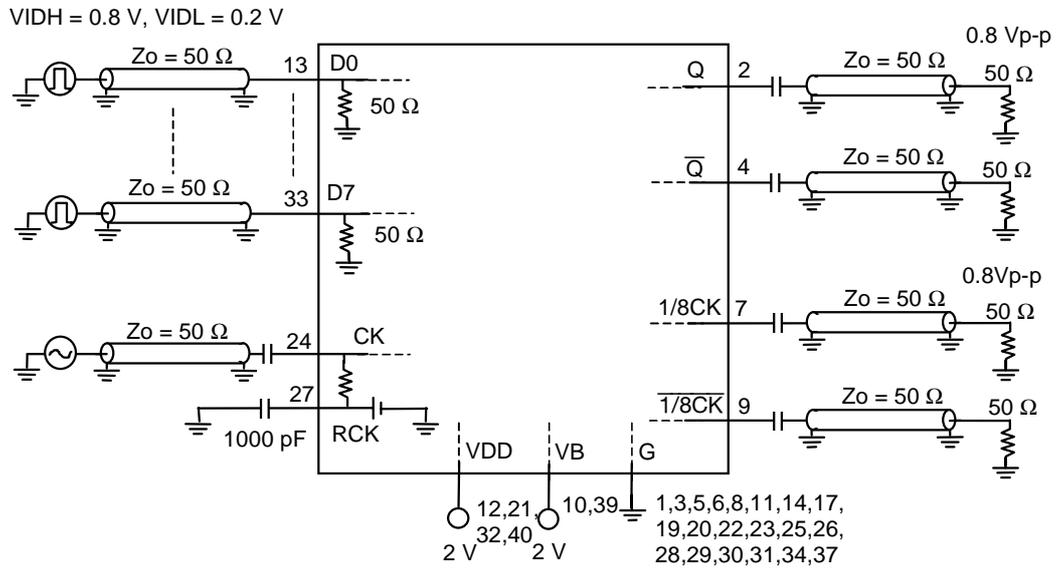
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