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VERSA MIX: MIXED-SIGNAL, FULLY INTEGRATED MICROCONTROLLER WITH DSP

Datasheet Rev 0.5

Preliminary

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Overview

The VERSA MIX is a fully integrated mixed-signal microcontroller that provides a "one-chip solution" for a broad range of signal conditioning, data acquisition, processing, and control applications. The VERSA MIX is based on a powerful single-cycle, RISC-based, 8051 microprocessor and an enhanced MAC unit that can be used to perform complex mathematical operations.

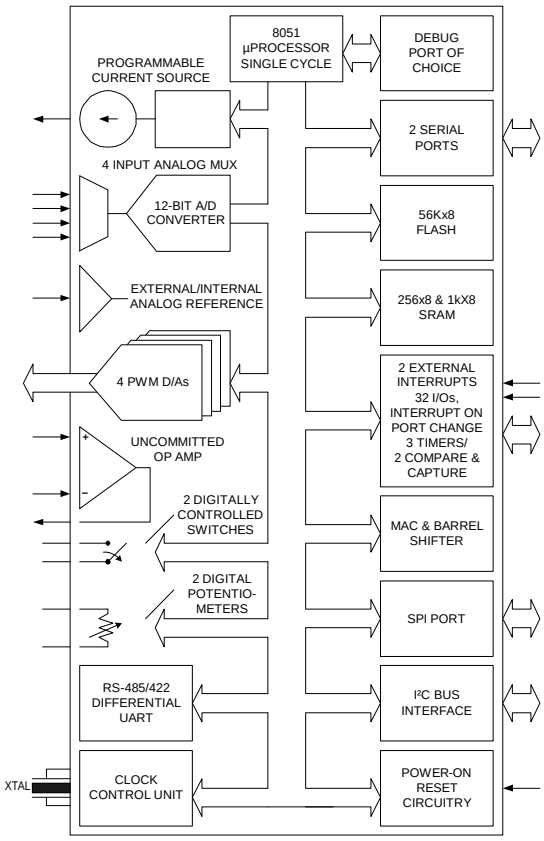
On-chip analog peripherals such as a 4-channel A/D converter, 4 PWM based D/A converters, a voltage reference, a programmable current source, an uncommitted operational amplifier, software programmable digital potentiometers and programmable switches make the VERSA MIX ideal for analog data acquisition.

The inclusion of a full set of digital interfaces such as an enhanced fully configurable SPI, an I^2C interface, UARTs and a differential RS-485/RS-422 interface allow a total system integration solution on one chip.

Applications

- Automotive Applications
- Medical Devices
- Industrial Controls/ Measurement Systems
- Consumer Products
- Instrumentation
- Battery Powered Systems
- Intelligent Sensors (IEEE 1451.2 Compatible)

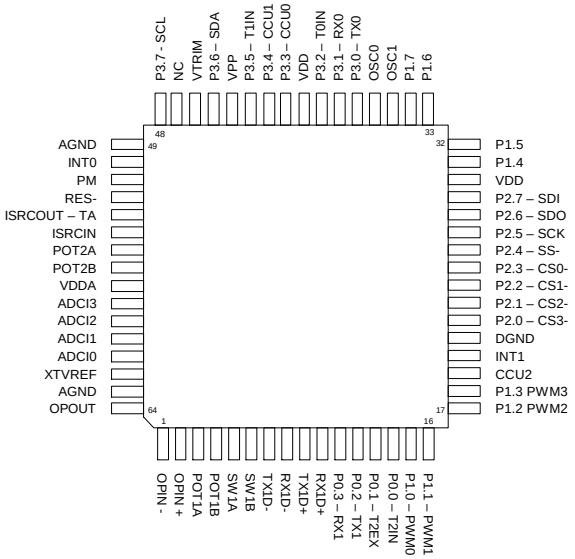
FIGURE 1: VERSA MIX BLOCK DIAGRAM



Feature Set

- 8051 Compatible RISC performances µProcessor
  - Single Cycle Instructions
  - Dual Data Pointers
- MAC including Barrel Shifter
  - Provides DSP Capability
- 56KB Flash Program/Storage Memory
- 1280 Bytes of SRAM
- 2 Serial Interface UARTs
- RS-485/RS-422 Transceiver interfaced to UART1
- Enhanced SPI interface (Master/Slave)
  - Fully configurable
  - Controls up to 4 slave devices
- Up to 32 General Purpose I/Os
- 1 / 2 General Purpose Interrupt Inputs
- Interrupt on port change
- 3 Timers / Counters
- Up to 3 Capture and Compare Inputs
- 4-Channel 12-bit A/D Converter
  - 0-2.7 Volt Input Range
  - Continuous/One-Shot operation
  - Single or 4-channel conversions
  - Programmable Interrupt to Processor
- On-Chip Voltage Reference
- 4 Pulse Width Modulated D/A Converters
- Programmable Current Source
- Uncommitted Operational Amplifier
- Up to 2 Digital Potentiometers
- Up to 2 Digitally Controlled Switches
- Power Saving Features
- Power-on Reset with Brown-Out Detect

FIGURE 2: QFP-64 PACKAGE #1 PINOUT



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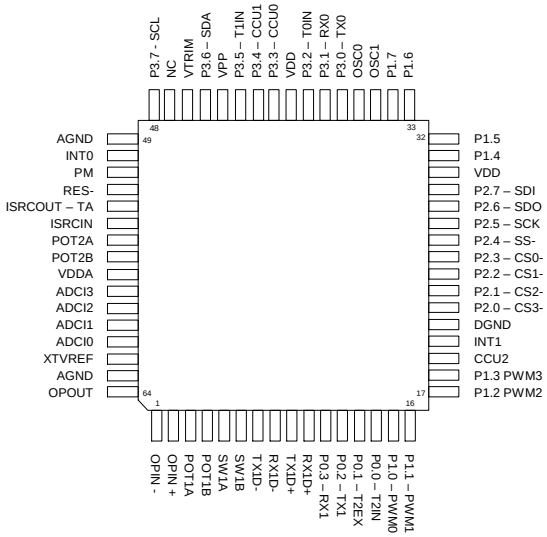
Pins Description for QFP-64-1

TABLE 1: PIN OUT DESCRIPTION

PIN	NAME	FUNCTION
1	OPIN-	Inverting Input of the Operational Amplifier
2	OPIN+	Non-inverting Input of the Operational Amplifier
3	POT1A	Digitally Controlled Potentiometer 1A
4	POT1B	Digitally Controlled Potentiometer 1B
5	SW1A	Digitally Controlled Switch 1A
6	SW1B	Digitally Controlled Switch 1B
7	TX1D-	RS-485 Differential Transmitter 1 or RS-422 Transceiver 1
8	RX1D-	RS-485 Differential Receiver 1 or RS-422 Transceiver 1
9	TX1D+	RS-485 Differential Transmitter 2 or RS-422 Transceiver 1
10	RX1D+	RS-485 Differential Receiver 1 or RS-422 Transceiver 1
11	P0.3-RX1	I/0 - Asynchronous UART1 Receiver Input
12	P0.2-TX1	I/0 - Asynchronous UART1 Transmitter Output
13	P0.1-T2EX	I/0 -Timer/Counter 2 Input
14	P0.0-T2IN	I/0 -Timer/Counter 2 Input
15	P1.0-PWM0	I/0 - Pulse Width Modulated Digital to Analog Converter 0
16	P1.1-PWM1	Pulse Width Modulated Digital to Analog Converter 1
17	P1.2-PWM2	Pulse Width Modulated Digital to Analog Converter 2
18	P1.3-PWM3	Pulse Width Modulated Digital to Analog Converter 3
19	CCU2	Capture and Compare Unit 2 Input
20	INT1	Interrupt Input 1
21	DGND	Digital Ground
22	P2.0-CS3-	I/0 - SPI Chip Enable Output (Master Mode)
23	P2.1-CS2-	I/0 - SPI Chip Enable Output (Master Mode)
24	P2.2-CS1-	I/0 - SPI Chip Enable Output (Master Mode)
25	P2.3-CS0-	I/0 - SPI Chip Enable Output (Master Mode)
26	P2.4-SS-	I/0 - SPI Chip Enable Output (Slave Mode)
27	P2.5-SCK	I/0 - SPI Clock (Input in Slave Mode)
28	P2.6-SDO	I/0 - SPI Data Output Bus
29	P2.7-SDI	I/0 - SPI Data Input Bus
30	VDD	Digital Supply
31	P1.4	I/0
32	P1.5	I/0
33	P1.6	I/0
34	P1.7	I/0
35	OSC1	Oscillator Crystal Output
36	OSC0	Oscillator Crystal input/External Clock Source Input
37	P3.0-TX0	I/0 - Asynchronous UART0 Transmitter Output
38	P3.1-RX0	I/0 - Asynchronous UART0 Receiver Input
39	P3.2-T0IN	I/0 - Timer/Counter 0 Input
40	VDD	5V Digital
41	P3.3-CCU0	I/0 - Capture and Compare Unit 0 Input
42	P3.4-CCU1	I/0 - Capture and Compare Unit 1 Input
43	P3.5-T1IN	I/0 - Timer/Counter 1 Input
44	VPP	Flash Programming Voltage Input
45	P3.6-SDA	I/0 - I2C Bi-Directional Data Bus
46	VTRIM	Reserved
47	NC	Not Connected
48	P3.7-SCL	I/0 - I2C Clock
49	AGND	Analog Ground
50	INT0	External interrupt Input (Negative Level or Edge Triggered)
51	PM	Mode Control Input
52	RES-	Hardware Reset Input
53	ISRCOUT-TA	Programmable Current Source Analog Output
54	ISRCIN	Programmable Current Source Input
55	POT2A	Digitally Controlled Potentiometer 2A
56	POT2B	Digitally Controlled Potentiometer 2B
57	VDDA	Analog Supply
58	ADCI3	Analog to Digital Converter 3 Input
59	ADCI2	Analog to Digital Converter 2 Input
60	ADCI1	Analog to Digital Converter 1 Input
61	ADCI0	Analog to Digital Converter 0 Input
62	XTVREF	External Reference Voltage Input
63	AGND	Analog Ground
64	OPOUT	Output of the Operational Amplifier

FIGURE 3: VERSA MIX PINOUT OF QFP-64-1 PACKAGE



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Absolute Maximum Ratings

V_{DD} to DGND	–0.3V, +6V
V_{DDA} to DGND	-0.3V, +6V
AGND to DGND	–0.3V, +0.3V
V_{DD} to V_{DDA}	-0.3V, +0.3V
ADCI(0-3) to AGND	-0.3V, V_{DDA}+0.3V
XTVREF to AGND	-0.3V, V_{DDA}+0.3V
Digital Input Voltage to DGND	-0.3V, V_{DD}+0.3V
RS422/485 Minimum and maximum Voltages	-2V, +7V
Digital Output Voltage to DGND	–0.3V, V_{DD}+0.3V
V_{PP} to DGND	+13V
Power Dissipation	
• To +75°C	1000mW
• Derate above +75°C	10mW/°C
Operating Temperature range	-40° to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10sec)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

TABLE 2: ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS (V_{DD} = +5V, V_{DDA} = +5V, T_A = +25°C, 16MHz input clock, unless otherwise noted.)						
Power Supply Voltage	V_{DD}		4.5	5.0	5.5	V
	V_{DDA}		4.5	5.0	5.5	V
Power Supply Current	I_{DD}			TBD		mA
	I_{DDA}			TBD		
Flash Programming Voltage	V_{PP}		11		13	V
DIGITAL INPUTS						
Minimum High-Level Input Voltage	V_{IH}	V_{DD} = +5V		2.0		V
Maximum Low-Level Input Voltage	V_{IL}	V_{DD} = +5V		0.8		V
Input Current	I_{IN}			±0.05		µA
Input Capacitance	C_{IN}			5	10	pF
DIGITAL OUTPUTS						
Minimum High-Level Output Voltage	V_{OH}	I_{SOURCE} = 4mA		4.2		V
Maximum Low-Level Output Voltage	V_{OL}	I_{SINK} = 4mA		0.2		V
Output Capacitance	C_{OUT}			10	15	pF
Tri-state Output Leakage Current	I_{OZ}				0.25	µA

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUTS						
ADCI(0-3) Input Voltage Range	V_{ADCI}		0		2.7	V
ADCI(0-3) Input Resistance	R_{ADCI}			100		MΩ
ADCI(0-3) Input Capacitance	C_{ADCI}			5		pF
ADCI(0-3) Input Leakage Current	I_{ADCI}			TBD		nA
Channel-to-Channel Crosstalk					-72 (12 bit)	dB
ANALOG OUTPUT						
TA Output Voltage	$V_{TA}=V_{ADCI(0-3)}$			TBD		V
	$V_{TA}=V_{BGI}$			TBD		
	$V_{TA}=V_{SR}$			200/800		MV
TA Output Drive Capabilities (Maximum Load Resistance)	$V_{TA}=V_{ADCI(0-3)}$		10			kΩ
	$V_{TA}=V_{BGI}$	Requires buffering				
	$V_{TA}=V_{BGH}$	Requires buffering	10			
	$V_{TA}=V_{ADC}$		10			
	$V_{TA}=V_{SR}$		buffer			
TA Output Drive Capabilities (Maximum Load Capacitance)	$V_{TA}=V_{ADCI(0-3)}$				50	pF
	$V_{TA}=V_{BGI}$	Requires buffering			15	
	$V_{TA}=V_{SR}$				5	
CURRENT SOURCE						
ISRC Current Drive	I_{ISRC}			33/133	530	µA
ISRC Output Resistance	R_{ISRC}			50		MΩ
ISRC Output Capacitance	C_{ISRC}			25		pF
ISRCIN Input Reference Resistance	R_{RESIN}			100		MΩ
ISRCIN Input Reference Capacitance	C_{RESIN}			5		pF
INTERNAL REFERENCE						
Bandgap Reference Voltage				1.23V		V
Bandgap Reference Tempco				50		ppm/°C
EXTERNAL REFERENCE						
Input Impedance	R_{XTVREF}			150		kΩ
PGA						
PGA Gain adjustment			2.11		2.29	V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG TO DIGITAL CONVERTER						
ADC Resolution				12		Bits
Differential Non linearity	DNL	No missing codes guaranteed			±1	LSB
Integral Non linearity	INL				±1	LSB
Full-Scale Error (Gain Error)		All channels, ADCI(0-3)		±4		LSB
Offset Error		All channels, ADCI(0-3)		±0.5		LSB
Channel-to-Channel Mismatch		All channels, ADCI(0-3)		±0.5		LSB
Conversion Time		4 channels			1.75	ms
		Single Channel			0.5	
RS-485 TRANSCEIVER						
Input Voltage	V_I		-2		+7	V
Input Impedance	Z_{IN}			1		MΩ

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Drive Current Source				1		mA
USER OP-AMP						
Output Impedance	Zout			20		mΩ
Voltage Gain	G_v			105		dB
Unit Gain Bandwidth	UGBW			5		MHz
Load Resistance to Ground				10		kΩ
Load Capacitance				20		pF
Slew rate	SR			5		V/µs
Power Dissipation	P_D	TA= 25°C		1150		µW
Input Offset Voltage	V_{IO}			TBM		
Input Voltage Range	$V_{I®}$		0		4	V
Common Mode Rejection Ratio	CMRR	Taken at 1kHz		-75		dB
Power Supply Rejection Ratio	PSRR	Taken at 1kHz (20dB/decade)	-75 (Vdd)		-94 (Vss)	dB
Output Voltage Swing	$V_{O(P-P)}$		0.1		4.9	V
Short Circuit Current to ground	I_{IC}			86		mA
Gain Bandwidth Product	GBW			525		MdB
DIGITAL POTENTIOMETER						
Number of Steps (8 bit binary weighted) 32k, 5kp of 125 ohms				256		steps
Minimum resistance			TBD	400	TBD	Ω
Absolute Linearity				0.2		%
Relative Linearity				0.2		%
Interchannel Matching				1		%
-3dB Cutoff Frequency	f_{cutoff}		1.5		125	MHz
Total Harmonic Distortion	THD+N	Taken at 1kHz	0.0001		0.001	%
Temperature Coefficient				0.16		%/°C
Inherent Capacitance				0.5		pF
DIGITAL SWITCHES						
Switch on Resistance			20		80	Ω
Switch turn on time				1		ns
Switch turn off time				1		ns
Inherent capacitance				2		pF
Voltage range on Pin			0		5	V

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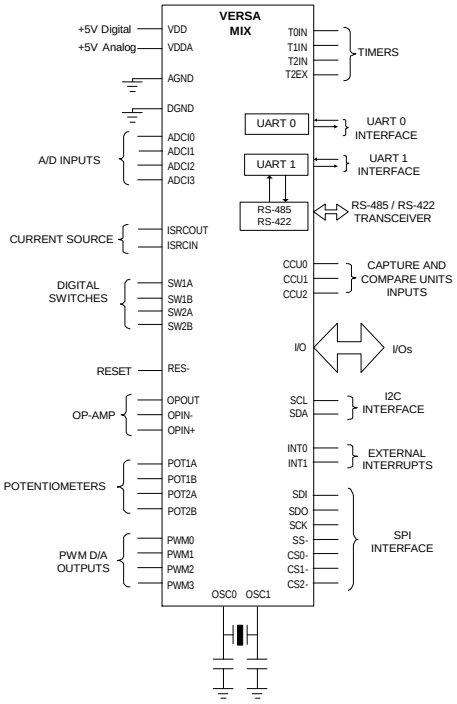
Detailed Description

The following sections will describe the VERSA MIX architecture and peripherals.

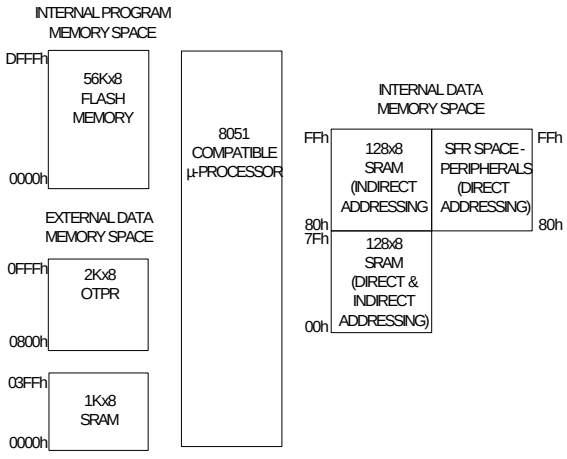
FIGURE 4: INTERFACE DIAGRAM FOR THE VERSA MIX



Memory Organization

The following figure shows the memory organization of the VERSA MIX.

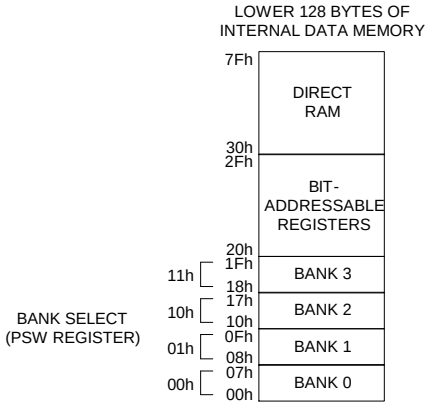
FIGURE 5: MEMORY ORGANIZATION OF THE VERSA MIX



At power-up/reset, the code is executed from the 56Kx8 Flash memory mapped into the processor's internal ROM space. An extra 2Kx8 of Secondary Flash memory is mapped into the external data memory space.
Note that 0000–0005h and 0195–0210h are reserved in the OTP. A 1Kx8 block of SRAM is also mapped into the external data memory of the VERSA MIX. This block can be used as a general-purpose scratch pad or storage memory. A 256x8 block of SRAM is mapped to the internal data memory space. This block of RAM is broken into 2 sub-blocks, with the upper block accessible via indirect addressing only, and the lower block accessible via both direct and indirect addressing.

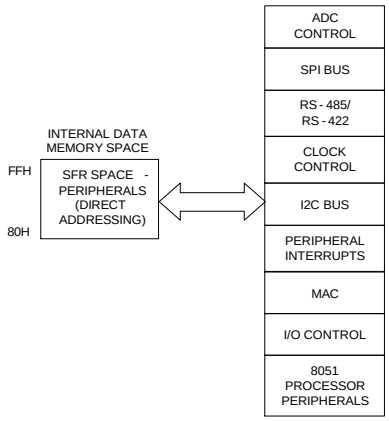
The following figure describes the access to the lower block of 128 bytes.

FIGURE 6: LOWER 128 BYTES BLOCK INTERNAL MEMORY MAP



The SFR (Special Function Register) space is also mapped into the upper 128 bytes of internal data memory space. This SFR space is accessible via direct-access only. The SFR space provides the interface to all the on-chip peripherals. The following figure describes this interface.

FIGURE 7: SFR ORGANIZATION



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Dual Data Pointers

The VERSA MIX employs dual data pointers to accelerate data memory block moves. The standard 8051 data pointer (DPTR) is a 16-bit value used to address external data RAM or peripherals. The VERSA MIX maintains the standard data pointer as DPTR0 at SFR locations 82h and 83h.

The VERSA MIX adds a second data pointer (DPTR1) at SFR Locations 84h and 85h. The SEL bit in the data pointer select register, DPS (SFR 86h), selects which data pointer is active. When SEL = 1, instructions that use the data pointer will use DPL0 and DPH0. When SEL = 1, instructions that use the DPTR will use DPL1 and DPH1. SEL is the bit 0 of SFR location 86h. No other bits of SFR location 86h are used.

All DPTR-related instructions use the currently selected data pointer. In order to switch the active pointer, toggle the SEL bit. The fastest way to do so is to use the increment instruction (INC DPTR). This requires only one instruction to switch from a source address and destination address. This will prevent application code from having to save source and destination addresses when doing a block move.

Using dual data pointers significantly increases efficiency when moving large blocks of data. The SFR locations and register representations related to the dual data pointers are:

TABLE 3: (DPH0) DATA POINTER HIGH 0 - SFR 83H

15	14	13	12	11	10	9	8
DPH0 [7:0]							

TABLE 4: (DPL0) DATA POINTER LOW 0 - SFR 82H

7	6	5	4	3	2	1	0
DPL0 [7:0]							

Bit	Mnemonic	Function
15-8	DPH0	Data pointer high 0. Used to access external code or data space.
7-0	DPL0	Data pointer low 0. Used to access external code or data space.

TABLE 5: (DPH1) DATA POINTER HIGH 1 - SFR 85H

15	14	13	12	11	10	9	8
DPH1 [7:0]							

TABLE 6: (DPL1) DATA POINTER LOW 1 - SFR 84H

7	6	5	4	3	2	1	0
DPL1 [7:0]							

Bit	Mnemonic	Function
15-8	DPH1	Data pointer high 1. Used to access external code or data space.
7-0	DPL1	Data pointer low 1. Used to access external code or data space.

TABLE 7: (DPS) DATA POINTER SELECT REGISTER - SFR 86H

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	SEL

Bit	Mnemonic	Function
7-1	0	Always zero
0	SEL	Used to toggle between both data pointers

MPAGE Register

The MPAGE register controls the upper 8 bits when we perform the MOVX instruction. It is used for external RAM jump control.

TABLE 8: (MPAGE) MEMORY PAGE - SFR CFH

7	6	5	4	3	2	1	0
MPAGE [7:0]							

User Flags

The VERSA MIX provides an SFR register that gives the user the ability to define software flags. It is for this purpose that each bit in this register is individually addressable. This register may also be used as a general-purpose storage location. Thus, the user flag feature allows the VERSA MIX to better adapt to each specific application.

The register is located at SFR address F8h and may be represented as follows:

TABLE 9: (USERFLAGS) USER FLAG - SFR F8H

7	6	5	4	3	2	1	0
TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

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Instruction Set

All VERSA MIX instructions are binary code compatible and perform the same functions as the industry standard 8051. However, the timing of the instructions is different. The following two tables describe the instruction set of the VERSA MIX.

TABLE 10: LEGEND FOR INSTRUCTION SET TABLE

Symbol	Function
A	Accumulator
Rn	Register R0-R7
Direct	Internal register address
@Ri	Internal register pointed to by R0 or R1 (except MOVX)
rel	Two's complement offset byte
bit	Direct bit address
#data	8-bit constant
#data 16	16-bit constant
addr 16	16-bit destination address
addr 11	11-bit destination address

TABLE 11: VERSA MIX INSTRUCTION SET

Mnemonic	Description	Size (bytes)	Instr. Cycles
Arithmetic instructions			
ADD A, Rn	Add register to A	1	1
ADD A, direct	Add direct byte to A	2	2
ADD A, @Ri	Add data memory to A	1	2
ADD A, #data	Add immediate to A	2	2
ADDC A, Rn	Add register to A with carry	1	1
ADDC A, direct	Add direct byte to A with carry	2	2
ADDC A, @Ri	Add data memory to A with carry	1	2
ADDC A, #data	Add immediate to A with carry	2	2
SUBB A, Rn	Subtract register from A with borrow	1	1
SUBB A, direct	Subtract direct byte from A with borrow	2	2
SUBB A, @Ri	Subtract data mem from A with borrow	1	2
SUBB A, #data	Subtract immediate from A with borrow	2	2
INC A	Increment A	1	1
INC Rn	Increment register	1	2
INC direct	Increment direct byte	2	3
INC @Ri	Increment data memory	1	3
DEC A	Decrement A	1	1
DEC Rn	Decrement register	1	2
DEC direct	Decrement direct byte	2	3
DEC @Ri	Decrement data memory	1	3
INC DPTR	Increment data pointer	1	1
MUL AB	Multiply A by B	1	5
DIV AB	Divide A by B	1	5
DA A	Decimal adjust A	1	1
Logical Instructions			
ANL A, Rn	AND register to A	1	1
ANL A, direct	AND direct byte to A	2	2
ANL A, @Ri	AND data memory to A	1	2
ANL A, #data	AND immediate to A	2	2
ANL direct, A	AND A to direct byte	2	3
ANL direct, #data	AND immediate data to direct byte	3	4
ORL A, Rn	OR register to A	1	1
ORL A, direct	OR direct byte to A	2	2
ORL A, @Ri	OR data memory to A	1	2
ORL A, #data	OR immediate to A	2	2
ORL direct, A	OR A to direct byte	2	3
ORL direct, #data	OR immediate data to direct byte	3	4
XRL A, Rn	Exclusive-OR register to A	1	1
XRL A, direct	Exclusive-OR direct byte to A	2	2
XRL A, @Ri	Exclusive-OR data memory to A	1	2
XRL A, #data	Exclusive-OR immediate to A	2	2
XRL direct, A	Exclusive-OR A to direct byte	2	3
XRL direct, #data	Exclusive-OR immediate to direct byte	3	4
CLR A	Clear A	1	1
CPL A	Compliment A	1	1
SWAP A	Swap nibbles of A	1	1
RLA	Rotate A left	1	1
RLC A	Rotate A left through carry	1	1
RRA	Rotate A right	1	1
RRCA	Rotate A right through carry	1	1
Data Transfer Instructions			
MOV A, Rn	Move register to A	1	1
MOV A, direct	Move direct byte to A	2	2
MOV A, @Ri	Move data memory to A	1	2
MOV A, #data	Move immediate to A	2	2
MOV Rn, A	Move A to register	1	2
MOV Rn, direct	Move direct byte to register	2	4
MOV Rn, #data	Move immediate to register	2	2
MOV direct, A	Move A to direct byte	2	3
MOV direct, Rn	Move register to direct byte	2	3
MOV direct, direct	Move direct byte to direct byte	3	4
MOV direct, @Ri	Move data memory to direct byte	2	4
MOV direct, #data	Move immediate to direct byte	3	3
MOV @Ri, A	Move A to data memory	1	3
MOV @Ri, direct	Move direct byte to data memory	2	5
MOV @Ri, #data	Move immediate to data memory	2	3
MOV DPTR, #data	Move immediate to data pointer	3	3
MOVC A, @A+DPTR	Move code byte relative DPTR to A	1	3
MOVC A, @A+PC	Move code byte relative PC to A	1	3
MOVX A, @Ri	Move external data (A8) to A	1	3-10
MOVX A, @DPTR	Move external data (A16) to A	1	3-10
MOVX @Ri, A	Move A to external data (A8)	1	4-11
MOVX @DPTR, A	Move A to external data (A16)	1	4-11
PUSH direct	Push direct byte onto stack	2	4
POP direct	Pop direct byte from stack	2	3
XCH A, Rn	Exchange A and register	1	2
XCH A, direct	Exchange A and direct byte	2	3
XCH A, @Ri	Exchange A and data memory	1	3
XCHD A, @Ri	Exchange A and data memory nibble	1	3
Branching Instructions			
ACALL addr 11	Absolute call to subroutine	2	6
LCALL addr 16	Long call to subroutine	3	6
RET	Return from subroutine	1	4
RETI	Return from interrupt	1	4
AJMP addr 11	Absolute jump unconditional	2	3
LJMP addr 16	Long jump unconditional	3	4
SJMP rel	Short jump (relative address)	2	3
JC rel	Jump on carry = 1	2	3
JNC rel	Jump on carry = 0	2	3
JB bit, rel	Jump on direct bit = 1	3	4
JNB bit, rel	Jump on direct bit = 0	3	4
JBC bit, rel	Jump on direct bit = 1 and clear	3	4
JMP @A+DPTR	Jump indirect relative DPTR	1	2
JZ rel	Jump on accumulator = 0	2	3
JNZ rel	Jump on accumulator 1= 0	2	3
CJNE A, direct, rel	Compare A, direct JNE relative	3	4
CJNE A, #d, rel	Compare A, immediate JNE relative	3	4
CJNE Rn, #d, rel	Compare reg, immediate JNE relative	3	4
CJNE @Ri, #d, rel	Compare ind, immediate JNE relative	3	4
DJNZ Rn, rel	Decrement register, JNZ relative	2	3
DJNZ direct, rel	Decrement direct byte, JNZ relative	3	4
Miscellaneous Instruction			
NOP	No operation	1	1

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Special Function Registers

The Special Function Registers (SFRs) control several of the features of the VERSA MIX. Many of the VERSA MIX SFRs are identical to the standard 8051 SFRs. However, there are additional SFRs that control the VESRA MIX's specific peripheral features that are not available in the standard 8051.

TABLE 12: SPECIAL FUNCTION REGISTERS

SFR Register	SFR Adrs	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Value
P0	80h	-	-	-	-	-	-	-	-	1111 1111b
SP	81h	-	-	-	-	-	-	-	-	0000 0111b
DPL0	82h	-	-	-	-	-	-	-	-	0000 0000b
DPH0	83h	-	-	-	-	-	-	-	-	0000 0000b
DPL1	84h	-	-	-	-	-	-	-	-	0000 0000b
DPH1	85h	-	-	-	-	-	-	-	-	0000 0000b
DPS	86h	0	0	0	0	0	0	0	SEL	0000 0000b
PCON	87h	SMOD_0	-	-	-	GF1	GF0	STOP	IDLE	0000 0000b
TCON	88h	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	0000 0000b
TMOD	89h	GATE_1	C/T_1	M1_1	M0_1	GATE_0	C/T_0	M1_0	M0_0	0000 0000b
TL0	8Ah	-	-	-	-	-	-	-	-	0000 0000b
TL1	8Bh	-	-	-	-	-	-	-	-	0000 0000b
TH0	8Ch	-	-	-	-	-	-	-	-	0000 0000b
TH1	8Dh	-	-	-	-	-	-	-	-	0000 0000b
CKCON	8Eh	-	-	-	-	-	STRETCH_2	STRETCH_1	STRETCH_0	0000 0000b
	8Fh									
P1	90h	-	-	-	-	-	-	-	-	1111 1111b
IRCON	91h	EXF2	TF2	IEX6	IEX5	IEX4	IEX3	IEX2	IADC	0000 0000b
ANALOGPWREN	92h	OPAMPEN	DIGPOTEN	ISRCSEL	ISRCEN	TAEN	ADCEN	PGAEN	BGAPEN	0000 0000b
DIGPWREN	93h	T2CLKEN	WDOGEN	MACEN	I2CEN	SPIEN	UART1DIFFEN	UART1EN	UART0EN	0000 0000b
CLKDIVCTRL	94h	SOFTRST	-	-	IRQNORMSPD	MCKDIV_3	MCKDIV_2	MCKDIV_1	MCKDIV_0	0000 0000b
ADCCLKDIV	95h	-	-	-	-	-	-	-	-	0000 0000b
S0RELL	96h	-	-	-	-	-	-	-	-	11011001b
S0RELH	97h	0	0	0	0	0	0	-	-	0000 0011b
S0CON (SCON)	98h	SM0	SM1	SM20	REN0	TB80	RB80	TI0	RI0	0000 0000b
S0BUF (SBUF)	99h	-	-	-	-	-	-	-	-	0000 0000b
IEN2	9Ah	-	-	-	-	-	-	-	ES1	0000 0000b
P0PINCFG	9Bh	-	-	-	-	RX1EN	TX1EN	T2EXEN	T2INEN	0000 0000b
	9Ch									
P2PINCFG	9Dh	SDIEN	SDOEN	SCKEN	SSEN	CS0EN	CS1EN	CS2EN	CS3EN	0000 0000b
P3PINCFG	9Eh	MSCLEN	MSDAEN	T1INEN	CCU1EN	CCU0EN	T0INEN	RX0EN	TX0EN	0000 0000b
PORTIRQEN	9Fh	P07IEN	P06IEN	P05IEN	P04IEN	P03IEN	P02IEN	P01IEN	P00IEN	0000 0000b
P2	A0h	-	-	-	-	-	-	-	-	1111 1111b
PORTIRQSTAT	A1h	P07ISTAT	P06ISTAT	P05ISTAT	P04ISTAT	P03ISTAT	P02ISTAT	P01ISTAT	P00ISTAT	0000 0000b
ADCCTRL	A2h	ADCIRGCLR	XVREFCAP	CALSKIP	ADCIRQ	ADCIE	ONECHAN	CONT	ONESHOT	0000 0000b
ADCCONVRLOW	A3h	-	-	-	-	-	-	-	-	0000 0000b
ADCCONVRMED	A4h	-	-	-	-	-	-	-	-	0000 0000b
ADCCONVRHIGH	A5h	-	-	-	-	-	-	-	-	0000 0000b
ADCD0LO	A6h	-	-	-	-	-	-	-	-	0000 0000b
ADCD0HI	A7h					ADCD0HI_3	ADCD0HI_2	ADCD0HI_1	ADCD0HI_0	0000 0000b
IEN0	A8h	EA1	WDT	ET2	ES0	ET1	EX1	ET0	EX0	0000 0000b
ADCD1LO	A9h	-	-	-	-	-	-	-	-	0000 0000b
ADCD1HI	AAh					ADCD1HI_3	ADCD1HI_2	ADCD1HI_1	ADCD1HI_0	0000 0000b
ADCD2LO	ABh	-	-	-	-	-	-	-	-	0000 0000b
ADCD2HI	ACh					ADCD2HI_3	ADCD2HI_2	ADCD2HI_1	ADCD2HI_0	0000 0000b
ADCD3LO	ADh	-	-	-	-	-	-	-	-	0000 0000b
ADCD3HI	AEh					ADCD3HI_3	ADCD3HI_2	ADCD3HI_1	ADCD3HI_0	0000 0000b
	AFh									
P3	B0h	-	-	-	-	-	-	-	-	1111 1111b
ADCFORCE	B1h	ADCFORCE	QNUMBER_2	QNUMBER_1	QNUMBER_0	QVALUE_3	QVALUE_2	QVALUE_1	QVALUE_0	0000 0000b
ADCALTBL	B2h	ADCALDATA_3	ADCALDATA_2	ADCALDATA_1	ADCALDATA_0	ADCALADRS_3	ADCALADRS_2	ADCALADRS_1	ADCALADRS_0	0000 0000b
BGAPCAL	B3h	-	-	-	-	-	-	-	-	0000 0000b
PGACAL	B4h	-	-	-	-	-	-	-	-	0000 0000b
INMUXCTRL	B5h	NOT USED	ADCINSEL_2	ADCINSEL_1	ADCINSEL_0	AINEN_3	AINEN_2	AINEN_1	AINEN_0	0000 0000b
OUTMUXCTRL	B6h	-	-	-	-	-	TAOUTSEL_2	TAOUTSEL_1	TAOUTSEL_0	0000 0000b
SWITCHCTRL	B7h	SWITCH2_3	SWITCH2_2	SWITCH2_1	SWITCH2_0	SWITCH1_3	SWITCH1_2	SWITCH1_1	SWITCH1_0	0000 0000b
IP0	B8h	0WDS	WDTS	IP0.5	IP0.4	IP0.3	IP0.2	IP0.1	IP0.0	0000 0000b
IP1	B9h	-	-	IP1.5	IP1.4	IP1.3	IP1.2	IP1.1	IP1.0	0000 0000b
DIGPOT1	BAh	-	-	-	-	-	-	-	-	0000 0000b

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SFR Register	SFR Adrs	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Value
DIGPOT2	BBh	-	-	-	-	-	-	-	-	0000 0000b
ISRCCAL1	BCh	PGACAL0	ISRCCAL1_6	ISRCCAL1_5	ISRCCAL1_4	ISRCCAL1_3	ISRCCAL1_2	ISRCCAL1_1	ISRCCAL1_0	0000 0000b
ISRCCAL2	BDh	-	ISRCCAL2_6	ISRCCAL2_5	ISRCCAL2_4	ISRCCAL2_3	ISRCCAL2_2	ISRCCAL2_1	ISRCCAL2_0	0000 0000b
S1RELL	BEh	-	-	-	-	-	-	-	-	0000 0000b
S1RELH	BFh	-	-	-	-	-	-	-	-	0000 0000b
S1CON	C0h	SM	-	SM21	REN1	TB81	RB81	TI1	RI1	0000 0000b
S1BUF	C1h	-	-	-	-	-	-	-	-	0000 0000b
CCL1	C2h	-	-	-	-	-	-	-	-	0000 0000b
CCH1	C3h	-	-	-	-	-	-	-	-	0000 0000b
CCL2	C4h	-	-	-	-	-	-	-	-	0000 0000b
CCH2	C5h	-	-	-	-	-	-	-	-	0000 0000b
CCL3	C6h	-	-	-	-	-	-	-	-	0000 0000b
CCH3	C7h	-	-	-	-	-	-	-	-	0000 0000b
T2CON	C8h	T2PS	T2PSM	T2S	T2R1	T2R0	T2CM	T2I1	T2I0	0000 0000b
CCEN	C9h	COCAH3	COCAL3	COCAH2	COCAL2	COCAH1	COCAL1	COCAH0	COCAL0	0000 0000b
CRCL	CAh	-	-	-	-	-	-	-	-	0000 0000b
CRCH	CBh	-	-	-	-	-	-	-	-	0000 0000b
TL2	CCh	-	-	-	-	-	-	-	-	0000 0000b
TH2	CDh	-	-	-	-	-	-	-	-	0000 0000b
	CEh									
MPAGE	CFh	-	-	-	-	-	-	-	-	0000 0000b
PSW	D0h	CY	AC	F0	RS1	RS	OV	-	P	0000 0000b
BREAKP0L	D1h	-	-	-	-	-	-	-	-	1111 1111b
BREAKP0H	D2h	-	-	-	-	-	-	-	-	1111 1111b
BREAKP1L	D3h	-	-	-	-	-	-	-	-	1111 1111b
BREAKP1H	D4h	-	-	-	-	-	-	-	-	1111 1111b
BREAKPCTRL	D5h	-	-	B1_EN	B0_EN	-	-	B1_CLR	B0_CLR	0000 0000b
DEBUGCTRL	D6h	FORCE_DEBUG_INT	-	-	-	I2C_EN	UART1EN	UART0EN	SPI_EN	0000 0000b
DEBUGSTATUS	D7h	FORCE_DEBUG_INT	PER_INT	-	-	-	-	BKP1	BKP0	0000 0000b
WDCON	D8h	WDCON	-	-	-	-	-	-	-	0000 0000b
WDTREL	D9h	PRES	WDTREL.6	WDTREL.5	WDTREL.4	WDTREL.3	WDTREL.2	WDTREL.1	WDTREL.0	0000 0000b
I2CCONFIG	DAh	I2CMASKID	I2CRXOVIE	I2CRXDAVIE	I2CTXEMPIE	I2CMANACK	I2CACKMODE	I2CMSTOP	I2CMASTER	0000 0010b
I2CCLKCTRL	DBh	-	-	-	-	-	-	-	-	0000 0000b
I2CCHIPID	DCh	I2CID_6	I2CID_5	I2CID_4	I2CID_3	I2CID_2	I2CID_1	I2CID_0	I2CWID	0100 0010b
I2CIRQSTAT	DDh	I2CGOTSTOP	I2CNOACK	I2CSDASYNC	I2CDATACK	I2CIDLE	I2CRXOV	I2CRXAV	I2CTXEMP	0010 1001b
I2CRXTX	DEh	-	-	-	-	-	-	-	-	0000 0000b
	DFh									
ACC	E0h	-	-	-	-	-	-	-	-	0000 0000b
SPIRXTX0	E1h	SPIRXTX0_7	SPIRXTX0_6	SPIRXTX0_5	SPIRXTX0_4	SPIRXTX0_3	SPIRXTX0_2	SPIRXTX0_1	SPIRXTX0_0	0000 0000b
SPIRXTX1	E2h	SPIRXTX1_15	SPIRXTX1_14	SPIRXTX1_13	SPIRXTX1_12	SPIRXTX1_11	SPIRXTX1_10	SPIRXTX1_9	SPIRXTX1_8	0000 0000b
SPIRXTX2	E3h	SPIRXTX2_23	SPIRXTX2_22	SPIRXTX2_21	SPIRXTX2_20	SPIRXTX2_19	SPIRXTX2_18	SPIRXTX2_17	SPIRXTX2_16	0000 0000b
SPIRXTX3	E4h	SPIRXTX3_31	SPIRXTX3_30	SPIRXTX3_29	SPIRXTX3_28	SPIRXTX3_27	SPIRXTX3_26	SPIRXTX3_25	SPIRXTX3_24	0000 0000b
SPICTRL1	E5h	SPICK_2	SPICK_1	SPICK_0	SPICS_1	SPICS_0	SPICKPH	SPICKPOL	SPIMA_SL	0000 0001b
SPICTRL2	E6h	SPICSLO	SPICLRTXEMPTO	FSONCS3	SPI LOAD	NOT USED	SPIRXOVIE	SPIRXAVIE	SPITXEMPIE	0000 0000b
SPISIZECTRL	E7h	SPISIZE								0000 0111b
IEN1	E8h	EXEN2	SWDT	EX6	EX5	EX4	EX3	EX2	EADC	0000 0000b
SPIIRQSTAT	E9h	-	-	SPITXEMPTO	SPISLAVESEL	SPISEL	SPIOV	SPIRAXV	SPITXEMP	00011001b
	EAh									
MACCTRL	EBh	LOADPREV	PREVMODE	OVMODE	OVRDVAL	ADDSRC_1	ADDSRC_0	MULCMD_1	MULCMD_0	0000 0000b
MACC0	ECh	-	-	-	-	-	-	-	-	0000 0000b
MACC1	EDh	-	-	-	-	-	-	-	-	0000 0000b
MACC2	EEh	-	-	-	-	-	-	-	-	0000 0000b
MACC3	EFh	-	-	-	-	-	-	-	-	0000 0000b
B	F0h	-	-	-	-	-	-	-	-	0000 0000b
MACCTRL2	F1h	MACCLR2_2	MACCLR2_1	MACCLR2_0	MACOV32IE	-	-	MACOV16	MACOV32	0000 0000b
MACA0	F2h	-	-	-	-	-	-	-	-	0000 0000b
MACA1	F3h	-	-	-	-	-	-	-	-	0000 0000b
MACRES0	F4h	-	-	-	-	-	-	-	-	0000 0000b
MACRES1	F5h	-	-	-	-	-	-	-	-	0000 0000b
MACRES2	F6h	-	-	-	-	-	-	-	-	0000 0000b
MACRES3	F7h	-	-	-	-	-	-	-	-	0000 0000b
USERFLAGS	F8h	-	-	-	-	-	-	-	-	0000 0000b
MACB0	F9h	-	-	-	-	-	-	-	-	0000 0000b
MACB1	FAh	-	-	-	-	-	-	-	-	0000 0000b
MACSHIFTCTRL	FBh	SHIFTMODE	ALSHSTYLE	SHIFTAMPL_5	SHIFTAMPL_4	SHIFTAMPL_3	SHIFTAMPL_2	SHIFTAMPL_1	SHIFTAMPL_0	0000 0000b
MACPREV0	FCh	-	-	-	-	-	-	-	-	0000 0000b
MACPREV1	FDh	-	-	-	-	-	-	-	-	0000 0000b
MACPREV2	FEh	-	-	-	-	-	-	-	-	0000 0000b
MACPREV3	FFh	-	-	-	-	-	-	-	-	0000 0000b

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Peripheral Interfaces

MAC

MAC Features

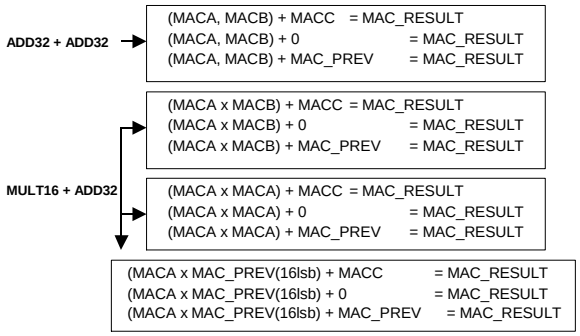
The VERSA MIX includes a multiply-accumulator that can be used to significantly speed up arithmetic operations.

The following is a list that describes of features of the MAC unit.

- Hardware Calculation Engine
- Calculation result is ready as soon as the input registers are loaded
- Signed mathematical calculations
- Auto/Manual reload of MAC_RES
- Enhanced VERSA MIX MAC Unit

The MAC block allows the following operations to be performed:

FIGURE 8: VERSA MIX MAC OPERATION



Where MACA (multiplier), MACB (multiplicand), MACACC (accumulator) and MACRESULT (result) are 16, 16, 32 and 32 bits, respectively.

MAC Unit Control Registers

The table below summarizes the exact functions of the MAC unit control registers.

TABLE 13: (MACCTRL) MAC UNIT CONTROL REGISTER - SFR EBH

7	6	5	4
LOADPREV	PREVMODE	OVMODE	OVRDVAL

3	2	1	0
ADDSRC [1:0]		MULCMD [1:0]	

Bit	Mnemonic	Function
7	LOADPREV	Force load of MACPREV register 1 = Manual load of the MACPREV register content if PREVMODE = 1
6	PREVMODE	Loading method of MACPREV register 0 = Automatic load when A0 is written. 1 = Manual Load when 1 is written into LOADPREV
5	OVMODE	Overflow Flags (IRQ) operation mode 0 = Overflow flag active while condition occurs 1 = Overflow flags registered (stay 1)
4	OVRDVAL	Overflowed value read 0 = Value on MACRES Calculation performed 1 = Value read on MACRES is the 32lsb of load when overflow occurred
3:2	ADDSRC	32-bit ADD source 00 = 0 (No Add) 01 = C (std 32-bit reg) 10 = RES –1 11 = TBD
1:0	MULCMD	Multiplication Command 00 = MACA x MACB 01 = MACA x MACA 10 = MACA x MACPREV (16 Lower bits)

TABLE 14: (MACCTRL2) MAC UNIT CONTROL REGISTER 2 -SFR F1H

7	6	5	4
MACCLR2 [2:0]			MACOV32IE

3	2	1	0
-	-	MACOV16	MACOV32

Bit	Mnemonic	Function
7:5	MACCLR	MAC Register Clear 000 = No Clear 001 = Clear MACA 010 = Clear MACB 011 = Clear MACC 100 = Clear MACPREV 101 = Clear All MAC regs + Overflow Flags 110 = Clear Overflow Flags only
4	MACOV32IE	MAC 32-bit Overflow IRQ Enable
3	-	-
2	-	-
1	MACOV16	16-bit Overflow Flag 1 = 16-bit MAC Overflow occurred
0	MACOV32	32-bit Overflow Flag 1 = 32-bit MAC Overflow Load MAC32OV reg can generate IRQ

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MAC Unit Mathematical Manipulation Registers

The MAC includes operation and result registers that serve to store the numbers being manipulated in mathematical operations. Some of these registers are uniquely for addition (such as MACC) while others can be used for all operations. The MAC operation registers are represented below.

TABLE 15: (MACC0) MAC UNIT C OPERAND, LOW BYTE - SFR ECH

7	6	5	4	3	2	1	0
MACC0 [7:0]							

Bit	Mnemonic	Function
7:0	MACC0	Segment of the 32-bit add register

TABLE 16: (MACC1) MAC UNIT C OPERAND, BYTE 1 - SFR EDH

7	6	5	4	3	2	1	0
MACC1 [15:8]							

Bit	Mnemonic	Function
15:8	MACC1	Segment of the 32-bit add register

TABLE 17: (MACC2) MAC UNIT C OPERAND, BYTE 2 - SFR EEH

7	6	5	4	3	2	1	0
MACC2 [23:16]							

Bit	Mnemonic	Function
23:16	MACC2	Segment of the 32-bit add register

TABLE 18: (MACC3) MAC UNIT C OPERAND, HIGH BYTE - SFR EFH

7	6	5	4	3	2	1	0
MACC3 [31:24]							

Bit	Mnemonic	Function
31:24	MACC3	Segment of the 32-bit add register

TABLE 19: (MACA0) MAC UNIT A OPERAND, LOW BYTE - SFR F2H

7	6	5	4	3	2	1	0
MACA0 [7:0]							

Bit	Mnemonic	Function
7:0	MACA0	Segment of a 16-bit mathematical operation register

TABLE 20: (MACA1) MAC UNIT A OPERAND, HIGH BYTE - SFR F3H

7	6	5	4	3	2	1	0
MACA1 [15:8]							

Bit	Mnemonic	Function
15:8	MACA1	Segment of a 16-bit mathematical operation register

TABLE 21: (MACRES0) MAC UNIT RESULT, LOW BYTE - SFR F4H

7	6	5	4	3	2	1	0
MACRES0 [7:0]							

Bit	Mnemonic	Function
7:0	MACRES0	Segment of the 32-bit MAC result register

TABLE 22: (MACRES1) MAC UNIT RESULT, BYTE 1 - SFR F5H

7	6	5	4	3	2	1	0
MACRES1 [15:8]							

Bit	Mnemonic	Function
15:8	MACRES1	Segment of the 32-bit MAC result register

TABLE 23: (MACRES2) MAC UNIT RESULT, BYTE 2 - SFR F6H

7	6	5	4	3	2	1	0
MACRES2 [23:16]							

Bit	Mnemonic	Function
23:16	MACRES2	Segment of the 32-bit MAC result register

TABLE 24: (MACRES3) MAC UNIT RESULT, HIGH BYTE - SFR F7H

7	6	5	4	3	2	1	0
MACRES3 [31:24]							

Bit	Mnemonic	Function
31:24	MACRES3	Segment of the 32-bit MAC result register

TABLE 25: (MACB0) MAC UNIT B OPERAND, LOW BYTE - SFR F9H

7	6	5	4	3	2	1	0
MACB0 [7:0]							

Bit	Mnemonic	Function
7:0	MACB0	Segment of 16-bit MACB register

TABLE 26: (MACB1) MAC UNIT B OPERAND, HIGH BYTE - SFR FAH

7	6	5	4	3	2	1	0
MACB1 [7:0]							

Bit	Mnemonic	Function
7:0	MACB1	Segment of 16-bit MACB register

TABLE 27: (MACPREV0) MAC UNIT PREVIOUS OPERATION RESULT, LOW BYTE - SFR FCH

7	6	5	4	3	2	1	0
MACPREV0 [7:0]							

Bit	Mnemonic	Function
7:0	MACPREV0	Segment of 32-bit MAC previous result register

TABLE 28: (MACPREV1) MAC UNIT PREVIOUS OPERATION RESULT, BYTE 1 - SFR FDH

7	6	5	4	3	2	1	0
MACPREV1 [7:0]							

Bit	Mnemonic	Function
15:8	MACPREV1	Segment of 32-bit MAC previous result register

TABLE 29: (MACPREV2) MAC UNIT PREVIOUS OPERATION RESULT, BYTE 2 - SFR FEH

7	6	5	4	3	2	1	0
MACPREV2 [15:8]							

Bit	Mnemonic	Function
23:16	MACPREV2	Segment of 32-bit MAC previous result register

TABLE 30: (MACPREV3) MAC UNIT PREVIOUS OPERATION RESULT, HIGH BYTE - SFR FFH

7	6	5	4	3	2	1	0
MACPREV3 [7:0]							

Bit	Mnemonic	Function
31:24	MACPREV3	Segment of 32-bit MAC previous result register

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MAC Barrel Shifter

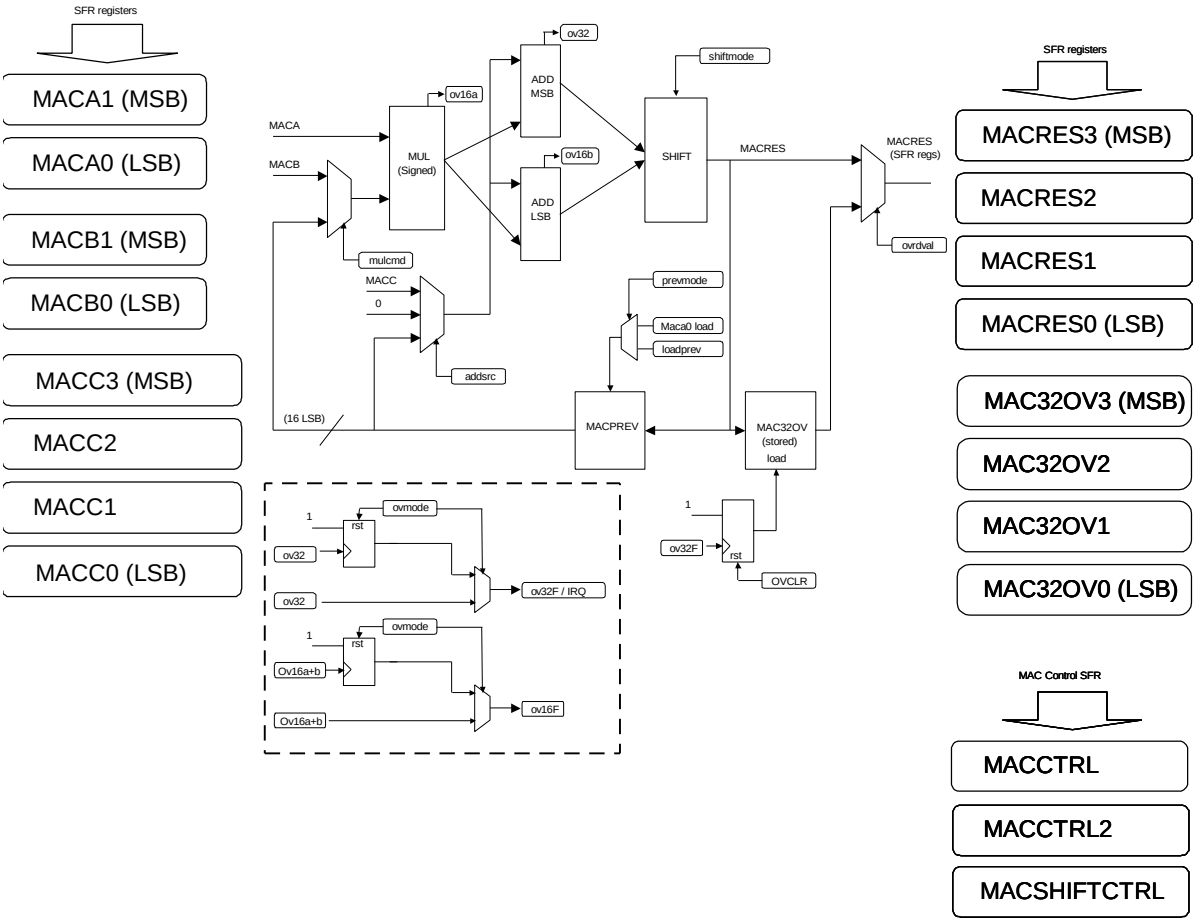
The MAC includes a 32-bit Barrel Shifter at the output of the 32-bit addition unit. This Barrel Shifter can perform right/left shift operations. The shifting range is adjustable from 0 to 16 both ways. The "shifted" addition unit output can be routed to:

- MAC_RES
- MAC_PREV
- MAC_OV32

The barrel shifter also supports arithmetic and logical shifts. Furthermore, arithmetic shift left can be configured to keep or discard the sign bit.

- Unsigned MATH operations are possible if the MUL engine operands are limited to 15 bits in size
- Easy implementation of complex MATH operations
- 32-bit Overflow Flag
- 32-bit Overflow can raise an interrupt to the µP
- MAC operand registers can be cleared individually or all together
- Overflow flags can be configured to stay active until manually cleared
- 16-bit Overflow Flag
- Can store and use results from previous operations

FIGURE 9: VERSA MIX MAC FUNCTIONAL DIAGRAM



The block diagram above shows the interaction between the registers and the other components that comprise the MAC unit on the VERSA MIX.

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TABLE 31: (MACSHIFTCTRL) MAC UNIT BARREL SHIFTER CONTROL REGISTER - SFR FBH

7	6	5	4	3	2	1	0
SHIFTMODE	ALSHSTYLE	SHIFTAMPL [5:0]					

Bit	Mnemonic	Function
7	SHIFTMODE	0 = Logical SHIFT 1 = Arithmetic SHIFT
6	ALSHSTYLE	Arithmetic Shift Left Style 0 = Arithmetic Left Shift = Logical Left 1 = Artith Left Shift keep sign bit
5:0	SHIFTAMPL	Shift Amplitude 0 to 16 (5 bits to provide 16 bits) Negative Number = Shift Right 2 complements Positive Number = Shift Left

TABLE 32: (DIGPWREN) DIGITAL PERIPHERALS POWER ENABLE REGISTER - SFR 93H

7	6	5	4
T2CLKEN	WDOGEN	MACEN	I2CEN

3	2	1	0
SPIEN	UART1DIFFEN	UART1EN	UART0EN

Bit	Mnemonic	Function
7	T2CLKEN	Timer2 / PWM Enable 0 = Timer 2 CLK stopped (reset value) 1 = Timer 2 CLK Running
6	WDOGEN	Watch dog Enable 0 = Watchdog Disabled (reset value) 1 = Watch Dog Enabled
5	MACEN	1 – MAC Enable 0 – MAC Disable
4	I2CEN	1 – I2C Interface Enable 0 – I2C Interface Disable This bit is merged with CLK STOP bit
3	SPIEN	1 – SPI interface Enable 0 – SPI Disable
2	UART1DIFFEN	UART1 Differential Interface Enable 0 = Disable 1 = Enable
1	UART1EN	UART1 Enable 0 = Disable 1 = Enable
0	UART0EN	UART0 Enable 0 = Disable 1 = Enable

Timers/Counters

The VERSA MIX includes 3 general purpose timer/counters (Timer 0, Timer 1, Timer 2) and two 10-bit timers reserved for UARTS. Timer 0 and Timer 1 can operate as either a timer with a clock rate based on the system clock, or as an event counter clocked by the T0IN (Timer 0) and T1IN (Timer 1). Timer 2 can only operate in a 16-bit timer mode. This timer can be used as a serial port baud rate generator.

Each general-purpose timer/counter consists of a 16-bit register that is accessible by software as two SFRs:

- **Timer 0** -TL0 and TH0
- **Timer 1** -TL1 and TH1
- **Timer 2** - TL2 and TH2

TABLE 33: (TL0) TIMER 0 LOW BYTE - SFR 8AH

7	6	5	4	3	2	1	0
TL0 [7:0]							

TABLE 34: (TL1) TIMER 1 LOW BYTE - SFR 8BH

7	6	5	4	3	2	1	0
TL1 [7:0]							

TABLE 35: (TH0) TIMER 0 HIGH BYTE - SFR 8CH

7	6	5	4	3	2	1	0
TH0 [7:0]							

TABLE 36: (TH1) TIMER 1 HIGH BYTE - SFR 8DH

7	6	5	4	3	2	1	0
TH1 [7:0]							

Timers 0 and 1

Timers 0 and 1 each operate in four modes controlled by the TMOD SFR and the TCON SFR (table 37). The four modes are:

- **Mode 0**: **13-bit** timer/counter
- **Mode 1**: **16-bit** timer/counter
- **Mode 2**: **8-bit** counter with auto-reload
- **Mode 3**: **Two 8-bit** counters

The table below represents the TCON special function register of the VERSA MIX. This register contains the Timer 0/1 overflow flags, the timer 0/1 run control bits; the interrupt 0/1 edge flags; and the interrupt 0/1 interrupt type control bits. The detailed bit functions are summarized in the table below.

TABLE 37: (TCON) TIMER 0, TIMER 1 TIMER/COUNTER CONTROL - SFR 88H

7	6	5	4
TF1	TR1	TF0	TR0

3	2	1	0
IE1	IT1	IE0	IT0

Bit	Mnemonic	Function
7	TF1	Timer 1 overflow flag set by hardware when Timer 1 overflows. This flag can be cleared by software and is automatically cleared when interrupt is processed.
6	TR1	Timer 1 Run control bit. If cleared Timer 1 stops.
5	TF0	Timer 0 overflow flag set by hardware when Timer 0 overflows. This flag can be cleared by software and is automatically cleared when interrupt is processed.
4	TR0	Timer 0 Run control bit. If cleared timer 0 stops.
3	IE1	Interrupt 1 edge flag. Set by hardware when falling edge on external INT1 is observed. Cleared when interrupt is processed.
2	IT1	Interrupt 1 type control bit. Selects falling edge or low level on input pin to cause interrupt.
1	IE0	Interrupt 0 edge flag. Set by hardware when falling edge on external pin int1 is observed. Cleared when interrupt is processed.
0	IT0	Interrupt 0 type control bit. Selects falling edge or low level on input pin to cause interrupt.

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The TMOD register allows the user to enable the external gate control and to select a timer or counter operation. Furthermore, one may also select the mode of Timer 1 and 0 by setting bits M1 and M2 of this register.

TABLE 38: (TMOD) TIMER MODE CONTROL - SFR 89H

7	6	5	4
GATE_1	C/T_1	M1_1	M0_1

3	2	1	0
GATE_0	C/T_0	M1_0	M0_0

Bit	Mnemonic	Function
7	GATE_1	If set, enables external gate control (pin INT1 for Counter 1). When INT1 is high, and TRx bit is set (see TCON register), a counter is incremented every falling edge on the T1IN input pin.
6	C/T_1	Selects timer or counter operation. 1 = A counter operation is performed 0 = The corresponding register will function as a timer.
5	M1_1	Selects mode for Timer/Counter 1, as shown in Table 39.
4	M0_1	Selects mode for Timer/Counter 1, as shown in Table 39.
3	GATE_0	If set, enables external gate control (pin INT0 for Counter 0). When INT0 is high, and TRx bit is set (see TCON register), a counter is incremented every falling edge on the T0IN input pin.
2	C/T_0	Selects timer or counter operation. 1 = A counter operation is performed 0 = The corresponding register will function as a timer.
1	M1_0	Selects mode for Timer/Counter 0, as shown in Table 39.
0	M0_0	Selects mode for Timer/Counter 0, as shown in Table 39.

The table below summarizes the four modes of operation of Timers 0 and 1. These modes are determined by bits M1 and M0 of the TMOD Special Function Register (Table 38 above).

TABLE 39: TIMER/COUNTER MODE DESCRIPTION SUMMARY

M1	M0	Mode	Function
0	0	Mode 0	13-bit Counter/Timer, with 5 lower bits in TL0 or TL1 register and bits in TH0 or TH1 register (for timer 0 and timer, respectively). The 3 high order bits of TL0 and TL1 are held at 0.
0	1	Mode 1	16-bit Counter/Timer
1	0	Mode 2	8-bit auto-reload Counter/Timer. The reload value is kept in TH0 or TH1, while TL0 or TL1 is incremented every machine cycle. When TLx overflows, a value from THx is copied to TLx.
1	1	Mode 3	If Timer 1 M1 and M0 bits are set to 1, Timer 1 stops. If Timer 0 M1 and M0 bits are set to 1, Timer 0 acts as two independent 8-bit Timers/Counters.

Mode 0 (13-bit)

Mode 0 operation is the same for Timer 0 and Timer 1. In Mode 0, the timer is configured as a 13-bit counter that uses bits 0-4 of TL0 (or TL 1) and all 8 bits of TH0 (or TH1). The timer enable bit (TR0/TR1) in the TCON SFR (table 37) starts the timer. The C/T bit selects the Timer/Counter clock source, CLK or T0IN/T1IN.

When the 13-bit count increments from 1FFFh (all ones), the counter rolls over to all zeros, the TF0 (or TF1) bit is set in the TCON SFR, and the T0OUT (or T1OUT) pin goes high for one clock cycle.

The upper 3 bits of TL0 (or TL1) are indeterminate in Mode 0 and must be masked when the software evaluates the register.

FIGURE 10: TIMER 0 MODE 0

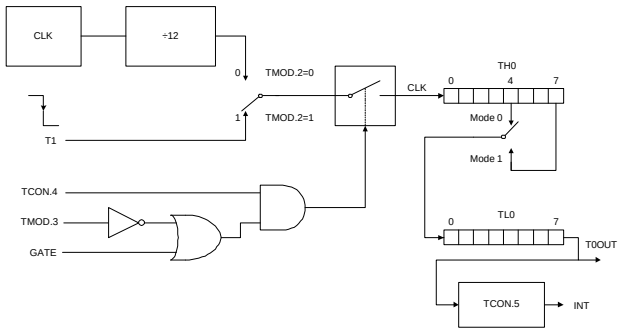
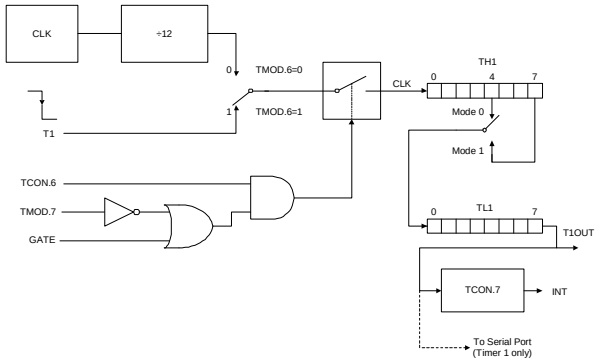


FIGURE 11: TIMER 1 MODE 0



Mode1 (16-bit)

Mode 1 operation is the same for Timer 0 and Timer 1. In Mode 1, the timer is configured as a 16-bit counter. The counter rolls over to all zeros (0000h) upon surpassing FFFFh. Otherwise, Mode 1 operation is the same as Mode 0.

FIGURE 12: TIMER 0 MODE 1

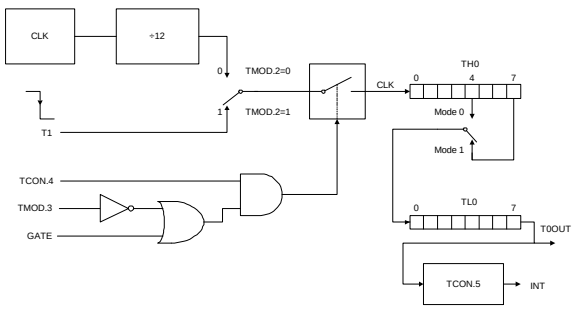


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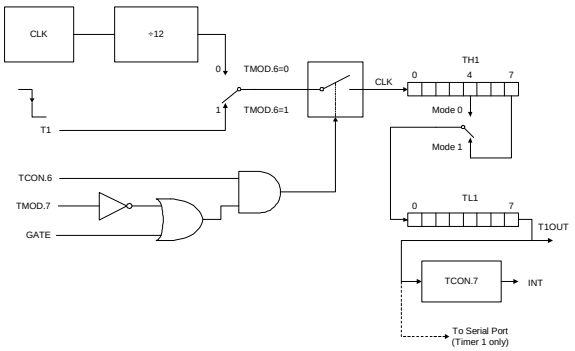
FIGURE 13: TIMER 1 MODE 1



Mode 2 (8-bit)

The operation of Mode 2 is the same for Timer 0 and Timer 1. In Mode 2, the timer is configured as an 8-bit counter, with automatic reload of the start value. The LSB register (TL0 or TL1) is the counter and the MSB register (TH0 or TH1) stores the reload value.

The Mode 2 counter control is the same as for Mode 0 and Mode 1. However, in Mode 2, when TLx surpasses FFh, the value stored in THx is reloaded into TLx.

FIGURE 14: TIMER 0 MODE 2

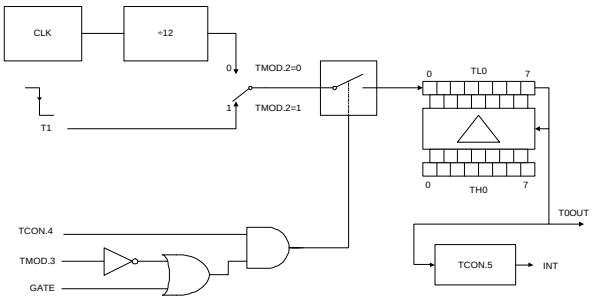
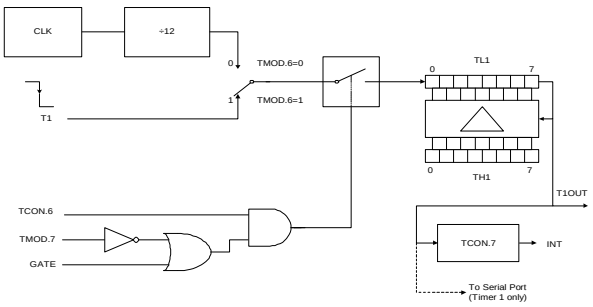


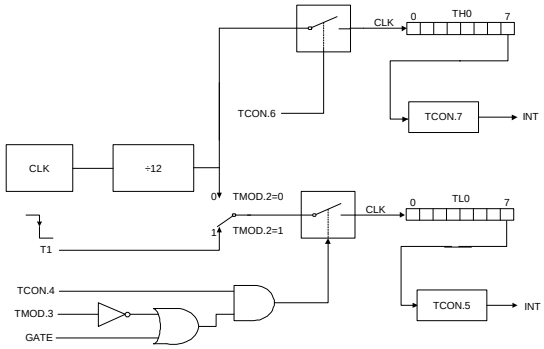
FIGURE 15: TIMER 1 MODE 2



Mode 3 (2 x 8-bit)

In Mode 3, Timer 0 operates as two 8-bit counters and Timer 1 stops counting and holds its value.

FIGURE 16: TIMER MODE 3



Timer 2

The VERSA MIX Timer 2 offers the three following general functionalities:

- 16-Bit Timer
- 16-Bit Auto-Reload Timer
- 16 Bit Precision Baud Rate Generator

Dividing the Clock Frequency

In the timer modes, the clocking of Timer 2 can only be accomplished using distinct clock division values. These values are $f_{clk}/2$, $f_{clk}/12$ and $f_{clk}/24$. The purpose of these distinct values becomes evident when performing Pulse Width Modulation.

In order to select the desired clocking frequency, one must adjust the values of the T2PS (Timer 2 prescaler) and T2PSM (Timer 2 master prescaler) bits of the T2CON register as shown in Table 39 (T2CON). See figure 17 (Timer 2 block diagram) for a schematic representation of this frequency division process.

Pulse Width Modulation (PWM)

Pulse Width Modulation is the process of adjusting the width of the logical high part of a square wave. In other words, when we carry out PWM, we adjust the duty cycle of a square wave. By adjusting this duty cycle, we are able to perform a digital to analog conversion by placing the modulated signal at the input of a low pass filter. The greater the duty cycle of the square wave, the greater the DC value is at the output of the low pass filter and vice versa. Below is a table that summarizes the relationship between the duty cycle and the output that it will generate on the VERSA MIX. (Note that the values are given with respect to the sinusoidal ripple that occurs at the output of the filter)

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TABLE 40: PULSE WIDTH MODULATION

	RIPPLE			
Duty Cycle	**Max V (V)**	**Min V (V)**	**Delta V (V)**	Stable (ms) ~
1% (T=0.16us)	81.887m	80.616	1.271m	4.5
10% (T= 1.6us)	817.538m	807.413	10.125m	5.8806
25% (T= 4us)	1.288	1.273	15.142m	5.7982
50% (T=8us)	2.5412	2.5213	19.841m	7.5483
75% (T=12us)	3.7883	3.7736	14.645m	6.6
100% (T=16us)	5	5	0	4.988

One may ask how exactly Timer 2 ties into this digital to analog conversion process. Firstly, it is important to know that Timer 2 may act as a counter that is incremented at every signal pulse of the appropriate source. This source is selected by the T211 and T210 bits of T2CON. When a digital value is written into one of the CCxx registers, a comparison occurs (providing that Timer 2 is in compare mode of course). As long as the value of the CCxx register is greater than the Timer 2 value, the compare unit will output a logical high. At the instant where the two signals are equal, the compare unit will change from a logical high to a logical low. Thus, inputting various digital values into a CCxx register will yield waveforms that vary in width. As explained above, a variation in width allows us to generate various DC values, which is equivalent to performing a digital to analog conversion.

Selecting the Data Line Width

The VERSA MIX is capable of comparing and capturing data using data lines up to 16 bits wide. When comparing 2 registers or capturing 1 register, it is encouraged to set the T2S bit of the T2CON register to 1. This adjusts the lines to have an 8-bit width.

On the other hand, when comparing 2 pairs of registers, for example CCH1 and CCL1 to TH2 and TL2, the T2S bit must be set to 0. This will make the data lines 16 bits wide.

TABLE 41: (T2CON) TIMER 2 CONTROL REGISTER -SFR C8H

7	6	5	4
T2PS	T2PSM	T2S	T2R1

3	2	1	0
T2R0	T2CM	T2I1	T2I0

Bit	Mnemonic	Function
7	T2PS	Prescaler select bit: 0 = Timer 2 is clocked with 1/12 of the oscillatory frequency 1 = Timer 2 is clocked with 1/24 of the oscillatory frequency
6	T2PSM	0 = Prescaler 1 = clock/2
5	T2S	0 = 16-bit 1 = 8-bit
4	T2R1	Timer 2 reload mode selection 0X = Reload disabled 10 = Mode 0 11 = Mode 1
3	T2R0	Timer 2 reload mode selection 0X = Reload disabled 10 = Mode 0 11 = Mode 1
2	T2CM	Timer 2 compare mode selection 0 = Mode 0 1 = Mode 1
1	T211	Timer 2 input selection 00 = Timer 2 stops 01 = Input frequency f/12 or f/24 10 = Timer 2 is incremented by external signal at pin T2 (P1.7) 11 = Internal clock input is gated to the Timer 2.
0	T210	Timer 2 input selection 00 = Timer 2 stops 01 = Input frequency f/2, f/12 or f/24 10 = Timer 2 is incremented by external signal at pin T2 (P1.7) 11 = Internal clock input is gated to the Timer 2.

Compare, Capture and Reload Registers

The following tables represent the different registers that may capture or that may be compared to the value of Timer 2 (there are 8 in total). Please note that the CRCx registers are the only ones that can be used to perform a reload operation.

TABLE 42: (CCL1) COMPARE/CAPTURE REGISTER 1, LOW BYTE - SFR C2H

7	6	5	4	3	2	1	0
CCL1 [7:0]							

TABLE 43: (CCH1) COMPARE/CAPTURE REGISTER 1, HIGH BYTE - SFR C3H

7	6	5	4	3	2	1	0
CCH1 [7:0]							

TABLE 44: (CCL2) COMPARE/CAPTURE REGISTER 2, LOW BYTE - SFR C4H

7	6	5	4	3	2	1	0
CCL2 [7:0]							

TABLE 45: (CCH2) COMPARE/CAPTURE REGISTER 2, HIGH BYTE - SFR C5H

7	6	5	4	3	2	1	0
CCH2 [7:0]							

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TABLE 46: (CCL3) COMPARE/CAPTURE REGISTER 3, LOW BYTE - SFR C6H

7	6	5	4	3	2	1	0
CCL3 [7:0]							

TABLE 47: (CCH3) COMPARE/CAPTURE REGISTER 3, HIGH BYTE - SFR C7H

7	6	5	4	3	2	1	0
CCH3 [7:0]							

TABLE 48: (CRCL) COMPARE/RELOAD/CAPTURE REGISTER, LOW BYTE - SFR CAH

7	6	5	4	3	2	1	0
CRCL [7:0]							

TABLE 49: (CRCH) COMPARE/RELOAD/CAPTURE REGISTER, HIGH BYTE - SFR CBH

7	6	5	4	3	2	1	0
CRCH [7:0]							

TABLE 50: (TL2) TIMER 2, LOW BYTE - SFR CCH

7	6	5	4	3	2	1	0
TL2 [7:0]							

TABLE 51: (TH2) TIMER 2, HIGH BYTE - SFR CDH

7	6	5	4	3	2	1	0
TH2 [7:0]							

Overflows and Interrupts

When the Timer 2 counter overflows from FFFFh, the TF2 flag is set. This occurrence raises a Timer 2 interrupt (if enabled). From Figure 19 (TIMER 2 Block diagram), notice that an interrupt may also be generated from T2EX if EXEN2 is enabled. An interrupt of this sort may be verified by checking the value of the EXF2 bit of the (IEN1) Interrupt Enable 1 Register-SFR E8h.

The compare and capture function on the VERSA MIX has a wide variety of different operating states. These states are controlled by the COCALX and COCAHX registers. The different states are: compare and capture mode enable/disable; capture on falling edge at CC0 enable; and compare enabled. The detailed signal combinations are summarized in the following table.

TABLE 52: (CCEN) COMPARE/CAPTURE ENABLE REGISTER -SFR C9H

7	6	5	4
COCAH3	COCAL3	COCAH2	COCAL2

3	2	1	0
COCAH1	COCAL1	COCAH0	COCAL0

Bit		
Mnemonic	Mnemonic	Function
COCAH0	**COCAL0**	Compare and capture mode for CRC register
0	0	Compare/capture disabled
0	1	Capture on falling edge at pin CC0 (1 cycle)
1	0	Compare enabled
1	1	Capture on write operation into register CRC1
COCAH1	**COCAL1**	Compare/capture mode for CC register 1
0	0	Compare/capture disabled
0	1	Capture on rising edge at pin CC1 (2 cycles)
1	0	Compare enabled
1	1	Capture on write operation into register CCL1
COCAH2	**COCAL2**	Compare/capture mode for CC register 2
0	0	Compare/Capture disabled
0	1	Capture on rising edge at pin CC2 (2 cycles)
1	0	Compare enabled
1	1	Capture on write operation into register CCL2
COCAH3	**COCAL3**	Compare/Capture mode for CC register 3
0	0	Compare/capture disabled
0	1	Capture on rising edge (2 cycles)
1	0	Compare enabled
1	1	Capture on write operation into register CCL3

Timer 2 16-bit Timer Modes

Event Counter Mode

When operating in the Event Counter Mode, the timer is incremented as soon as the external signal T2IN changes value from 1 to 0. A sample of the T2IN input is taken at every machine cycle. Timer 2 is incremented in the cycle following the one in which the transition was detected.

Gated Timer Mode

When operating in the Gated Timer Mode, the internal clock, which incremented timer 2, is gated by the external signal T2IN. In other words, when T2IN is high, the internal clock is allowed to pass through the AND gate. A low value of T2IN will stop the clock pulse, which allows for easier pulse width measurements.

The functionality and register interactions of the Timer 2 and the Compare, Capture and Reload Modes are depicted in figure 17.

Notice from the figure that the input selection of Timer 2 has 4 possible sources determined by 2 bits in the T2CON

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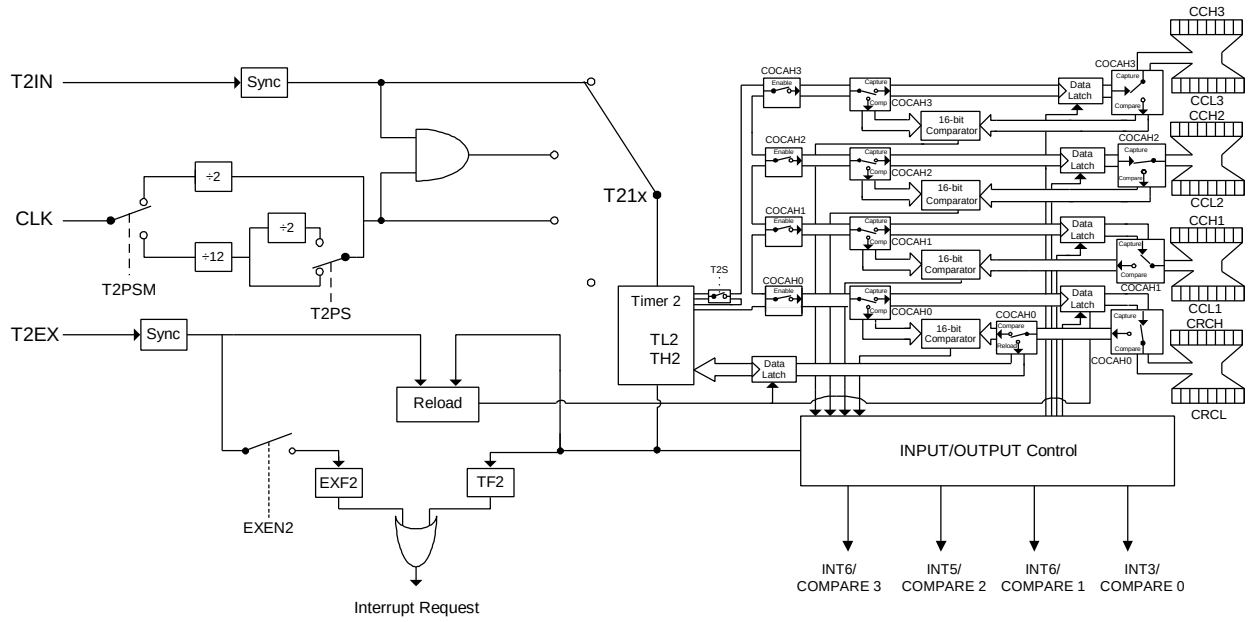
register. These select bits are named T211 and T210. The purpose of these bits is to select whether Timer 2 stops, takes its input from the f/12 or f/24 line, if it is incremented by an external signal at pin T2IN or if the internal clock input is gated to Timer 2 (as shown in Figure 17).

FIGURE 17: TIMER 2 AND COMPARE/CAPTURE UNIT



One may further delve into the functionality of this unit by analyzing the specifics of each mode. These specifics are explained in the following paragraphs.

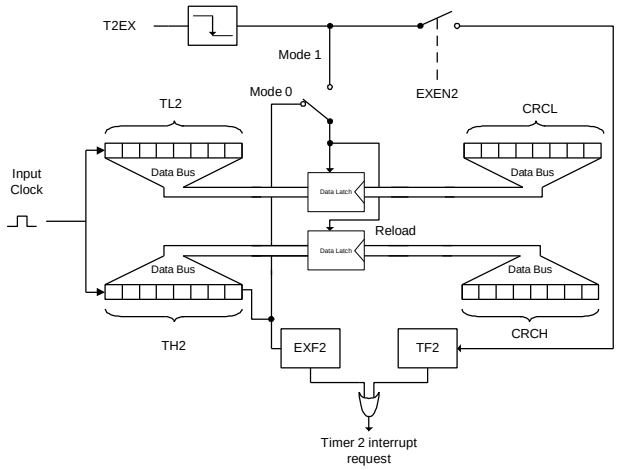
Reload Modes

Figure 18 (Timer 2 Reload mode) shows what happens during a reload operation. From the schematic, we see that CRCx constantly reloads TL2 and/or TH2 at each clock pulse. The reload mode is selected by the T2R1 and T2R0 bits of the T2CON register.

In Mode 0, when the timer overflows and all 1's become 0's, the TF2 overflow flag is set. Concurrently, this overflow causes the Timer 2 registers to be loaded with the 16-bit value contained in the CRC register (which has been preset by software). This reload operation will occur during the same clock cycle in which TF2 was set, thus overwriting the present count value 0000h.

In Mode 1, a 16-bit reload from the CRCx register on the falling edge of T2EX occurs. This transition will set EXF2 if EXEN2 is set. This action will cause an interrupt (providing that the Timer 2 interrupt is enabled).

FIGURE 18: TIMER 2 RELOAD MODE



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Compare Modes

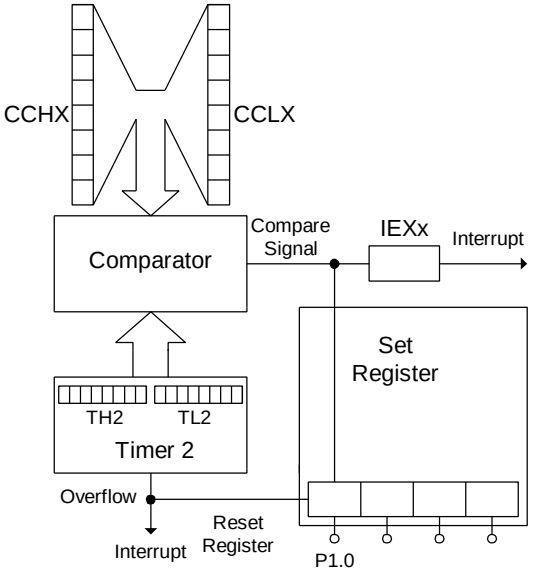
When Timer 2 is in compare mode, a Timer 2 count value is compared to a value that is stored in the CCxx or CRCx registers. If the values compared match (i.e. when the pulse changes state), an interrupt is generated at the appropriate port pin. Varying the value of the CCxx or CRCx allows a variation of the rectangular pulse generated at the output. This variation can be used to perform pulse width modulation.

In order to select the compare mode, we must adjust the value of bit T2CM in the T2CON register. In both modes the new value arrives at port pin 1 in the same clock cycle during which the internal compare signal is activated.

Compare Mode 0

The functional diagram of this mode can be found below in Figure 19. From this schematic, we notice that upon comparison of the 16-bit values of the CCxx and Txx (Timer 2 registers), a high compare signal is generated. The compare signal is then propagated to IEXx (which will generate an interrupt) and to the pin P1.0. Pin P1.0 is reset when a Timer 2 overflow occurs. It is important to note that when compare mode is enabled, the corresponding output pin can only be reset by the internal timer circuitry.

FIGURE 19: TIMER 2 COMPARE MODE 0 BLOCK DIAGRAM



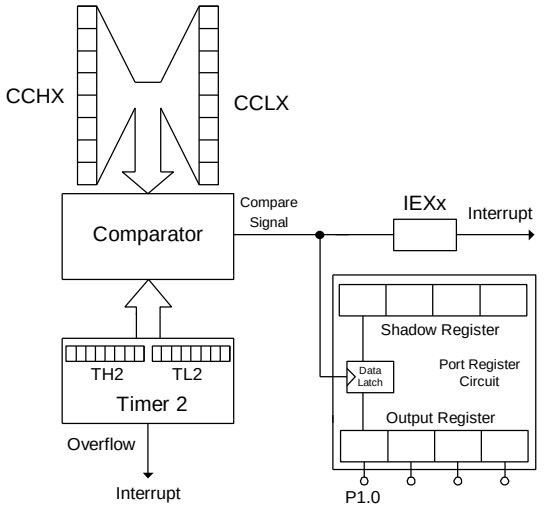
Compare Mode 1

This mode should be used when output signals are not related to a constant signal period.

If the unit is operating in Mode 1, and the software writes to the corresponding output register at the port, the new value will not appear at the output until the next compare match occurs.

One may, therefore, decide whether the output signal is to make a new transition, or if it is to keep the old value that Timer 2 contained when it last matched the values in the CCxx or CRCx registers.

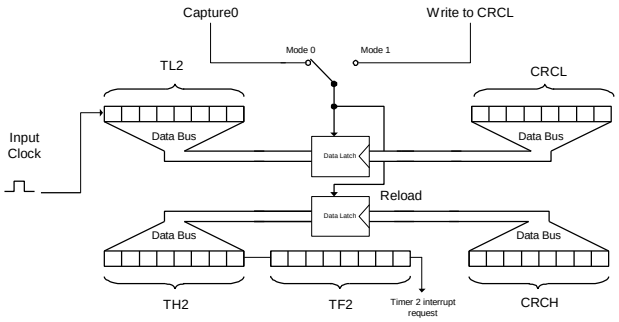
FIGURE 20: TIMER 2 COMPARE MODE 1 BLOCK DIAGRAM



Capture Modes

In capture mode, the CCxx or CRCx latches the data placed on the data lines by Timer 2. In Mode 0, an external event triggers the latching of Timer 2's data by one of the compare and capture registers. In Mode 1, a capture will occur upon writing to the Low Byte of the chosen capture register. This mode allows the software to continuously read the contents of Timer 2. Table 52 (on page 24) contains the information concerning the clock edges on which the capture occurs.

FIGURE 21: TIMER 2 CAPTURE MODE 0 FOR CRCL AND CRCH BLOCK DIAGRAM



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Serial Interface

The VERSA MIX provides two asynchronous UART interfaces: UART 0 and UART 1. Please note that Serial and UART will be used interchangeably throughout this document.

Each serial port has a 10-bit timer devoted to baud rate generation.

Serial Port Data Buffers

Both serial ports operate in full duplex asynchronous mode. The VERSA MIX buffers receive data in a holding register, enabling the UART to accept an incoming word before the software has read the previous value.

The buffers consist of two separate registers. The S1BUF register and the S0BUF register.

TABLE 53: (S1BUF) SERIAL PORT 1, DATA BUFFER - SFR C1H

7	6	5	4	3	2	1	0
S1BUF [7:0]							

TABLE 54: (S0BUF) SERIAL PORT 0, DATA BUFFER - SFR 99H

7	6	5	4	3	2	1	0
S0BUF [7:0]							

Serial 0: Modes of Operation

The VERSA MIX's serial interfaces are capable of operating in various modes.

Below is a tabulated summary of the modes of operation of UART0.

TABLE 55: SERIAL PORT 0 MODES

SM0	SM1	MODE	DESCRIPTION	BAUD RATE
0	0	0	Shift Register	Fosc/12
0	1	1	8-bit UART	Variable
1	0	2	9-bit UART	Fclk/32 or /64
1	1	3	9-bit UART	Variable

**Note that the speed in mode 2 depends on SMOD bit in the Special Function Register PCON when SMOD = 1 fclk/32

In order to achieve these operating states, the user must set certain bits in the register represented below (table 56). Serial Port 0 contains other control bits that are also explained in detail in table 56.

TABLE 56: (S0CON) SERIAL PORT 0, CONTROL REGISTER - SFR 98H

7	6	5	4
SM0	SM1	SM20	REN0

3	2	1	0
TB80	RB80	TI0	RI0

Bit	Mnemonic	Function
7	SM0	Sets baud rate
6	SM1	Sets baud rate
5	SM20	Enables the multiprocessor communication feature.
4	REN0	1 = Enables serial reception. Cleared by software to disable reception.
3	TB80	The 9th transmitted data bit in Modes 2 and 3. Set or cleared by the CPU, depending on the function it performs (parity check, multiprocessor communication etc.).
2	RB80	In Modes 2 and 3, it is the 9th data bit received. In Mode 1, if sm20 is 0, RB80 is the stop bit. In Mode 0, this bit is not used. Must be cleared by software.
1	TI0	Transmit interrupt flag set by hardware after completion of a serial reception. Must be cleared by software.
0	RI0	Receive interrupt flag set by hardware after completion of a serial reception. Must be cleared by software.

With the appropriate select bits in mind, let us now examine the 4 operating modes of Serial 0 in detail.

Mode 0

In this mode, pin RX0 is used as an input and an output, while TX0 is used only to output the shift clock. For an operation in this mode, 8 bits are transmitted with the LSB as the first bit. In addition, the baud rate is fixed at 1/12 of the crystal oscillator frequency. In order to initialize reception in this mode, the user must set the bits RI0 and REN0 in the S0CON register to 0 and 1 respectively. Note that in other modes, when REN0=1, the interface begins to receive data.

Mode 1

In this mode, pin RX0 serves uniquely as an input and TX0 serves as a serial output. In this case, no external shift clock is used. For an operation in this mode, 10 bits are transmitted: a logical low start bit; 8 bits of data starting with the LSB; and a logical high stop bit (always). During a reception, the start bit synchronizes the transmission and 8 bits of data are available by reading S0BUF. The reception is completed once the stop bit sets the RB80 flag in the S0CON register. The baud rate may be specified by the internal baud rate generator or by Timer 1.

Mode 2

In this mode, pin RX0 is used as an input and as an output while TX0 is used only to output the shift clock. For an operation in this mode, 11 bits are transmitted or received. These 11 bits are composed of a logical low start bit, 8 bits of data (LSB first), a programmable 9th bit, and a logical high stop bit. The purpose of this 9th bit is used to control the

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parity of the serial interface. For a data transmission, bit TB80 of the S0CON is outputted as the 9th bit. For a reception, the 9th bit will be stored into the RB80 bit of the S0CON register.

Mode 3

Mode 3 is essentially identical to Mode 2. However, in Mode 3, the user may use the internal baud rate generator or timer 1 to set the baud rate.

Serial 1: Modes of Operation

Serial 1 can operate in two modes. The S1CON register controls this serial port. The following section explains the operation of Serial 1.

Below is a summarized mode table for Serial Port 1.

TABLE 57: SERIAL PORT 1 MODES

SM	MODE	DESCRIPTION	BAUD RATE
0	A	9-bit UART	Variable
1	B	8-bit UART	Variable

Table 58 explains the bit functions of the Serial Port 1 control register.

TABLE 58: (S1CON) SERIAL PORT 1, CONTROL REGISTER - SFR C0H

7	6	5	4
SM	-	SM21	REN1

3	2	1	0
TB81	RB81	TI1	RI1

Bit	Mnemonic	Function
7	SM	Is used to set baud rate
6	-	-
5	SM21	1 = Enables multiprocessor communication feature.
4	REN1	If set, enables serial reception. Cleared by software to disable reception.
3	TB81	The 9th transmitted data bit in mode A. Set or cleared by the CPU, depending on the function it performs (parity check, multiprocessor communication, etc.)
2	RB81	In Mode A, it is the 9th data bit received. In Mode B, if SM21 is 0, RB81 is the stop bit. Must be cleared by software.
1	TI1	Transmit interrupt flag, set by hardware after completion of a serial transfer. Must be cleared by software
0	RI1	Receive interrupt flag, set by hardware after completion of a serial reception. Must be cleared by software

Mode A

In this mode, 11 bits are transmitted or received. These 11 bits are composed of a logical low start bit, 8 bits of data (LSB first), a programmable 9th bit and a logical high stop bit. As in Mode 2 and 3 of Serial 1, this 9th bit is used to control the parity of the serial interface. For a data transmission, bit TB81 of the S1CON is outputted as the 9th bit. For a reception, the 9th bit will be stored into the RB81 bit of the S1CON register. Note that in this mode, the only way to specify the baud rate is by using the internal baud rate generator.

Mode B

In this mode, pin RX1 serves uniquely as an input and TX01 serves as a serial output. In this case, no external shift clock is used. For an operation in this mode, 10 bits are transmitted: a logical low start bit; 8 bits of data starting with the LSB; and a logical high stop bit (always). During a reception, the start bit synchronizes the transmission and 8 bits of data are available by reading S1BUF. The reception is completed once the stop bit sets the RB81 flag in the S1CON register. The baud rate is specified by the internal baud rate generator.

Baud Rate Generator (Serial 0 and 1)

The tables below (excluding WDCON) are those in which we must store specific values to obtain a desired baud rate. The TH1 Register (Table 36 of the Timer 1 section), controls the baud rate of Serial 0 when WDCON.7 = 0, whereas the S0REL registers are used to set the baud rate of Serial 0 when WDCON.7 = 1.

TABLE 59: (WDCON) POWER FAIL CONTROL REGISTER - SFR D8H

7	6	5	4	3	2	1	0
WDCON.7	-	-	-	-	-	-	-

7	WDCON.7	Controls the baud rate generator mode: 0 = (Standard mode) 1 = (Fast Mode)
6:0	-	-

On the other hand, the S1REL registers are used when one needs to adjust the baud rate on Serial 1.

TABLE 60: (S0RELL) SERIAL PORT 0, RELOAD REGISTER, LOW BYTE - SFR 96H

7	6	5	4	3	2	1	0
S0RELL [7:0]							

TABLE 61: (S0RELH) SERIAL PORT 0, RELOAD REGISTER, HIGH BYTE - SFR 97H

7	6	5	4	3	2	1	0
S0RELH [15:8]							

TABLE 62: (S1RELL) SERIAL PORT 1, RELOAD REGISTER, LOW BYTE - SFR BEH

7	6	5	4	3	2	1	0
S1RELL [7:0]							

TABLE 63: (S1RELH) SERIAL PORT 1, RELOAD REGISTER, HIGH BYTE - SFR BFH

7	6	5	4	3	2	1	0
S1RELH [7:0]							

In order to calculate the baud rate or reload value for Timer 1, one must evaluate the following equation. Please note that one may avoid having to apply these formulas by plugging the required values into the VERSA MIX SERIAL

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INTERFACE BAUD RATE CALCULATOR on the Goal Semiconductor website at www.goalsemi.com. The calculator will display the correct TH1, S0REL, and S1REL HEX and decimal values. Instructions on how to use this simple and user-friendly program are found in the VERSA MIX application notes.

TABLE 64: EQUATION TO CALCULATE BAUD RATE FOR SERIAL 0

Serial 0: mode 1 and 3
Mode 1: For WDCON.7=0 (standard mode)
$\text{Baud Rate} = \frac{2^{SMOD} \times f_{clk}}{32 \times 12 \times (256-TH1)}$
$TH1 = 256 - \frac{2^{SMOD} \times f_{clk}}{32x12x \text{ Baud Rate}}$
Mode 3: For WDCON.7=1 (fast mode)
$\text{Baud Rate} = \frac{2^{SMOD} \times f_{clk}}{64 \times (1024 - \text{S0REL})}$
$\text{SOREL} = 1024 - \frac{2^{SMOD} \times f_{clk}}{64 \times \text{Baud Rate}}$

TABLE 65: SERIAL 0 BAUD RATE SAMPLE VALUES WDCON.7 =0, SMOD = 1

Desired Baud Rate	TH1 @ f_{clk}= 11.0592 MHz	TH1 @ f_{clk}= 14.746 MHz	TH1 @ f_{clk}= 16.000 MHz
115.2 kbps	N/A	N/A	N/A
57.6 kbps	FFh	N/A	N/A
19.2 kbps	FDh	FCh	N/A
9.6 kbps	FAh	F8h	N/A
2.4 kbps	E8h	E0h	DDh
1.2 kbps	D0h	C0h	BBh
300 bps	40h	N/A	N/A

TABLE 66: SERIAL 0 BAUD RATE SAMPLE VALUES WDCON.7 =0, SMOD = 0

Desired Baud Rate	TH1 @ f_{clk}= 11.0592 MHz	TH1 @ f_{clk}= 14.746 MHz	TH1 @ f_{clk}= 16.000 MHz
115.2 kbps	N/A	N/A	N/A
57.6 kbps	N/A	N/A	N/A
19.2 kbps	N/A	FEh	N/A
9.6 kbps	FDh	FCh	N/A
2.4 kbps	F4h	F0h	N/A
1.2 kbps	E8h	E0h	DDh
300 bps	A0h	80h	75h

TABLE 67: SERIAL 0 BAUD RATE SAMPLE VALUES WDCON.7 = 1, SMOD = 1

Desired Baud Rate	S0REL @ f_{clk}= 11.0592 MHz	S0REL @ f_{clk}= 14.746 MHz	S0REL @ f_{clk}= 16.000 MHz
115.2 kbps	3FDh	3FCh	N/A
57.6 kbps	3FAh	3F8h	N/A
19.2 kbps	3EEh	3E8h	3E6h
9.6 kbps	3DCh	3D0h	3CCh
2.4 kbps	370h	340h	330h
1.2 kbps	2E0h	280h	25Fh
300 bps	N/A	N/A	N/A

TABLE 68: SERIAL 0 BAUD RATE SAMPLE VALUES WDCON.7 =1, SMOD = 0

Desired Baud Rate	S0REL @ f_{clk}= 11.0592 MHz	S0REL @ f_{clk}= 14.746 MHz	S0REL @ f_{clk}= 16.000 MHz
115.2 kbps	N/A	3FEh	N/A
57.6 kbps	3FDh	3FCh	N/A
19.2 kbps	3F7h	3F4h	3F3h
9.6 kbps	3EEh	3E8h	3E6h
2.4 kbps	3B8h	3A0h	398h
1.2 kbps	370h	340h	330
300 bps	1C0h	100	0BFh

In order to calculate the Baud Rate of Serial 1, one must perform the following operation or use the VERSA MIX SERIAL INTERFACE BAUD RATE CALCULATOR.

Serial 1
$\text{Baud Rate} = \frac{f_{clk}}{32 \times (2^{10}-\text{S1REL})}$
Note: S1REL.9-0 = S1RELH.1-0 + S1RELL.7-0
$\text{S1REL} = 1024 - \frac{f_{clk}}{32 \times \text{Baud Rate}}$

TABLE 69: SERIAL 1 BAUD RATE SAMPLE VALUES

Desired Baud Rate	S1REL @ f_{clk}= 11.0592 MHz	S1REL @ f_{clk}= 14.746 MHz	S1REL @ f_{clk}= 16.000 MHz
115.2 kbps	3FDh	3FCh	N/A
57.6 kbps	3FAh	3F8h	N/A
19.2 kbps	3EEh	3E8h	3E6h
9.6 kbps	3DCh	3D0h	3CCh
2.4 kbps	370h	34Fh	330h
1.2 kbps	2E0h	280h	25Fh
300 bps	N/A	N/A	N/A

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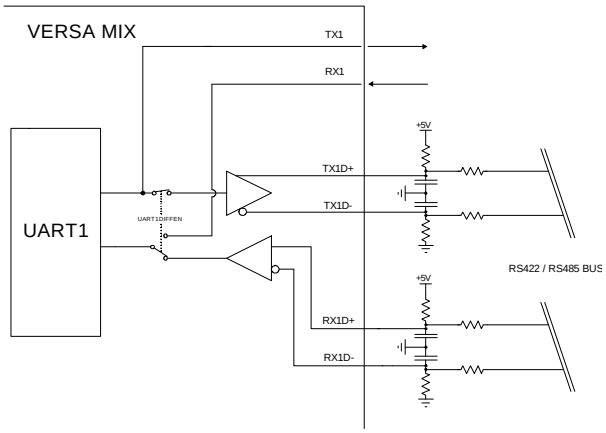
RS-485/RS-422 Interface

The VERSA MIX includes an RS-485/RS-422 Transceiver that can be internally connected to UART1.

FIGURE 22: RS-485/RS-422 INTERFACE



This interface may be enabled by setting bit 2 (UART1DIFFEN) of the digital peripheral power enable register to 1 (see Table 32).

- Permits interface with RS-485/RS-422 devices
- Differential interface provides great noise immunity
- Common mode voltage range: -2.5V to 7.5V
- Interfaced through UART1
- Communication protocol control is given to the user

SPI Interface

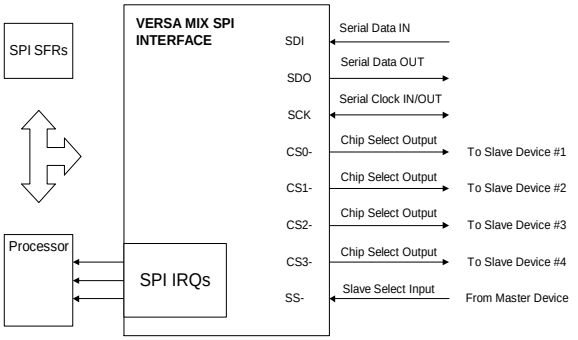
The VERSA MIX SPI interface can operate as either a master or a slave device. In master mode, an additional 4 chip enable signals can be used to allow 4 slave devices to share the SPI bus.

The SPI interface is fully configurable. The following parameters of the SPI interface can be configured:

- Permits synchronous serial data transfers
- Transactions are configurable from 1-32 bits+
- Full duplex support
- SPI Modes 0, 1, 2, 3, and 4 supported (clock polarity/phase control)
- Up to four slave devices can be connected to the SPI interface when configured in master mode
- The SPI interface can be used in slave mode
- Data transmission speed is configurable
- Double buffers in transmission and reception
- 3 dedicated interrupt flags
- TX-Empty
- RX Data Available
- RX Overrun
- Automatic/Manual control of the chip select (no wasted I/O)
- SPI operation is not affected by the clock control unit

The figure below represents the SPI Interface in block diagram format.

FIGURE 23: SPI INTERFACE BLOCK DIAGRAM



The registers below serve as a 32-bit buffer to regulate the data being received by and transmitted from the SPI interface.

TABLE 70: (SPIRXTX0) SPI DATA BUFFER, LOW BYTE - SFR E1H

7	6	5	4	3	2	1	0
SPIRXTX0 [7:0]							

Bit	Mnemonic	Function
7-0	SPIRXTX0	SPI Receive / Transmit Data Bits 7:0

TABLE 71: (SPIRXTX1) SPI DATA BUFFER, BYTE 1 - SFR E2H

7	6	5	4	3	2	1	0
SPIRXTX1 [15:8]							

Bit	Mnemonic	Function
15:8	SPIRXTX1	SPI Receive / Transmit Data Bits 15:8

TABLE 72: (SPIRXTX2) SPI DATA BUFFER, BYTE 2 - SFR E3H

7	6	5	4	3	2	1	0
SPIRXTX2 [23:16]							

Bit	Mnemonic	Function
22:16	SPIRXTX2	SPI Receive / Transmit Data Bits 22:16

TABLE 73: (SPIRXTX3) SPI DATA BUFFER, HIGH BYTE - SFR E4H

7	6	5	4	3	2	1	0
SPIRXTX3 [31:24]							

Bit	Mnemonic	Function
31:24	SPIRXTX3	SPI Receive / Transmit Data Bits 31:24

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The following register summarizes the possible clock frequencies of the SPI interface.

TABLE 74: (SPICTRL1) SPI CONTROL REGISTER 1 - SFR E5H

7	6	5	4
SPICK [2:0]			SPICS_1

3	2	1	0
SPICS_0	SPICKPH	SPICKPOL	SPIMA_SL

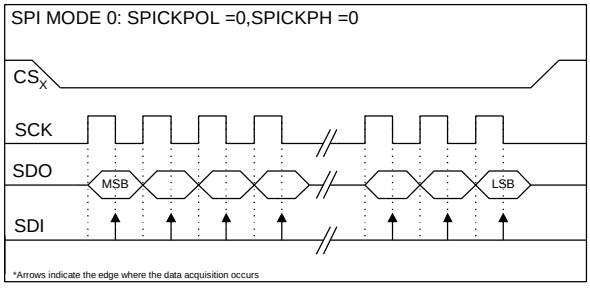
Bit	Mnemonic	Function
7:5	SPICK	SPI Clock control 000 = OSC Ck Div 2 001 = OSC Ck Div 4 010 = OSC Ck Div 8 011 = OSC Ck Div 16 100 = OSC Ck Div 32 101 = OSC Ck Div 64 110 = unused
4:3	SPICS	Active CS line in Master Mode 00 = CS0- Active 01 = CS1- Active 10 = CS2- Active 11 = CS3- Active
2	SPICKPH	SPI Clock Phase
1	SPICKPOL	SPI Clock Polarity 0 – CK Polarity is Low 1 – CK Polarity is High
0	SPIMA_SL	Master / -Slave 0 = Master 1 = Slave

The figures below show how the SPI Clock Polarity and Phase affect the reading and writing operations of the SPI interface. Notice that when the chip select bit (CSx) goes to 0, the SCK clock begins to operate. The difference in the operating modes lies in the SDO and SDI parameters.

In Figure 24 (Mode 0):

- Data is placed on the lines (SDO) at every rising edge of the clock.
-
- Data is latched at every falling edge of the clock.

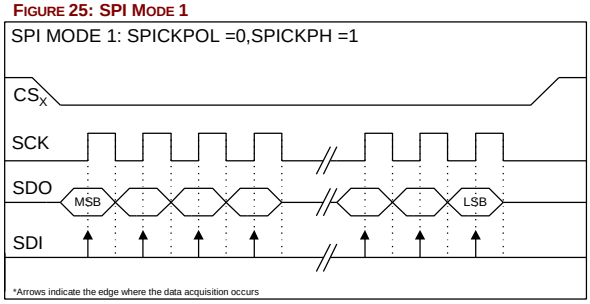
FIGURE 24: SPI MODE 0



In Figure 25 (Mode 1):

- Data is placed on the lines (SDO) at every falling edge of the clock.
- Data is latched at every rising edge of the clock.

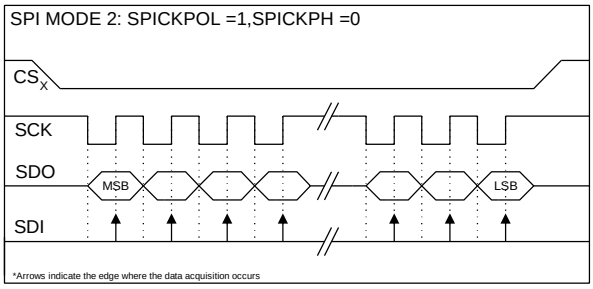
FIGURE 25: SPI MODE 1



In Figure 26 (Mode 2):

- Data is placed on the lines (SDO) at every falling edge of the clock.
- Data is latched at every rising edge of the clock.

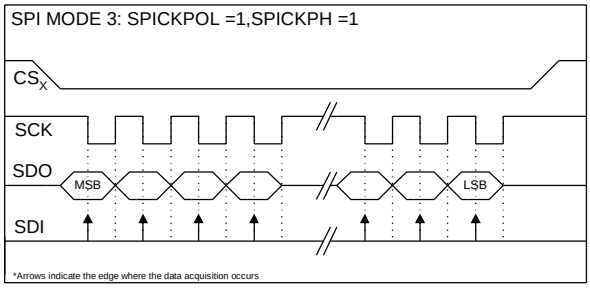
FIGURE 26: SPI MODE 2



In Figure 27 (Mode 3):

- Data is placed on the lines (SDO) at every rising edge of the clock.
- Data is latched at every falling edge of the clock.

FIGURE 27: SPI MODE 3



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The remaining SPI interface registers are listed in the following tables:

TABLE 75: (SPICTRL2) SPI CONTROL REGISTER 2 - SFR E6H

7	6	5	4
SPICSLO	SPICLRTXEMPTO	FSONICS3	SPIOPT

3	2	1	0
-	SPIRXOVIE	SPIRXAVIE	SPITXEMP

Bit	Mnemonic	Function
7	SPICSLO	Manual CS up (Master mode) 0 = The CSx goes low when transmission begins and returns to high when it ends. 1 = The CSx stays low after transmission ends. The user must clear this bit for the CSx line to return high.
6	SPICLRTXEMPTO	This bit only reads in a 0. Write → clr
5	FSONCS3	Optional Frame Select on CS3-
4	SPILOAD	Optional Load function on CS3-
3	-	-
2	SPIRXOVIE	SPI Receiver overrun interrupt enable.
1	SPIRXAVIE	SPI Receiver available interrupt enable.
0	SPITXEMPIE	SPI Transmitter empty interrupt enable.

TABLE 76: (SPISIZECTRL) SPI SIZE CONTROL REGISTER - SFR E7H

7	6	5	4	3	2	1	0
SPISIZE	-	-	-	-	-	-	-

Bit	Mnemonic	Function
7	SPISIZE	SPI transaction size = (SPI SIZE)

TABLE 77: (SPIIRQSTAT) SPI INTERRUPT STATUS REGISTER - SFR E9H

7	6	5	4
-	-	SPITXEMPTO	SPISLAVESEL

3	2	1	0
SPISEL	SPIOV	SPIRAXV	SPITXEMP

Bit	Mnemonic	Function
7:3	-	-
2	SPIOV	SPI Receiver overrun
1	SPIRXAV	SPI Receiver available
0	SPITXEMP	SPI Transmitter empty

I²C Interface

The VERSA MIX includes an I²C compatible interface that can be configured both in Master and Slave modes.

When PM = 0:

- Master/Slave configurable I²C interface
- Can be used to communicate with I²C devices or systems
- Many devices can share the I²C bus
- Adjustable communication speed (Up to 1MHz)
- Manual/Automatic acknowledge control when receiving data
- Tx Empty / Rx Data Available / Rx Overrun Flags

When PM = 1:

- The I²C interface serves to program the VERSA MIX Flash memory
- The I²C interface can serve to control the VERSA MIX peripherals
- The VERSA MIX processor is halted

TABLE 78: (I2CCONFIG) I2C CONFIGURATION - SFR DAH

7	6	5	4
I2CMASKID	I2CRXOVIE	I2CRXDAVIE	I2CTXEMPIE

3	2	1	0
I2CMANACK	I2CACKMODE	I2CMSTOP	I2CMASTER

Bit	Mnemonic	Function
5	I2CRXOVIE	I2C Receiver overrun interrupt enable
4	I2CRXDAVIE	I2C Receiver available interrupt enable
3	I2CTXEMPIE	I2C Transmitter empty interrupt enable
2	I2CMSTOP	I2C Master receiver stops when meeting acknowledged
1	-	-
0	I2CMASTER	I2C Master mode enable

TABLE 79: (I2CCHIPID) I2C CHIP ID - SFR DCH

7	6	5	4	3	2	1	0
I2CID [6:0]							I2CWID

Bit	Mnemonic	Function
7:1	I2CID	This Chip ID
0	I2WID	Wrong Chip ID

TABLE 80: (I2CCLKCTRL) I2C CLOCK CONTROL - SFR DBH

7	6	5	4	3	2	1	0
I2CCLKCTRL [7:0]							

Bit	Mnemonic	Function
7:0	I2CCLKCTRL	I2C Clock speed control

TABLE 81: (I2CIRQSTAT) I2C INTERRUPT STATUS - SFR DDH

7	6	5	4
I2CGOTSTOP	I2CNOACK	I2CSDASYNC	I2CDATACK

3	2	1	0
I2CIDLE	I2CRXOV	I2CRXAV	I2CTXEMP

Bit	Mnemonic	Function
7:3	-	-
2	I2CRXOV	I2C Receiver overrun
1	I2CRXAV	I2C Receiver available
0	I2CTXEMP	I2C Transmitter empty

TABLE82: (I2CRXTX) I2C DATA BUFFER - SFR DEH

7	6	5	4	3	2	1	0
I2CRXTX [7:0]							

Bit	Mnemonic	Function
7:0	I2CTX	I2C Data Receiver transmitter buffer

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General Purpose I/O

The VERSA MIX devices can be configured to provide up to 32 I/O pins. The I/Os are shared with the digital peripherals and can be configured individually.

Ports are bi-directional, each of them consist of a latch, an open drain driver with pull-up, and an input buffer. This means, the CPU can output or read data through any of these ports if they are not used for alternate purposes. The ports are represented in the table below:

TABLE 83: (P0) PORT 0 - SFR 80H

7	6	5	4	3	2	1	0
P0 [7:0]							

(P1) PORT 1 - SFR 90H

7	6	5	4	3	2	1	0
P1 [7:0]							

(P2) PORT 2 - SFR A0H

7	6	5	4	3	2	1	0
P2 [7:0]							

(P3) PORT 3 - SFR B0H

7	6	5	4	3	2	1	0
P3 [7:0]							

Bit	Mnemonic	Function
7-0	P01,2,3	When set to 1, the corresponding pin is at VCC. When set to 0, the corresponding pin is set to ground.

TABLE 84: (P0PINCFG) PORT 0 ALTERNATE FUNCTIONS CONFIGURATION REGISTER - SFR 9BH

7	6	5	4
UNUSED [7:4]			

3	2	1	0
RX1EN	TX1EN	T2EXEN	T2INEN

Bit	Mnemonic	Function
7	Not used	Reserved for future uses
6	Not used	Reserved for future uses
5	Not used	Reserved for future uses
4	Not used	Reserved for future uses
3	RX1EN	Alternate function enable UART1 Rx
2	TX1EN	Alternate function enable UART1 Tx
1	T2EXEN	Alternate function enable Timer 2 EX Input
0	T2INEN	Alternate function enable Timer 2 Input

TABLE 85: (P2PINCFG) PORT 2 ALTERNATE FUNCTION CONFIGURATION REGISTER - SFR 9DH

7	6	5	4
SDIEN	SDOEN	SCKEN	SSEN

3	2	1	0
CS0EN	CS1EN	CS2EN	CS3EN

Bit	Mnemonic	Function
7	SDIEN	Alternate function enable SPI SDI
6	SDOEN	Alternate function enable SPI SDO
5	SCKEN	Alternate function enable SPI SCK
4	SSEN	Alternate function enable SPI SS-
3	CS0EN	Alternate function enable SPI CS0-
2	CS1EN	Alternate function enable SPI CS1-
1	CS2EN	Alternate function enable SPI CS2-
0	CS3EN	Alternate function enable SPI CS3-

TABLE 86: (P3PINCFG) PORT 3 ALTERNATE FUNCTION CONFIGURATION REGISTER - SFR 9EH

7	6	5	4
MSCLEN	MSDAEN	T1INEN	CCU1EN

3	2	1	0
CCU0EN	T0INEN	RX0EN	TX0EN

Bit	Mnemonic	Function
7	MSCLEN	Alternate function enable Master I2C SCL
6	MSDAEN	Alternate function enable Master I2C SDA
5	T1INEN	Alternate function enable Timer1 Input
4	CCU1EN	Alternate function enable CCU1 Input
3	CCU0EN	Alternate function enable CCU0 Input
2	T0INEN	Alternate function enable Timer 0 Input
1	RX0EN	Alternate function enable UART0 Rx
0	TX0EN	Alternate function enable UART0 Tx

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Analog Signal Path

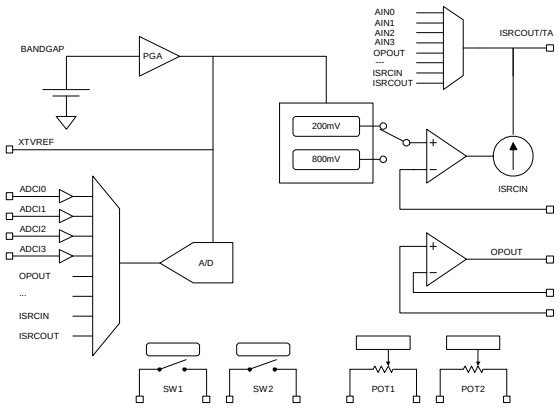
On the analog side, the VERSA MIX provides the following features:

- 4 External input channels for A/D converter
- Internal Band-Gap reference and PGA
- Programmable current source
- Input multiplexer
- Multiplexed analog output
- Digital potentiometers controlled by the µC
- Digital switches controlled by the µC

This permits the VERSA MIX to be used as a single chip acquisition system.

Figure 28 shows the analog block of the VERSA MIX. The choice of an on-chip calibrated bandgap or an external reference provides the basis for all derived on-chip voltages. These voltages are used as the reference signals for the ADC and the current source.

FIGURE 28: ANALOG SIGNAL PATH OF THE VERSA MIX



The control of the internal versus external reference, the multiplexer's current source drive, ADC and their respective power downs are all done via µ-Processor control through SFR registers.

TABLE 87: (INMUXCTRL) ANALOG INPUT MULTIPLEXER CONTROL REGISTER - SFR B5H

7	6	5	4	3	2	1	0
-	ADCINSEL [2:0]			AINEN [3:0]			

Bit	Mnemonic	Function
7	-	-
6:4	ADCINSEL	ADC Input Select 000 - AIN0 001 - AIN1 010 - AIN2 011 - AIN3 100 - OPAMP OUT 101 - VSR 110 - ISRCIN 111 - ISRCOUT
3:0	AINEN[3:0]	Analog Input Enable

The table below summarizes the analog output multiplexer select line combinations and their corresponding outputs.

TABLE 88: (OUTMUXCTRL) ANALOG OUTPUT MULTIPLEXER CONTROL REGISTER - SFR B6H

7	6	5	4	3	2	1	0
-	-	-	-	-	TAOUTSEL [2:0]		

Bit	Mnemonic	Function
7-3	Unused	Unused
2:0	TAOUTSEL	Signal output on TA 000 – AIN0 001 – AIN1 010 – AIN2 011 – AIN3 100 – VBGAP 101 – VSR 110 – unused 111 – unused

The analog peripherals such as the op amp, digital potentiometer, current source and analog to digital converter have one register dedicated to enabling and disabling them. This register and its bit functions are found below in Table 89.

TABLE 89: (ANALOGPWREN) ANALOG PERIPHERALS POWER ENABLE REGISTER - SFR 92H

7	6	5	4
OPAMPEN	DIGPOTEN	ISRCSEL	ISRCEN

3	2	1	0
TAEN	ADCEN	PGAEN	BGAPEN

Bit	Mnemonic	Function
7	OPAMPEN	1 = User Op-Amp Enable 0 = User Op-Amp Disable
6	DIGPOTEN	1 = Digital Potentiometer and Switch Enable 0 = Digital Potentiometer and Switch Disable
5	ISRCSEL	0 = ISRC 33uA 1 = ISRC 133uA
4	ISRCEN	1 = ISRC Output Enable 0 = ISRC Output Disable
3	TAEN	1 = TA Output Enable 0 = TA Output Disable
2	ADCEN	1 = ADC Enable 0 = ADC Disable
1	PGAEN	1 = PGA Enable 0 = PGA Disable
0	BGAPEN	1 = Bandgap Enable 0 = Bandgap Disable

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Internal Bandgap Reference and PGA

The VERSA MIX provides an internal temperature stable bandgap reference coupled with a programmable gain amplifier. These two units provide a reference voltage for the ADC as well as the internal programmable current source. Both bandgap and PGA are calibrated during production. The associated calibration vectors are stored in the OTP memory. It is also possible to use an external reference instead of the internal bandgap.

TABLE 90: (BGAPCAL) BANDGAP CALIBRATION VECTOR REGISTER - SFR B3H

7	6	5	4	3	2	1	0
BGAPCAL [7:0]							

Bit	Mnemonic	Function
7:0	BGAPCAL	Bandgap data calibration

TABLE 91: (DPL1) PGA CALIBRATION VECTOR REGISTER - SFR B4H

7	6	5	4	3	2	1	0
BGAPCAL [7:0]							

Bit	Mnemonic	Function
7:0	PGACAL	8 MSBs of PGA Calibration Vector (LSB is on ISRCCAL1)

A/D Converter

The on-chip A/D converter can be configured for a number of different operating modes to meet the specific application requirements. It supports both continuous and single shot modes.

The continuous conversion mode sets the ADC to perform timed conversions of 1 or 4 channels, while the single Shot conversion sets the ADC to perform one conversion of 1 or 4 channels at any given time.

When the ADC is configured to perform 4 channel conversions, the converted data will be available in a set of four 12-bit registers mapped into the processor's SFR space (ADC channels 0-3 registers). When the ADC is configured to perform the conversion on one channel only, the conversion result is always placed into the ADC channel 0 register.

The analog input voltage range for the ADC is 0 to 2.7V and the output coding is binary with 1 LSB = Full Scale/4096. The following describes the ideal transfer function for the VERSA MIX:

TABLE 92: (ADCCTRL) ADC CONTROL REGISTER - SFR A2H

7	6	5	4
ADCIRQCLR	XVREFCAP	CALSKIP	ADCIRQ

3	2	1	0
ADCIE	ONECHAN	CONT	ONESHOT

Bit	Mnemonic	Function
7	ADCIRQCLR	ADC interrupt clear Writing 1 Clears interrupt
6	XVREFCAP	External Voltage Ref Capacitor size Select 0 = Ext Cap <= Low Value TBD 1 = Ext Cap >= 4.7uF
5	CALSKIP	1 = Skip Calibration Process 0 = Perform ADC Calibration
4	ADCIRQ	Read ADC Interrupt Flag Write 1 generate ADC IRQ
3	ADCIE	ADC interrupt enable
2	ONECHAN	1 = Conversion is performed on one channel Specified ADCINSEL 0 = Conversion is performed on 4 ADC channels
1	CONT	1 = Enable ADC continuous conversion
0	ONESHOT	1 = Force a single conversion on 1 or 4 channels

TABLE 93: (ADCCONVRLOW) ADC CONVERSION RATE REGISTER LOW BYTE - SFR A3H

Bit	Mnemonic	Function
7:0	CONVRLOW	Conversion rate low byte

TABLE 94: (ADCCONVERMED) ADC CONVERSION RATE REGISTER MED BYTE - SFR A4H

Bit	Mnemonic	Function
7:0	CONVRMED	Conversion rate medium byte

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TABLE 95: (ADCCONVRHIGH) ADC CONVERSION RATE REGISTER HIGH BYTE - SFR A5H

Bit	Mnemonic	Function
7:0	CONVRHIGH	Conversion rate high byte

TABLE 96: (ADCD0LO) ADC CHANNEL 0 DATA REGISTER, LOW BYTE - SFR A6H

Bit	Mnemonic	Function
7:0	ADCD0LO	ADC channel 0 low

TABLE 97: (ADCD0HI) ADC CHANNEL 0 DATA REGISTER, HIGH BYTE - SFR A7H

Bit	Mnemonic	Function
3:0	ADCD0HI	ADC channel 0 high

TABLE 98: (ADCD1LO) ADC CHANNEL 1 DATA REGISTER, LOW BYTE - SFR A9H

7	6	5	4	3	2	1	0
ADCD1LO [7:0]							

Bit	Mnemonic	Function
7:0	ADCD1LO	ADC channel 1 low

TABLE 99: (ADCD1HI) ADC CHANNEL 1 DATA REGISTER, HIGH BYTE - SFR AAH

7	6	5	4	3	2	1	0
-	-	-	-	ADCD1HI [3:0]			

Bit	Mnemonic	Function
3:0	ADCD1HI	ADC channel 1 high

TABLE 100: (ADC2LO) ADC CHANNEL 2 DATA REGISTER, LOW BYTE - SFR ABH

7	6	5	4	3	2	1	0
ADCD2LO [7:0]							

Bit	Mnemonic	Function
7:0	ADCD2LO	ADC channel 2 low

TABLE 101: (ADCD2HI) ADC CHANNEL 2 DATA REGISTER, HIGH BYTE - SFR ACH

7	6	5	4	3	2	1	0
-	-	-	-	ADCD2HI [3:0]			

Bit	Mnemonic	Function
7:4	-	-
3:0	ADCD2HI	ADC channel 2 high

TABLE 102: (ADCD3LO) ADC CHANNEL 3 DATA REGISTER, LOW BYTE - SFR ADH

7	6	5	4	3	2	1	0
ADCD3LO [7:0]							

Bit	Mnemonic	Function
7:0	ADCD3LO	ADC channel 3 low

TABLE 103: (ADCD3HI) ADC CHANNEL 3 DATA REGISTER, HIGH BYTE - SFR AEH

7	6	5	4	3	2	1	0
-	-	-	-	ADCD3HI [3:0]			

Bit	Mnemonic	Function
7:4	-	-
3:0	ADCD3HI	ADC channel 3 high

TABLE 104: (ADCFORCE) ADC CALIBRATION VECTOR REGISTER - SFR B1H

7	6	5	4	3	2	1	0
ADCFORCE	QNUMBER [2:0]			QVALUE [3:0]			

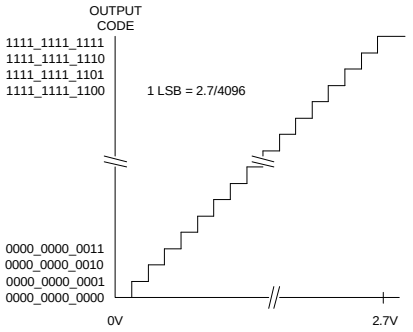
Bit	Mnemonic	Function
7	ADCFORCE	Writing 1 force ADC quartets values to be used as ADC calibration vector
6:4	QNUMBER	ADC Quartet Number (Write Only)
3:0	QVALUE	ADC Quartet value (R/W)

TABLE 105: (ADCCALTBL) ADC CALIBRATION TABLE REGISTER - SFR B2H

7	6	5	4	3	2	1	0
ADCALDATA [3:0]				ADCALADRS [3:0]			

Bit	Mnemonic	Function
7:4	ADCALDATA	Calibration data (Read Only)
3:0	ADCALADRS	Calibration address (Write Only)

FIGURE 29: IDEAL A/D CONVERTER TRANSFER FUNCTION



A/D SFR Registers

Below is a list of the specifications and related formulas for each A/D SFR Register.

- ADC Clock Divider
  - Can derive the 250kHz A/D reference clock from the system clock

Equation:

$$\text{ADC Clk ref} = \frac{f_{OSC}}{4x\ (ADCCDIV + 1)}$$

TABLE 106: (ADCCLKDIV) ADC CLOCK DIVISION CONTROL REGISTER - SFR 95H

7	6	5	4	3	2	1	0
ADCCLKDIV [7:0]							

Bit	Mnemonic	Function
7:0	ADCCLKDIV	ADC clock divider (R/W)

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• A/D Conversion Rate Registers
  • 24-bit word sets the A/D conversion rate in continuous mode

Equation:

$$\text{Conversion rate registers value (24-bit)} = \frac{f_{OSC}}{\text{Conv\_Rate} + 1}$$

• A/D Control Register
  • Enable control of the A/D
  • External ref cap select
  • Single shot/continuous operation mode select
  • 4-Channel/1-Channel control
  • A/D interrupt enable control/interrupts clear
  • A/D completion/interrupt flag

• A/D Input Mux Control
  • Selects which input is sampled in the 1-Channel mode
  • Individual control of input buffers

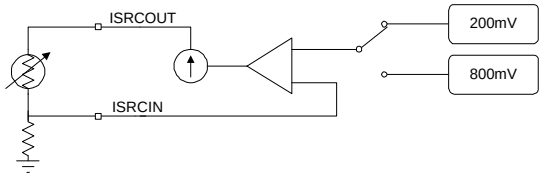
Programmable Current Source

The VERSA MIX includes a programmable current source that is calibrated to provide an output current of 33µA or 133µA and is dynamically adjustable.

The current source is intended to provide excitation to resistive sensor types connected between the ISRCOUT and ISRCIN pins

A feedback loop made of an external 6kO resistor connected between the ISRCIN pin and the analog ground ensures the accuracy and stability of the programmable current source output.

FIGURE 30: PROGRAMMABLE CURRENT SOURCE TO EXCITE SENSOR



Changing the value of the feedback resistor makes it possible to adjust the output current for specific applications. It is possible to adjust the ISRC output current up to 530µA.

TABLE 107: (ISRCCAL1) CURRENT SOURCE CALIBRATION VECTOR FOR 33? A REGISTER - SFR BCH

7	6	5	4	3	2	1	0
PGACAL0	ISRCCAL1 [6:0]						

Bit	Mnemonic	Function
7	PGACAL0	Bit 0 of PGACAL
6:0	ISRCCAL1	ISRC CAL 1 for 33µA

TABLE 108: (ISRCCAL2) CURRENT SOURCE CALIBRATION VECTOR FOR 133? A REGISTER - SFR BDH

7	6	5	4	3	2	1	0
-	ISRCCAL2 [6:0]						

Bit	Mnemonic	Function
7	-	-
6:0	ISRCCAL2	ISRC CAL 2 for 133µA

Digital Potentiometers

The VERSA MIX also has 2 digital potentiometers that the user may control by setting the bits of either the DIGPOT1 register or DIGPOT2 register.

Here is a short list of some possible applications of the digital potentiometers:

- Gain control
- Offset adjustment
- A/D input attenuation

TABLE 109: (DIGPOT1) DIGITAL POTENTIOMETER 1 CONTROL REGISTER - SFR BAH

7	6	5	4	3	2	1	0
DIGPOT1 [7:0]							

Bit	Mnemonic	Function
7-0	POT1RES	Potentiometer Value R_{pot} = (POT1RES / 256) x R_{max} (TBD)

TABLE 110: (DIGPOT2) DIGITAL POTENTIOMETER 2 CONTROL REGISTER - SFR BBH

7	6	5	4	3	2	1	0
DIGPOT2 [7:0]							

Bit	Mnemonic	Function
7-0	POT2RES	Potentiometer Value R_{pot} = (POT2RES / 256) x R_{max}

Operational Amplifier

The VERSA MIX is equipped with an operational amplifier. This op amp can be used for a wide array of analog applications. Here is a short list of some applications.

- Gain control
- Offset Control
- Reference buffering
- Integrator
- Other standard op amp applications

The op-amp on the VERSA MIX has an open-loop gain of 105 decibels, a unit gain bandwidth of 5MHz, load resistance to ground of 5kO, a load capacitance of 20pF. The slew rate of this device was measured at 5V/µs. The output voltage swing is between 0.1 and 4.9 Volts.

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Digitally Controlled Switches

On the VERSA MIX, there are two digital switches, each with 4 sub-switches. These sub-switches can be individually controlled by writing to the SFR register at B7h.

The switch-on resistance for the Digital Switches is between 20 and 80 Ohms depending on the number of sub-switches being used. If, for example, one switch is closed, there will be a resistance of 80 Ohms, and if all 4 switches are closed, there will be a resistance of 20 Ohms. Their turn on and turn off times are 1ns.

TABLE 111: (SWITCHCTRL) USER SWITCHES CONTROL REGISTERS - SFR B7H

7	6	5	4	3	2	1	0
SWITCHCTRL [7:0]							

Bit	Mnemonic	Function
7:4	SW2CTRL	Switch 2 control (composed of 4 individual switches each bit controlled) (Optional)
3:0	SW1CTRL	Switch 1 control (composed of 4 individual switches each bit controlled)

Interrupts

The VERSA MIX is a highly integrated device incorporating a vast number of peripherals for which a comprehensive set of 13 interrupts sources ease system program development. Nearly all active peripherals in the VERSA MIX are able to generate a specific interrupt that can provide feedback to the MCU core that an event has occurred or a task has been completed.

Below is a list of things that one should know about the interrupts on the VERSA MIX:

- Each digital peripheral on the VERSA MIX has an interrupt channel.
- The SPI, UARTs and I²C all have event specific flag bits.
- When the processor is in IDLE mode, an interrupt may be used to wake it up.
- The processor can run at full speed during interrupt routines.

The following tables are the interrupt enable register representations and their bit functions:

TABLE 112: (IEN0) INTERRUPT ENABLE REGISTER 0 - SFR A8H

7	6	5	4
EA1	WDT	ET2	ES0

3	2	1	0
ET1	EX1	ET0	EX0

Bit	Mnemonic	Function
7	EA1	0 = Disable all interrupts
6	WDT	Watchdog timer refresh flag. This bit is used to initiate a refresh of the watchdog timer. In order to prevent an unintentional reset, the watchdog timer the user must set this bit directly before SWDT.
5	ET2	0 = Disable Timer 2 overflow or external reload interrupt
4	ES0	0 = Disable Serial Channel 0 interrupt.
3	ET1	0 = Disable Timer 1 overflow interrupt
2	EX1	0 = Disable External Interrupt 1
1	ET0	0 = Disable Timer 0 overflow interrupt
0	EX0	0 = Disable External Interrupt 0

TABLE 113: (IEN1) INTERRUPT ENABLE 1 REGISTER -SFR E8H

7	6	5	4
EXEN2	SWDT	EX6	EX5

3	2	1	0
EX4	EX3	EX2	EADC

Bit	Mnemonic	Function
7	EXEN2	This bit enables interrupts generated from T2EX.
6	SWDT	Watchdog timer start/refresh flag. Set to activate/refresh the watchdog timer. When directly set after setting WDT, a watchdog timer refresh is performed. Bit SWDT is reset.
5	EX6	0 = Disable External Interrupt 6 1 = Enable External Interrupt 6
4	EX5	0 = Disable External Interrupt 5 1 = Enable External Interrupt 5
3	EX4	0 = Disable External Interrupt 4 1 = Enable External Interrupt 4
2	EX3	0 = Disable External Interrupt 3 1 = Enable External Interrupt 3
1	EX2	0 = Disable External Interrupt 2 1 = Enable External Interrupt 2
0	EADC	

TABLE 114: (IEN2) INTERRUPT ENABLE 2 REGISTER - SFR 9AH

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	ES1

Bit	Mnemonic	Function
7-1	-	-
0	ES1	0 = Disable Serial Channel 1 Interrupt 1 = Enable Serial Channel 1 Interrupt

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TABLE 115: (IRCON) INTERRUPT REQUEST CONTROL REGISTER - SFR 91H

7	6	5	4
EXF2	TF2	IEX6	IEX5

3	2	1	0
IEX4	IEX3	IEX2	IADC

Bit	Mnemonic	Function
7	EXF2	Timer 2 external reload flag This bit informs the user whether or not an interrupt has been generated from T2EX, provided that the EXEN2 is enabled.
6	TF2	Timer 2 overflow flag
5	IEX6	External Interrupt 6 edge flag
4	IEX5	External Interrupt 5 edge flag
3	IEX4	External Interrupt 4 edge flag
2	IEX3	External Interrupt 3 edge flag
1	IEX2	External Interrupt 2 edge flag
0	IADC	A/D converter interrupt request flag

The other interrupt registers are summarized in the tables below:

TABLE 116: (PORTIRQEN) PORT CHANGE IRQ CONFIGURATION - SFR 9FH

7	6	5	4
P07IEN	P06IEN	P05IEN	P04IEN

3	2	1	0
P03IEN	P02IEN	P01IEN	P00IEN

Bit	Mnemonic	Function
7	P07IEN	Port 0.7 IRQ on change enable 0 = Disable 1 = Enable
6	P06IEN	Port 0.6 IRQ on change enable 0 = Disable 1 = Enable
5	P05IEN	Port 0.5 IRQ on change enable 0 = Disable 1 = Enable
4	P04IEN	Port 0.4 IRQ on change enable 0 = Disable 1 = Enable
3	P03IEN	Port 0.3 IRQ on change enable 0 = Disable 1 = Enable
2	P02IEN	Port 0.2 IRQ on change enable 0 = Disable 1 = Enable
1	P01IEN	Port 0.1 IRQ on change enable 0 = Disable 1 = Enable
0	P00IEN	Port 0.0 IRQ on change enable 0 = Disable 1 = Enable

TABLE 117: (PORTIRQSTAT) PORT CHANGE IRQ STATUS - SFR A1H

7	6	5	4
P07ISTAT	P06ISTAT	P05ISTAT	P04ISTAT

3	2	1	0
P03ISTAT	P02ISTAT	P01ISTAT	P00ISTAT

Bit	Mnemonic	Function
7	P07ISTAT	Port 0.7 changed 0 = No 1 = Yes
6	P06ISTAT	Port 0.6 changed 0 = No 1 = Yes
5	P05ISTAT	Port 0.5 changed 0 = No 1 = Yes
4	P04ISTAT	Port 0.4 changed 0 = No 1 = Yes
3	P03ISTAT	Port 0.3 changed 0 = No 1 = Yes
2	P02ISTAT	Port 0.2 changed 0 = No 1 = Yes
1	P01ISTAT	Port 0.1 changed 0 = No 1 = Yes
0	P00ISTAT	Port 0.0 changed 0 = No 1 = Yes

The SPI, UARTs and I²C interfaces have event specific flag bits. It is also possible to have the interrupts wake-up the processor from IDLE mode or force it to return to full speed when an interrupt occurs.

TABLE 118: (IP0) INTERRUPT PRIORITY REGISTER 0 - SFR B8H

7	6	5	4	3	2	1	0
OWDS	WDTS	IP0 [5:0]					

Bit	Mnemonic	Function		
7	OWDS			
6	WDTS	Watchdog timer status flag. Set by hardware when the watchdog timer was started. Can be read by software.		
5	IP0.5	Timer 2 Interrupt	-	External Interrupt 6
4	IP0.4	Serial Channel 0 Interrupt	-	External Interrupt 5
3	IP0.3	Timer 1 Interrupt	-	External Interrupt 4
2	IP0.2	External Interrupt 1	-	External Interrupt 3
1	IP0.1	Timer 0 Interrupt	-	External Interrupt 2
0	IP0.0	External Interrupt 0	Serial Channel 1 Interrupt	A/D Converter Interrupt

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TABLE 119: (IP1) INTERRUPT PRIORITY REGISTER 1 - SFR B9H

7	6	5	4	3	2	1	0
-	-	IP1 [5:0]					

Bit	Mnemonic	Function		
7	-	-		
6	-	-		
5	IP1.5	Timer 2 Interrupt	-	External Interrupt 6
4	IP1.4	Serial Channel 0 Interrupt	-	External Interrupt 5
3	IP1.3	Timer 1 Interrupt	-	External Interrupt 4
2	IP1.2	External Interrupt 1	-	External Interrupt 3
1	IP1.1	Timer 0 Interrupt	-	External Interrupt 2
0	IP1.0	External Interrupt 0	Serial Channel 1 Interrupt	A/D Converter Interrupt

The following table summarizes the interrupt sources, the natural priority and the associated interrupt vector addresses.

TABLE 120: INTERRUPT SOURCES AND NATURAL PRIORITY

Interrupt	Interrupt Vector
DEBUG PORT	043h
INT0	003h
UART1	083h
TIMER 0	00Bh
SPI Tx	04Bh
INT1 & PORT CHANGE	013h
SPI RX & SPI RX OVERRUN	053h
TIMER 1	01Bh
I2C (Tx, Rx, Rx Overrun)	05Bh
UART0	023h
MAC OVERFLOW BIT	063h
TIMER 2	02Bh
A/D CONVERTER	06Bh

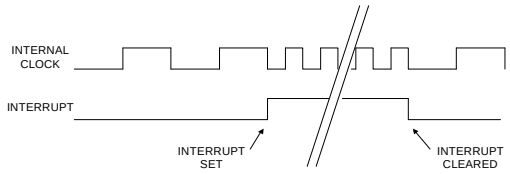
Clock Control Circuitry

The VERSA MIX clock control circuitry serves to dynamically adjust the clock speed of the VERSA MIX.

General Clock Control Unit

- Permits dynamic adjustment of system clock
- Serves to lower power consumption
- Possible clock rates: Fosc/1 down to Fosc/512
- Can make the clock return to full speed once an interrupt occurs

FIGURE 31: CLOCK TIMING WHEN AN INTERRUPT OCCURS



Processor Specific Power Saving Modes

IDLE Mode:

- µP clock is stopped
- The internal clock and enabled peripherals continue to run
- Any enabled interrupts can make the µP exit IDLE mode

Stop Mode:

- uP clock is stopped
- All internal clocking is stopped
- The following events can restart the processor: Reset, INT0, INT1, Debug Port, SPI Rx/Rx Overrun, and I²C

TABLE 121: (CLKDIVCTRL) CLOCK DIVISION CONTROL REGISTER -SFR 94h

7	6	5	4
SOFTRST	-	-	IRQNORMSPD

3	2	1	0
MCKDIV [3:0]			

Bit	Mnemonic	Function
7	SOFTRST	Writing 1 into this bit location provokes a reset. Read as a 0
6:5	-	-
4	IRQNORMSPD	0 = Full Speed in IRQ 1 = Selected speed during IRQs
3:0	MCKDIV	Master Clock Divisor 0000 – Sys CLK 0001 = SYS /2 0010 = SYS /4 0011 = SYS /8 0100 = SYS /16 0101 = SYS /32 0110 = SYS /64 0111 = SYS /128 1000 = SYS /256 1001 = SYS /512 (…) 1111 = SYS /32768

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TABLE 122: (CKCON) CLOCK CONTROL - SFR 8EH

7	6	5	4	3	2	1	0
-	-	-	-	-	STRETCH [2:0]		

Bit	Mnemonic	Function
7:3	-	-
2:0	Stretch	Used for changing the stretch value for the read and write signal widths.

TABLE 123: STRETCH MEMORY CYCLE WIDTH

CKCON Register			Stretch Value
STRETCH_2	STRETCH_1	STRETCH_0	
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Stretch Value	Read Signal Width		Write Signal Width	
	memaddr	memrd	memaddr	memwr
0	1	1	2	1
1	2	2	3	1
2	3	3	4	2
3	4	4	5	3
4	5	5	6	4
5	6	6	7	5
6	7	7	8	6
7	8	8	9	7

Reset and Power Control

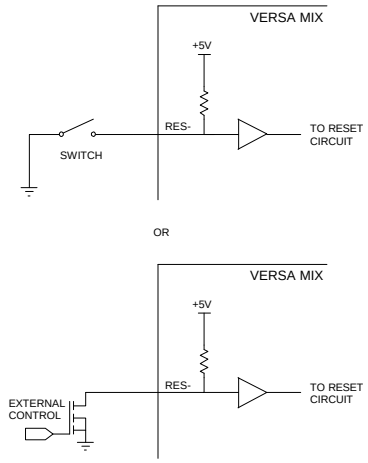
Reset Control

The VERSA MIX provides two resets, *POR_n* and RES-. *POR_n* is the power-on reset that is generated internally by the Power-On-Reset/Brown-Out device.

- Upon Reset, all SFR locations return to their default values and peripherals are disabled
- The internal 256 byte RAM cells are reset to 00h
- The external 1K RAM memory block is not affected by reset
- The VERSA MIX requires no external component for Reset (on power-up)
- No debouncing circuit is required when a manual Reset switch is used
- An internal pull-up is provided on the reset input

It is also possible to control the VERSA MIX reset line externally as shown on the following figures.

FIGURE 32: EXTERNAL RESET CONTROL



Power Control

The power management unit has two modes of operation: IDLE mode and STOP mode.

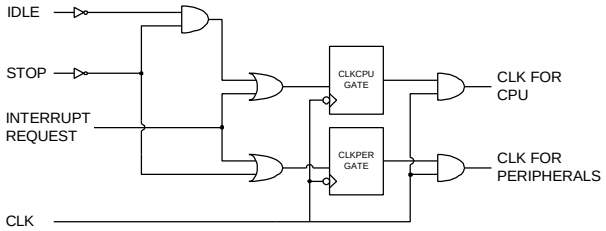
Idle Mode

In order to enter IDLE mode, the user must set the IDLE bit of the PCON register (Table 125). When the VERSA MIX is in IDLE mode, the internal clock and peripherals are still running. Power consumption drops because the CPU is not active. As soon as an interrupt or reset occurs, the CPU exits the IDLE state. To exit Idle mode, the 8051 does not require that the reset and interrupt signals 0/1 be level.

Stop Mode

In order to enter STOP mode, the user must set the STOP bit of the PCON register. In this mode, in contrast to IDLE mode, all internal clocking shuts down. The CPU will exit this state only when a no-clocked external interrupt or reset occurs (internal interrupts are not possible because they require clocking activity). In order to wake up from Stop mode, the 8051 requires that the reset and interrupt signals 0/1 be level.

FIGURE 33: POWER MANAGEMENT ON THE VERSA MIX



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Represented below is the power control register of the VERSA MIX.

TABLE 124: (PCON) POWER CONTROL (CPU) - SFR 87H

7	6	5	4	3	2	1	0
SMOD_0	-	-	-	GF1	GF0	STOP	IDLE

Bit	Mnemonic	Function
7	SMOD	The speed in Mode 2 of Serial port 0 is controlled by this bit. When SMOD= 1, f_{clk} /32. This bit is also significant in Mode 1 and 3, as it adds a factor of 2 to the baud rate.
6	-	-
5	-	-
4	-	-
3	GF1	Not used for power management
2	GF0	Not used for power management
1	STOP	Stop mode control bit. Setting this bit turns on the STOP Mode. STOP bit is always read as 0.
0	IDLE	IDLE mode control bit. Setting this bit turns on the IDLE mode. IDLE bit is always read as 0.

Watchdog Timer

The watchdog timer is a 15-bit counter. It consists of WDTH and WDTL: These two internal registers are used to keep track of the count of the watchdog timer. On the watchdog timer, the counter is incremented once every 24 or 384 clock cycles. Upon a reset, the watchdog is disabled and all registers are set to zero.

From the schematic in Figure 32, we notice that the watchdog timer consists of a 15-bit counter WDTL/H, a reload register WDTREL, prescalers that divide one twelfth of the oscillator by 2 or 16, and some control logic.

Start Procedure

In order for the watchdog to begin counting, the user must set bit 6 (WDOGEN) of DIGPWREN (Table 32).

In order to start the watchdog timer using the hardware automatic start procedure, we must examine the state of the SWDT signal during an active internal reset. If this bit is set , the watchdog will begin to run with default setting i.e. all registers will be set to zero.

If this above condition is not met, the user may start the watchdog later. This start will occur when the signal becomes active. Note that once the watchdog has started to count, it cannot be stopped until the RST signal is set to 1.

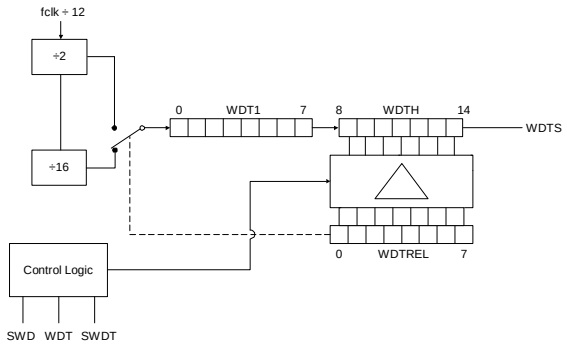
When the WDT registers enter the state 7CFFh, the asynchronous signal, WDTS, will become active. This signal will set bit 6 in the IP0 register. Setting this bit requests a reset state.

TABLE 125: (WDTREL) WATCHDOG TIMER RELOAD REGISTER - SFR D9H

7	6	5	4	3	2	1	0
PRES	WDTREL [6:0]						

Bit	Mnemonic	Function
7	PRES	Prescaler select bit. When set, the watchdog is clocked through an additional divide-by-16 prescaler.
6-0	WDTREL	7-bit reload value for the high-byte of the watchdog timer. This value is loaded to the WDT when a refresh is triggered by a consecutive setting of bits WDT and SWDT.

FIGURE 34: WATCHDOG TIMER



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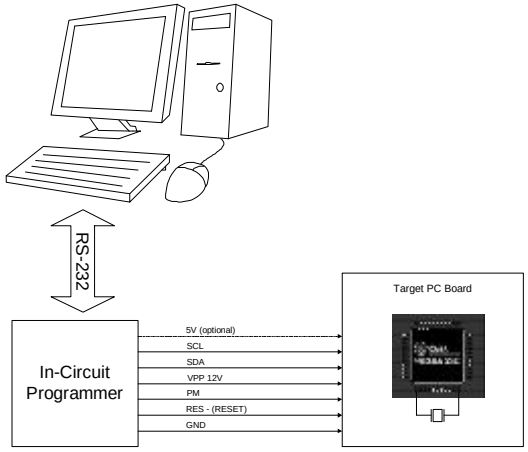
VERSA MIX Programming

When the PM pin is set to 1, the I²C interface serves to program the Flash memory of the VERSA MIX.

- The VERSA MIX Flash memory is programmed using the I²C interface in slave mode and control lines
- In-circuit programming is easy to implement at the board level
- An external programming voltage of 12V is required (provided by programmer)
- The VERSA MIX can be programmed using the DevBoard or the In-Circuit programmer

FIGURE 35: VERSA MIX PROGRAMMING



Author: Steven Czerniak

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TEL：021-28311762 56703037 13701955389 FAX：021-56703037
西安分公司：西安高新开发区 20 所(中国电子科技集团导航技术研究所)
西安劳动南路 88 号电子商城二楼 D23 号
TEL：029-81022619 13072977981 FAX:029-88789382