

LED Driver IC

DESCRIPTION

is an LED Controller driven on a 1/4 to 1/7 duty factor. Twelve/nine segment output lines, 4 to 7 grid output lines, one display memory, control circuit are all incorporated into a single chip to build a highly reliable peripheral device for a single chip microcomputer. Serial data is fed to DL8835 via a three-line serial interface. Housed in a 24-pin SO Package, DL8835's pin assignments and application circuit are optimized for easy PCB Layout and cost saving advantages.

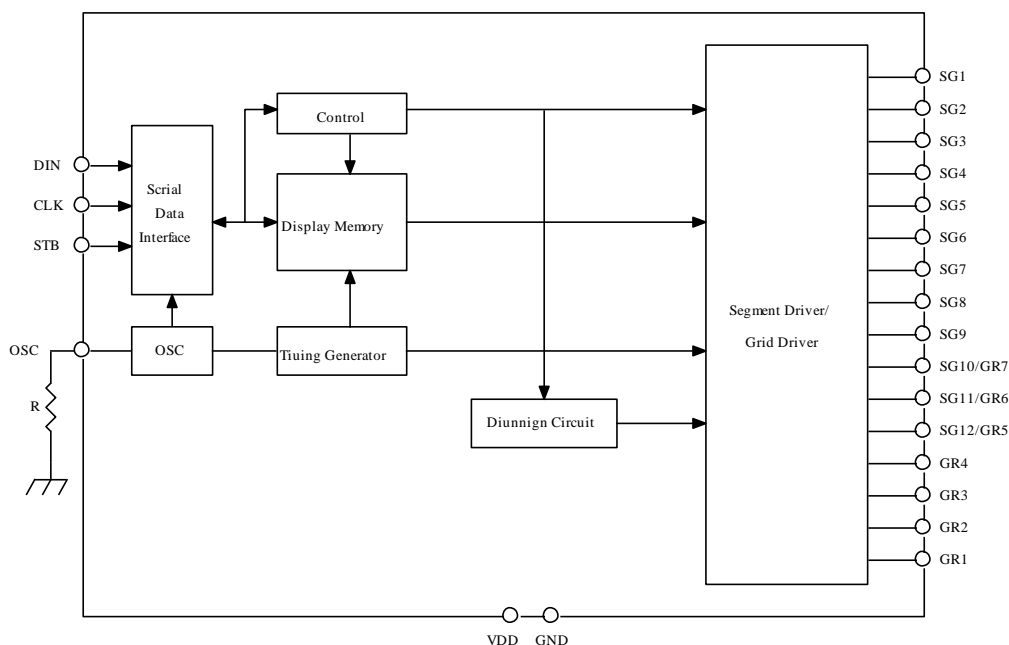
FEATURES

- CMOS Technology
- Low Power Consumption
- 8-Step Dimming Circuitry
- Serial Interface for Clock, Data Input, Strobe Pins
- Available in 24-pin, SO Package

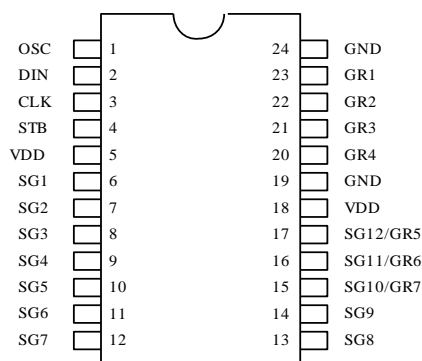
APPLICATION

- Micro-computer Peripheral Device

BLOCK DIAGRAM

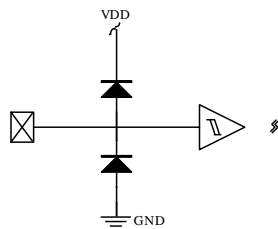


PIN CONFIGURATION

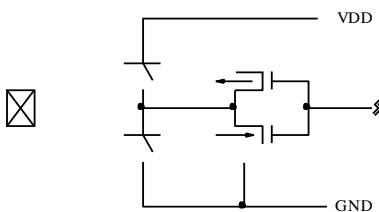


INPUT / OUTPUT CONFIGURATIONS

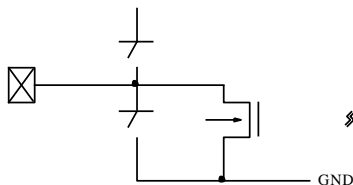
The SUNSTAR 单片机专用电路 of the input and output circuits of the logic section are shown below.
Input Pins: CLK, STB & DIN



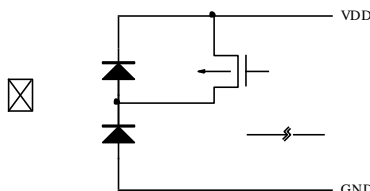
Output Pins: SG10/GR7, SG11/GR6, SG12/GR5



Output Pins: GR1 to GR4



Output Pins: SG1 to SG9



PIN DESCRIPTION

Pin Name	I/O	DeScription	Pin NO.
OSG	I	OSGillator Input Pin A resistor is connected to this pinto determine the oSGillation frequency	1
DIN	I	Data Input Pin This pin inputs serial data at the rising edge of the shift clock (starting from the lower bit)	2
CLK	I	Clock Input Pin This pin reads serial data at the rising edge.	3
STB	I	Serial Interface Strobe Pin The data input after the STB has fallen is processed as a command. When this pin is " HIGH ", CLK is ignored.	4
VDD	-	Power Supply	5,18
SG1 to SG9	O	Segment Output Pins (p-channel, open drain)	6~14
SG10/GR7 to SG12/GR5	O	Segment Output Pin/Grid Output Pin (CMOS Output)	15~17
GND	-	Ground Pin	19,24
GR4 to GR1	O	Grid Output Pins (n-channel, open drain)	20~23

FUNCTIONAL DESCRIPTION

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Commands

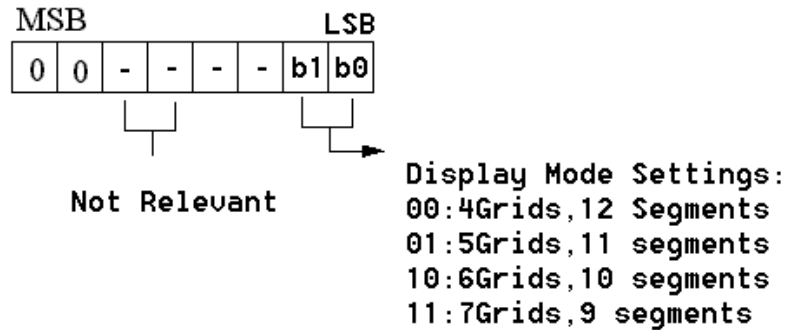
A command is the first byte (b0 to b7) inputted to DL8835 via the DIN Pin after STB Pin has changed from "HIGH" to "LOW" State. If for some reason the STB Pin is set to "HIGH" while data or commands are being transmitted, the serial communication is initialized, and the data/commands being transmitted are considered invalid.

COMMAND 1: DISPLAY MODE SETTING COMMANDS

DL8835 provides 4 display mode settings as shown in the diagram below: As stated earlier a command is the first one byte (b0 to b7) transmitted to DL8835 via the DIN Pin when STB is "LOW". However, for these commands, Bit No. 3 to Bit No.6 (b2 to b5) are ignored, Bit No. 7 & Bit No. 8 (b6 to b7) are given a value of "0".

The Display Mode Setting Commands determine the number of segments and grids to be used (1/4 to 1/7 duty, 12 to 9 segments). When these commands are executed, the display is forcibly turned off. A display command "ON" must be executed in order to resume display. If the same mode setting is selected, no command execution is take place, therefore, nothing happens.

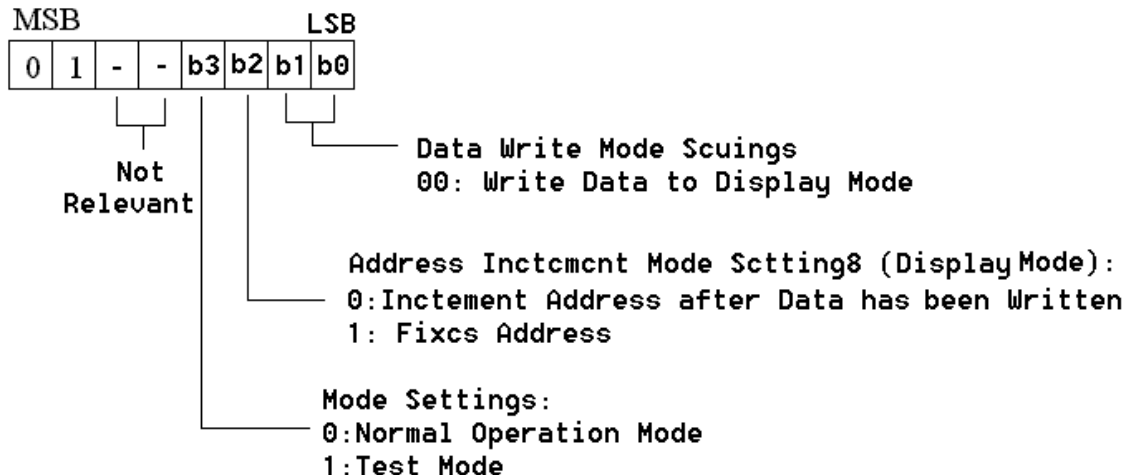
When Power is turned "ON", the 7-Grid , 9-Segment Mode is selected.



COMMAND 2: DATA SETTING COMMANDS

The Data Setting Commands executes the Data Write Mode for DL8835. The Data Setting Command, the bits 5 and 6 (b4, b5) are ignored, bit 7 (b6) is given the value of "1" while bit 8 (b7) is given the value of "0". Please refer to the diagram below.

When power is turned ON, bit 4 to bit 1 (b3 to b0) are given the value of "0".



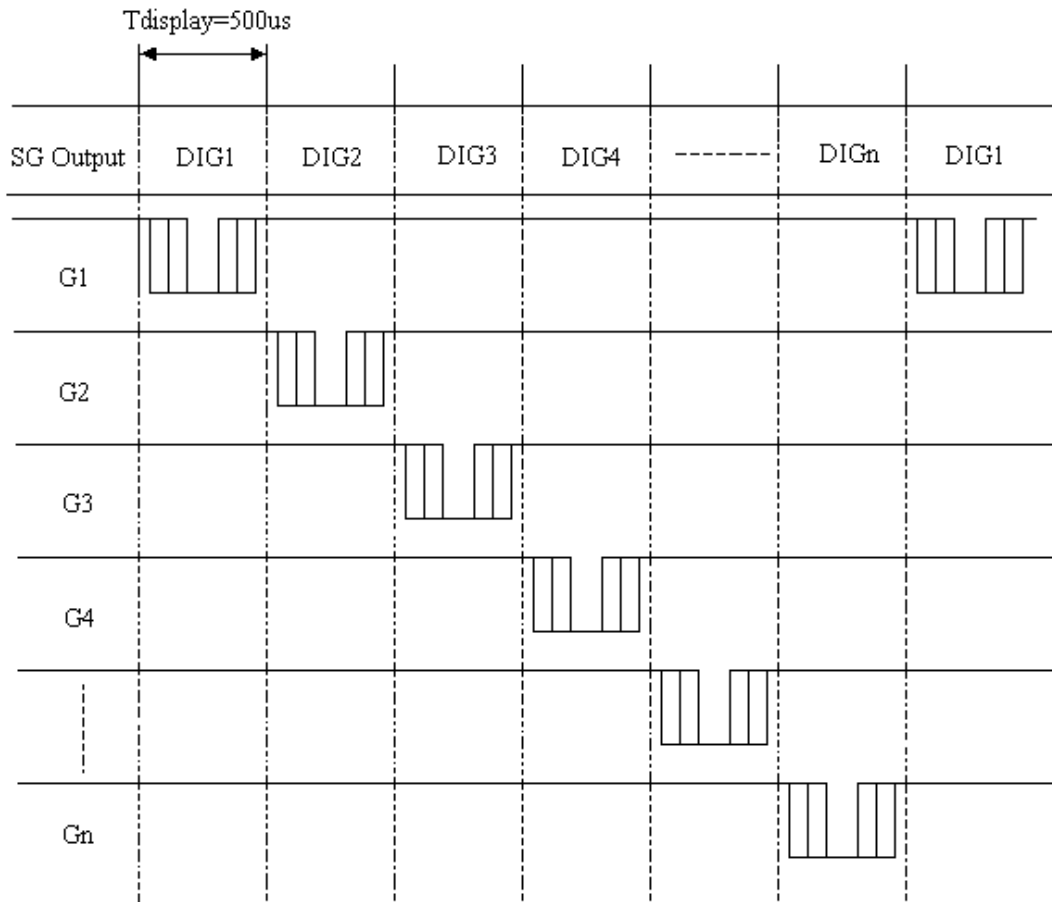
COMMAND 3: ADDRESS SETTING COMMANDS

Address Setting Commands are used to set the address of the display memory. The address is

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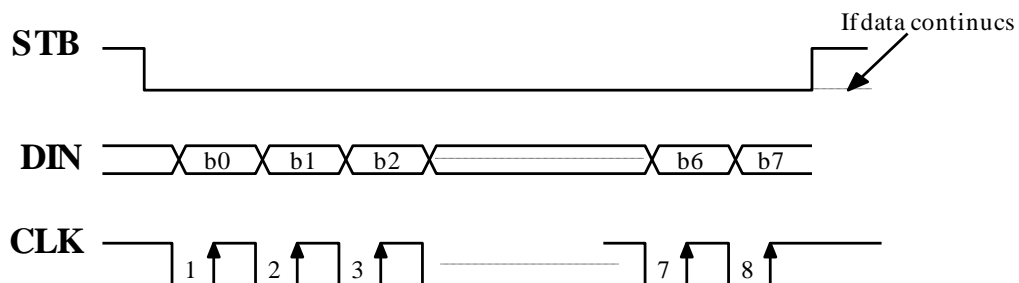
DISPLAY TIMING WAVEFORM

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SERIAL COMMUNICATION FORMAT

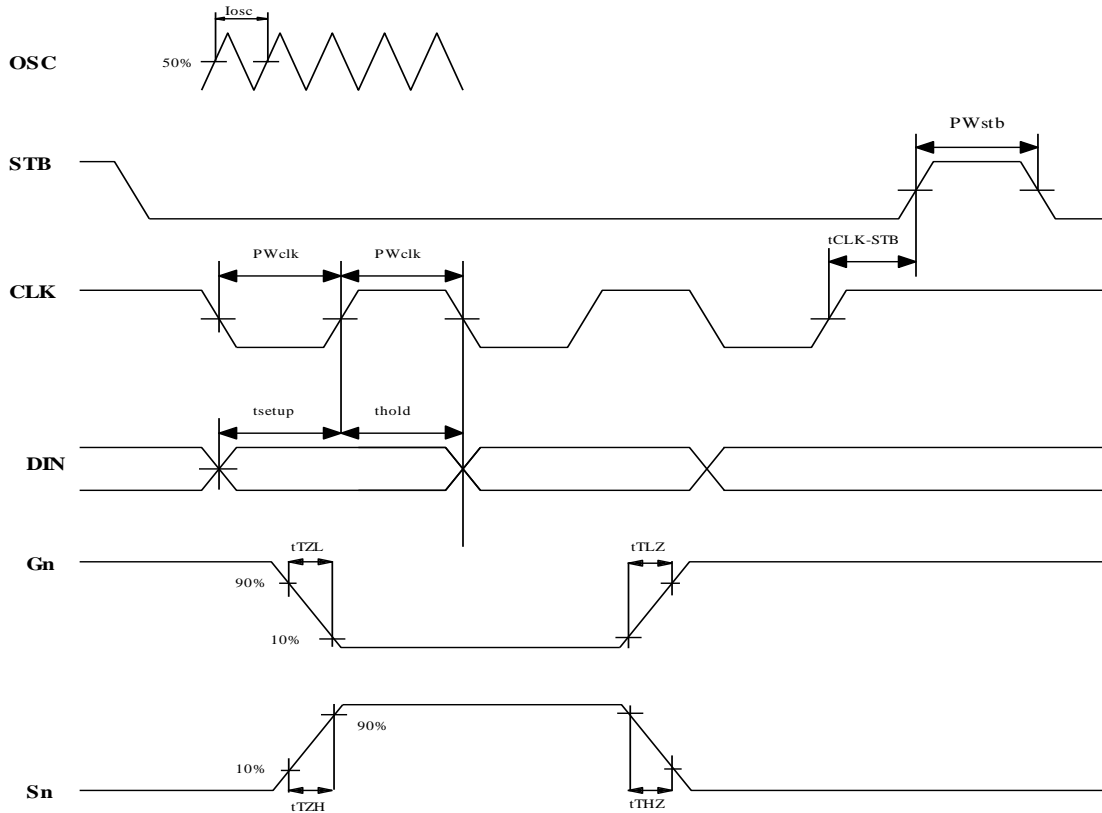
The following diagram shows the DL8835 serial communication format.



SWITCHING CHARACTERISTIC WAVEFORM

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DL8835 Switching Characteristics Waveform is given below.

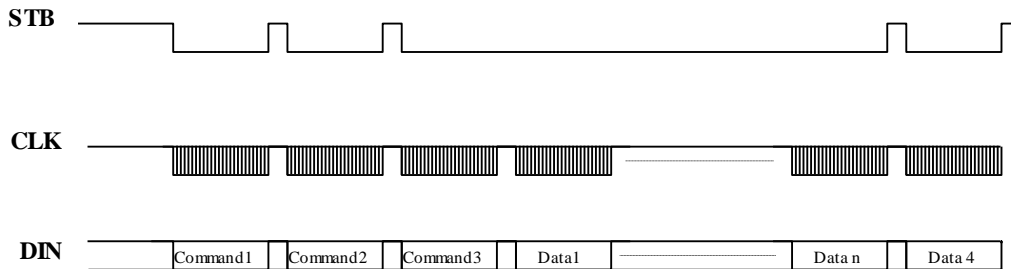


where: PW_{CLK} (Clock Pulse Width) $\cong 400ns$
 t_{setup} (Data Setup Time) $\cong 100ns$
 $t_{CLK-STB}$ (Clock-Strobe Time) $\cong 1\mu s$
 t_{TZH} (Rise Time) $\cong 1\mu s$
 $t_{TTL} < 1\mu s$

PW_{STB} (Strobe Pulse Width) $\cong 1\mu s$
 t_{hold} (Data Hold Time) $\cong 100ns$
 t_{THZ} (fall Time) $\cong 10\mu s$
 f_{oSG} = OSGillation Frequency
 $t_{TLZ} < 10\mu s$

APPLICATIONS

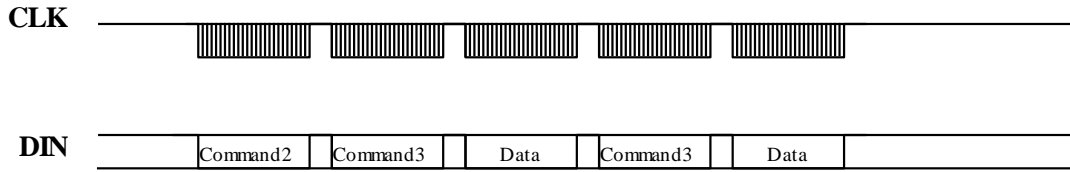
Display memory is updated by is incrementing addresses. Please refer to the following diagram.



where: Command 1: Display Mode Setting
 Command 2: Data Setting Command
 Command 3: Address Setting Command
 Data 1 to n : Transfer Display Data (14 Bytes max.)
 Command 4: Display Control Command

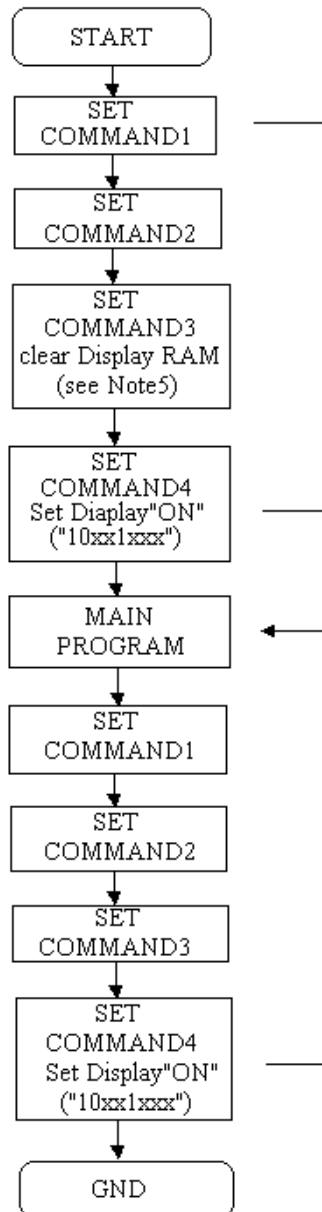
The following diagram shows the waveforms when updating specific addresses.

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Where: Command2-- Data Setting Command
 Command3-- Address Setting Command
 Data--Display Data

RECOMMENDED SOFTWARE PROGRAMMING FLOWCHART



Note: 1. Command 1: Display Mode Setting Commands

2. Command 2: Data Setting Commands

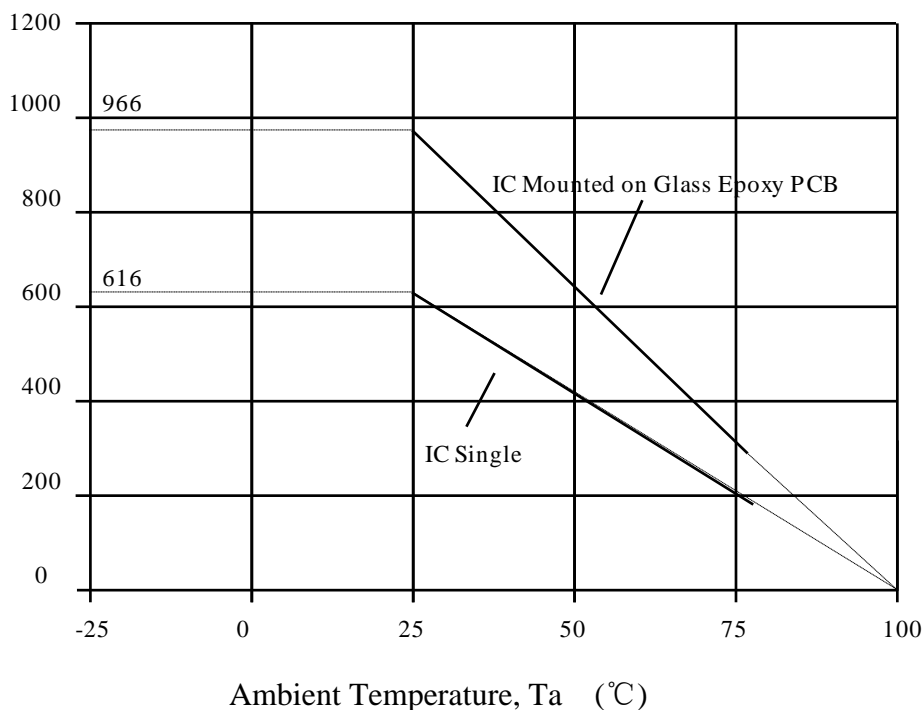
3. Command 3 : Address Setting Commands

4. Command 4 : Display Control Commands

5. When IC power is applied for the first time, the contents of the Display RAM are not defined; thus, it is strongly suggested that the contents of the Display RAM must be cleared during the initial setting.

SOP 24L (300MIL) THERMAL PERFORMANCE IN STILL AIR

Junction Temperature: 100 °C



ABSOLUTE MAXIMUM RATINGS

(Unless otherwise stated, Ta=25°C, GND=0V)

Parameter	Symbol	Rating	Units
Supply Voltage	V _{DD}	-5.0 to +7.0	Volt
Logic Input Voltage	V _I	-0.5 to V _{DD} +0.5	Volts
Driver Output Current/Pin	I _{OLGR}	+250	mA
	I _{OHS}	-50	mA
Maximum Driver Output Current/Total	I _{TOTAL}	400	mA

RECOMMENDED OPERATING RANGE

(Unless otherwise stated, Ta=-20 to +70°C, GND=0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Logic Supply Voltage	V _{DD}	4.5	5	5.5	V
Dynamic Current (see Note)	I _{DDdyn}	-	-	5	mA
High-Level Input Voltage	V _{IH}	0.8V _{DD}	-	V _{DD}	V
Low-Level Input Voltage	V _{IL}	0	-	0.3V _{DD}	V

Note: Test Condition: Set Display Control Commands = 80H (Display Turn OFF State)

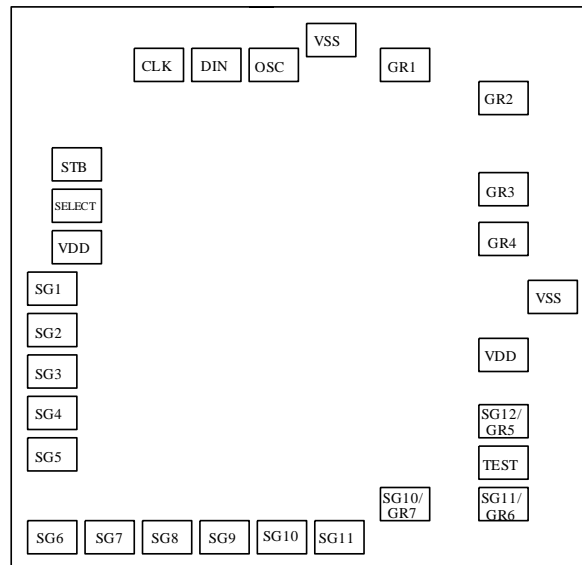
ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, V_{DD}=5V, GND=0V, Ta=25°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
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SUNSTAR单片机专用电路 High-Level Output Current	$I_{OHSG(1)}$	$V_O=V_{DD}-1V$ SG1 to SG9, SG10/GR7 to SG12/GR5	-10	-14	-30	mA
	$I_{OHSG(2)}$	$V_O=V_{DD}-2V$ SG1 to SG9, SG10/GR7 to SG12/GR5	-20	-25	-50	mA
Low-Level Output Current	I_{OLGR}	$V_O=0.3V$ GR1 to GR4, SG10/GR7 to SG12/GR5	100	140	-	mA
Segment High-Level Output Current Tolerance	I_{TOLSG}	$V_O=V_{DD}-1V$ SG1 to SG9 SG10/GR7 to SG12/GR5	-	-	± 5	%
High- Level Input Voltage	V_{IH}	-	$0.8V_{DD}$	-	-	V
Low- Level Input Voltage	V_{IL}	-	-	-	$0.3 V_{DD}$	V
OSGillation Frequency	f_{oSG}	R=51 Kohms	350	500	650	KHz

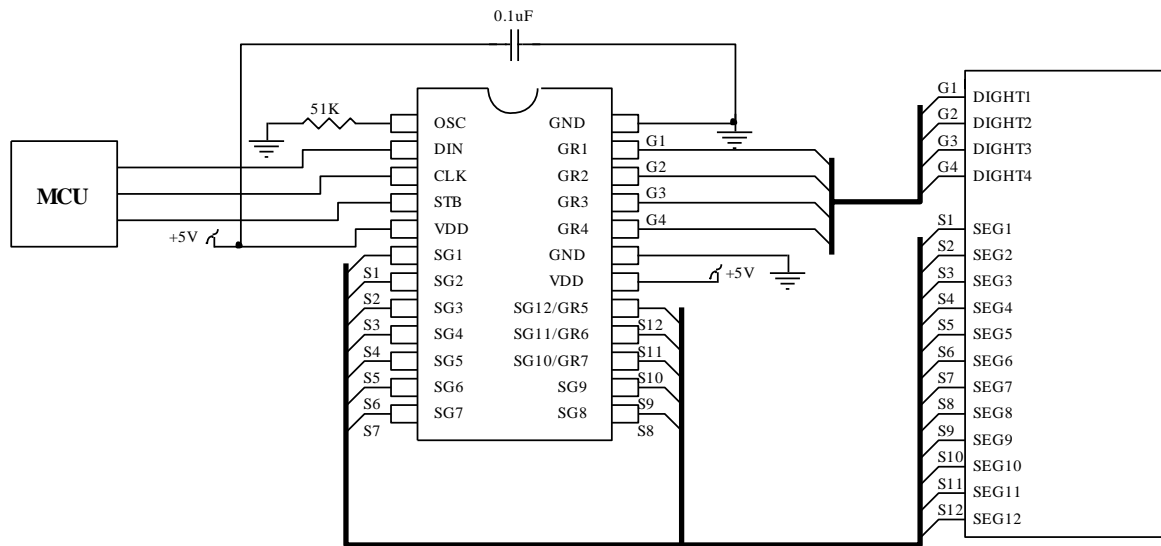
PAD



No	PAD	X	Y	No	PAD	X	Y
1	STB	103.7	1064	15	SG10/GR7	737	136.5
2	SELECT	103.7	946.8	16	SG11/GR6	956	136.5

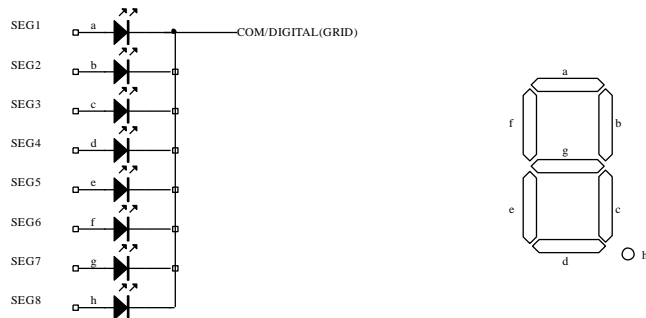
3	VDD	103.7	836.8	17	TEST	969.2	288.5
4	SG1	46.5	724.3	18	GR5	956	375.5
5	SG2	46.5	614.3	19	VDD	956	498.4
6	SG3	46.5	504.3	20	VSS	1069.6	608.4
7	SG4	46.5	394.3	21	GR4	956	779.6
8	SG5	46.5	284.3	22	GR3	956	974.4
9	SG6	48.8	51.5	23	GR2	956	1191
10	SG7	158.8	51.5	24	GR1	766.8	1226
11	SG8	268.8	51.5	25	VSS	619.8	1349.6
12	SG9	378.8	51.5	26	OSG	504.4	1256.3
13	SG10	488.8	51.5	27	DIN	386.9	1256.3
14	SG11	598.8	51.5	28	CLK	264	1256.3

APPLICATION CIRCUIT



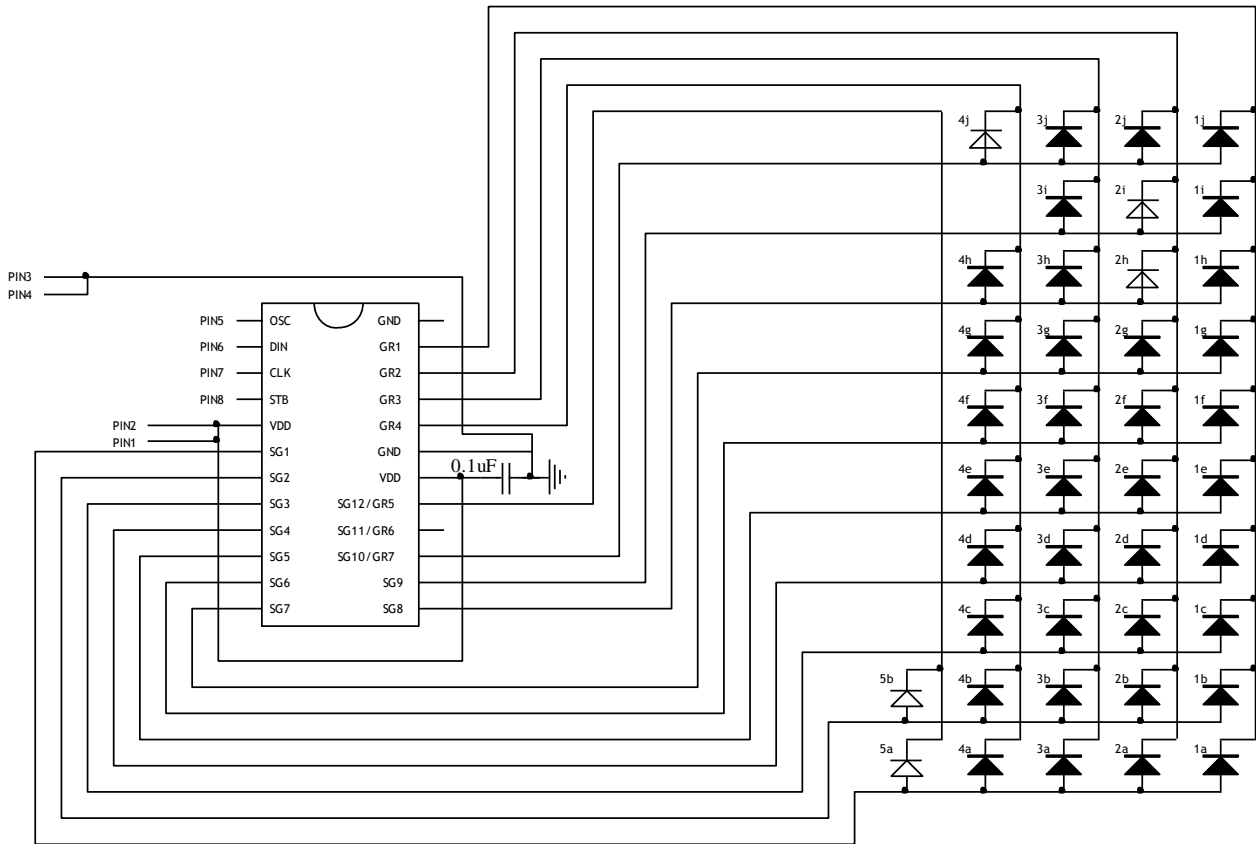
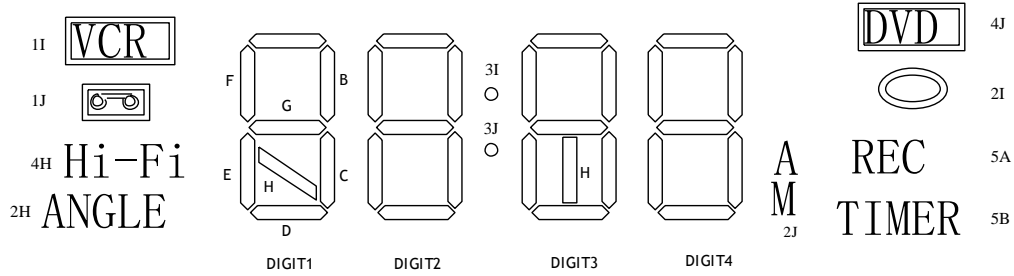
Note: The capacitor (0.1uF) connected between the GND and VDD Pins must be located as near as possible to the DL8835 chip.

COMMON CATHODE TYPE LED PANEL:



INTERNAL CIRCUIT DIAGRAM PIN CONNECTION

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NOTE: THE SIGN " " IS STANDARD FOR GREEN CHIP.
 THE SIGN " " IS STANDARD FOR RED ORANGE CHIP.
 THE SIGN " " IS STANDARD FOR AMBER CHIP.