RX3930 Low Power ISM-band FM/FSK Receiver IC

Description

The RX3930 is a low power 315/433/868/915 MHz FM/FSK receiver IC which is suitable for use in the North American 315/915 MHz and the European 433/868 MHz ISM bands.

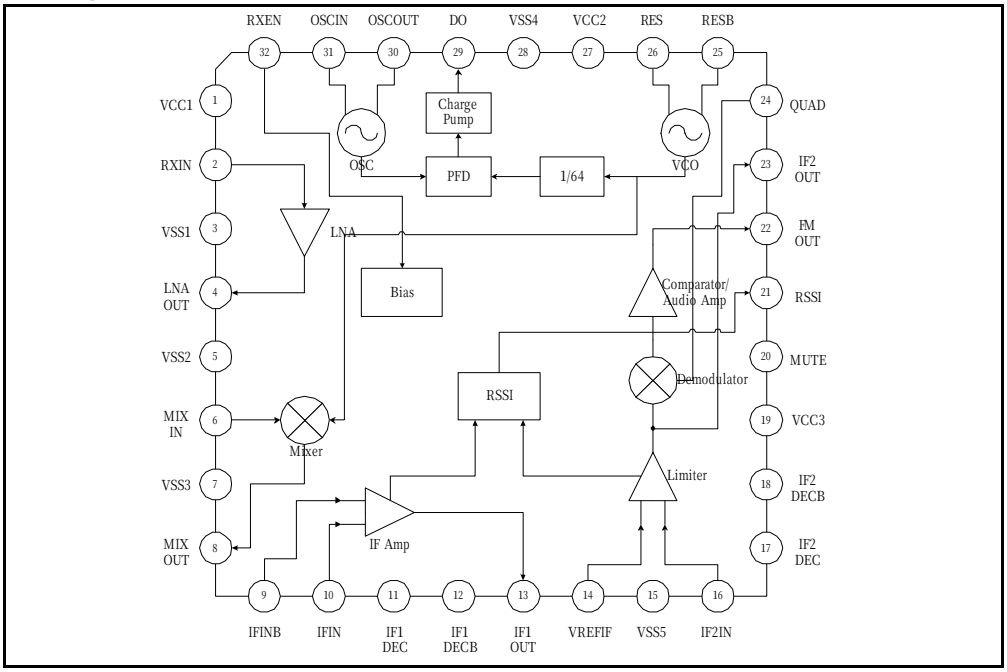
Features

- Integrated VCO with fixed ÷ 64 prescaler, phase/frequency detector, and reference oscillator forming complete phase-locked loop
- User selectable FM (sinusoidal) or FSK (CMOS compatible) output by the MUTE pin
- RSSI output with 70 dB of dynamic range
- Receiver enable pin for power saving (1 μA current consumption in stand-by mode)
- TQFP 32L package (5 mm x 5 mm)

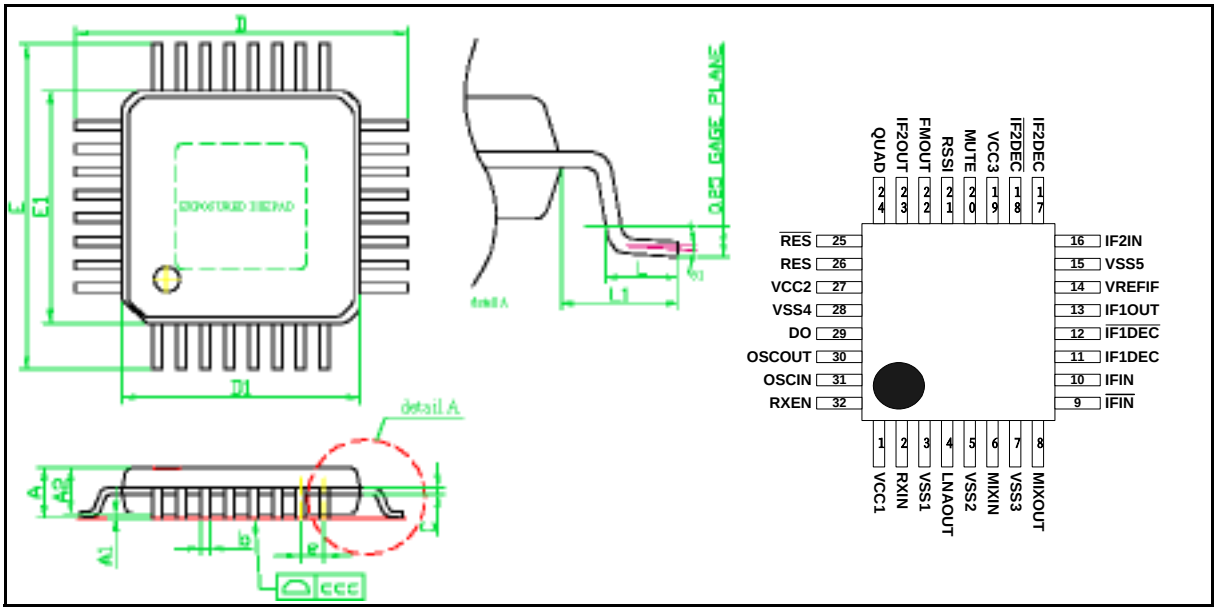
Applications

- Wireless mouse / joystick
- Wireless voice transmission
- Wireless car alarm system

Block Diagram

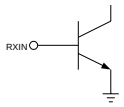
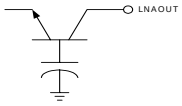
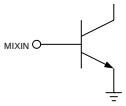
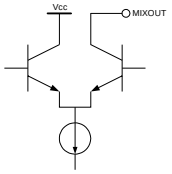
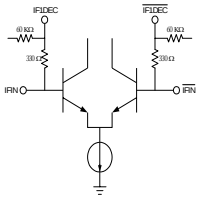
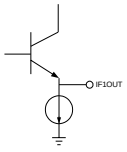


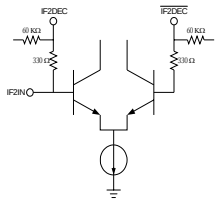
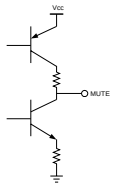
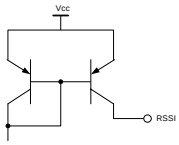
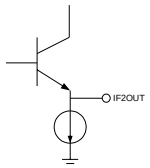
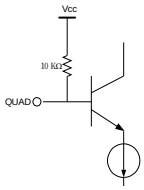
Package and Pin Assignment: 32L, TQFP

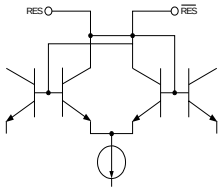
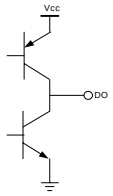
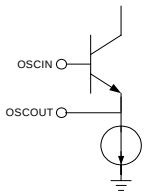


Symbols	Dimensions in mm			Dimensions in inches		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.17	0.22	0.27	0.007	0.009	0.011
C	0.09	—	0.20	0.003	—	0.008
D1	4.90	5.00	5.10	0.193	0.197	0.201
D	6.80	7.00	7.20	0.267	0.275	0.283
E1	4.90	5.00	5.10	0.193	0.197	0.201
E	6.80	7.00	7.20	0.267	0.275	0.283
e	—	0.50 (typ.)	—	—	0.02 (typ.)	—
L	0.45	0.60	0.75	0.018	0.024	0.029
L1	—	1.00 (ref.)	—	—	0.039 (ref.)	—
θ1	0°	3.5°	7°	0°	3.5°	7°
ccc	—	—	0.008	—	—	0.003

Pin Descriptions

Pin	Name	I/O	Description	Interface Schematic
1	VCC1	POWER	DC voltage supply for the RF section. A bypass capacitor should be added between this pin and ground (47 pF is recommended for 915 MHz and 100 pF is recommended for 433 MHz).	
2	RXIN	I	RF amplifier input for the receiver. It requires a matching network from the antenna to the RXIN pin for optimum sensitivity.	
3	VSS1	GND	Ground for RF amplifier. It should immediately be connected to the ground plane for best performance.	
4	LNAOUT	O	LNA output. This pin is the open-collector structure and must be connected to the DC bias by an external inductor. A series capacitor may be used to match the LNA output and the mixer input.	
5	VSS2	GND	Ground for 40 dB IF limiting amplifier. It should immediately connect to the ground plane for the best performance.	
6	MIXIN	I	RF input to RF Mixer. An L-C matching network should be connected between the LNA output and the mixer input.	
7	VSS3	GND	Ground for RF Mixer.	
8	MIXOUT	O	IF output from RF Mixer. An external inductor is conected from this pin to the DC bias and a series capacitor is used to match the 330 ohm terminal impedance of the 10.7 MHz ceramic filter. In addition, a 15 pF capacitor is recommended to be put from this pin to the ground.	
9	$\overline{\text{IFIN}}$	I	Inverting IF input of the 40 dB limiting amplifier (requires 10 nF DC blocking capacitor).	
10	IFIN	I	Same as pin 9 except non-inverting amplifier input.	
11	IF1DEC	I/O	DC feedback for 40 dB limiting amplifier (requires 10 nF bypass capacitor).	see pin9 and pin10
12	$\overline{\text{IF1DEC}}$	I/O	See pin 11.	
13	IF1OUT	O	IF output from the 40 dB limiting amplifier. This output pin has a nominal 330 ohm output impedance and may be directly connected to the 10.7 MHz ceramic filter.	

Pin	Name	I/O	Description	Interface Schematic
14	VREFIF	O	DC voltage reference for the IF limiting amplifier (requires 10 nF capacitor).	
15	VSS5	GND	Ground for 60 dB IF limiting amplifier. It should immediately be connected to the ground plane for best performance.	
16	IF2IN	I	Inverting input to the 60 dB limiting amplifier (requires 10 nF DC blocking capacitor).	
17	IF2DEC	I/O	DC feedback node for the 60 dB limiting amplifier (required 10 nF bypass capacitor).	
18	$\overline{\text{IF2DEC}}$	I/O	See pin 17	
19	VCC3	POWER	DC voltage supply to the 60 dB IF limiting amplifier. A bypass capacitor should be added between this pin and ground (10 nF is recommended for 10.7 MHz IF application).	
20	MUTE	I	Control pin for FMOUT output. MUTE = L is FSK mode; MUTE = H disables the FMOUT output; MUTE = floating is FM mode.	
21	RSSI	O	Received signal strengh indicator output. Outputs a DC voltage (0.5 V – 2.5 V) proportional to the received signal strength.	
22	FMOUT	O	Demodulator output. The output level is CMOS-compatible in FSK mode and linear sinusoidal in FM mode.	
23	IF2OUT	O	IF output from the 60 dB limiting strip. A 2.7 pF capacitor is connected between this pin and the QUAD input (pin 24).	
24	QUAD	I	FM demodulator input (not AC coupled). A DC blocking capacitor is required to avoid a DC path to ground. An L-C tank resonator or a ceramic discriminator should be connected to this pin.	

Pin	Name	I/O	Description	Interface Schematic
25	$\overline{\text{RES}}$	I/O	DC voltage supply to VCO through an external resonator inductor. The VCO resonator tank is connected to $\overline{\text{RES}}$ and RES (pins 25 and 26).	
26	RES	I/O	See pin 25.	
27	VCC2	POWER	DC voltage supply to the frequency synthesizer. A bypass capacitor should be added between this pin and ground.	
28	VSS4	GND	Ground for the frequency synthesizer.	
29	DO	I/O	Output of the charge pump. An R-C low-pass filter is used from this pin to ground and determines the PLL bandwidth.	
30	OSCIN	I/O	Crystal oscillator input (transistor base). A 100 pF capacitor should be connected between this pin and OSCOUT (pin 31).	
31	OSCOUT	I/O	Crystal oscillator output (transistor emitter). A 100 pF capacitor should be connected between this pin and ground.	
32	RXEN	I	Receiver enable pin. RXEN = H enables the entire RX3930 receiver IC and RXEN = L puts the entire receiver IC into stand-by mode).	

Absolute Maximum Ratings

V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC1} V_{CC2}	V_{SS} – 0.5 to V_{SS} + 5.5	V
Operating temperature range	T_{OPR}	–40 to 85	°C
Storage temperature range	T_{STG}	–40 to 150	°C
Soldering temperature range	T_{SLD}	255	°C
Soldering time range	t_{SLD}	10	s

Recommended Operating Conditions

V_{SS} = 0 V

Parameter	Symbol	Value			Unit
		min.	typ.	max.	
Supply voltage range	V_{CC1}	2.4	3.6	5.0	V
	V_{CC2}	2.4	3.6	5.0	V
	V_{CC3}	2.4	3.6	5.0	V
Operating temperature	T_A	–10	27	60	°C

Receiver Characteristics

(V_{CC1}, V_{CC2}, V_{CC3} = 2.4 to 5.0 V, V_{SS} = 0 V, RXEN = high, T_A = –10 to 60 °C unless otherwise noted)

Parameter	Symbol	Condition	Value			Unit
			min.	typ.	max.	
Input RF frequency range			300		1000	MHz
Sensitivity	P_{SENS}	BW_{IF} = 180 KHz f_{RF} = 915 MHz BER < 0.001		–97		dBm
Maximum RF input power	P_{RF_IN}			–20		dBm
LO leakage	α_{LO}			–55		dBm

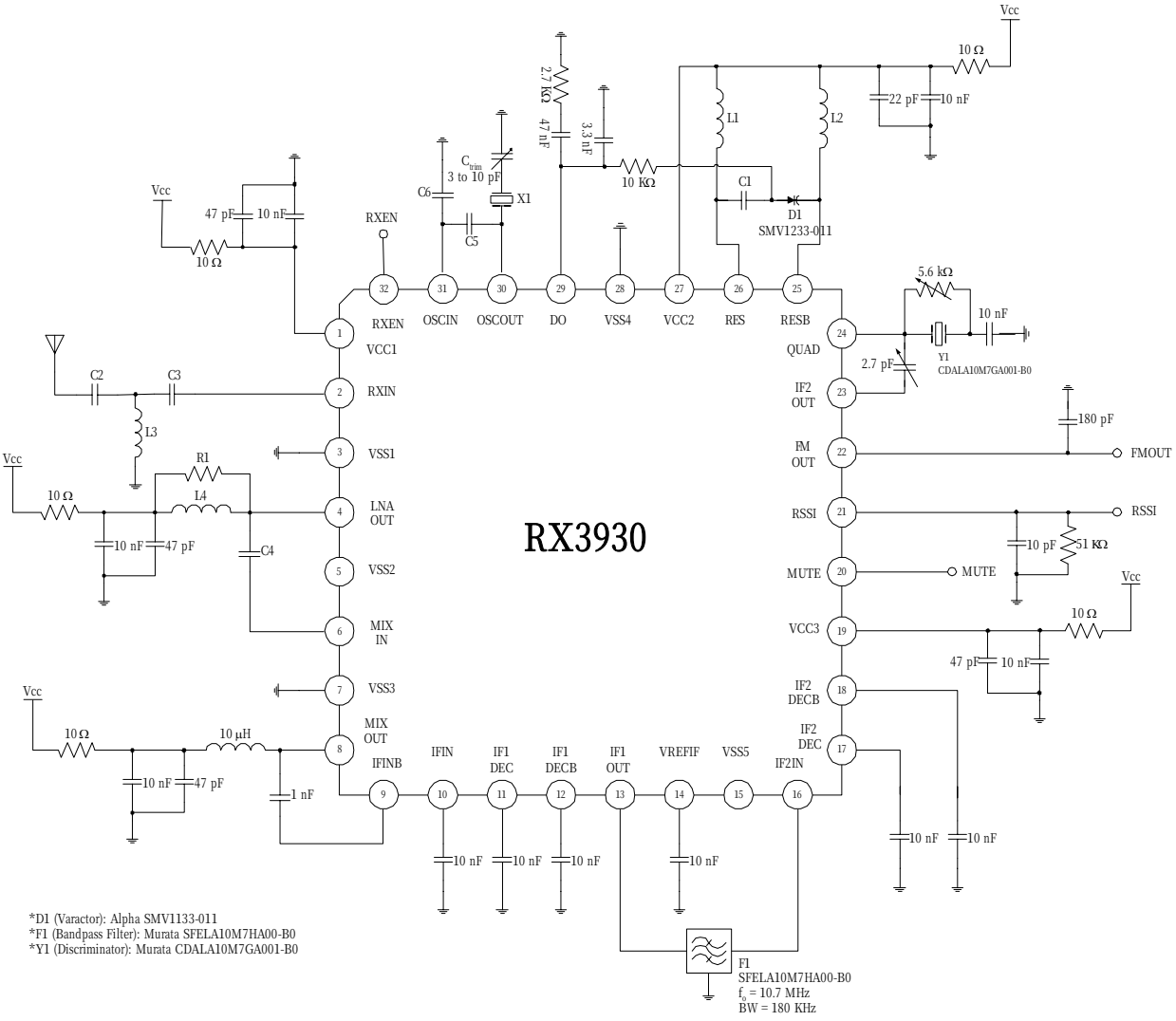
Electrical Characteristics

(V_{CC1}, V_{CC2}, V_{CC3} = 2.4 to 5.0 V, V_{SS} = 0 V, RXEN = high, T_A = –10 to 60 °C, f_{RF} = 915 MHz unless otherwise noted)

Parameter	Symbol	Condition	Value			Unit
			min.	typ.	max.	
Power supply						
VCC1 supply voltage	V_{CC1}		2.4	3.6	5.0	V
VCC2 supply voltage	V_{CC2}		2.4	3.6	5.0	V
VCC3 supply voltage	V_{CC3}		2.4	3.6	5.0	V
Total dc current (normal operation)	I_{DC}			7.5	9	mA
Total dc current (stand-by mode)	$I_{standby}$	RXEN = low			10	µA
LNA						
Power gain	G_{LNA}	Matched to 50 Ω		12		dB
Noise figure	NF_{LNA}	Depends on the matching network		3.5		dB
Input third-order intermodulation intercept point	$IIP3_{LNA}$			–14		dBm
Mixer						
Conversion power gain	G_C	Matched to 50 Ω		8		dB
Noise figure (SSB)	NF_{MIX}	Depends on the matching network		13		dB
Input third-order intermodulation intercept point	$IIP3_{MIX}$			–7.5		dBm

Parameter	Symbol	Condition	Value			Unit
			min.	typ.	max.	
VCO						
Frequency range		External varactor	300		1000	MHz
PLL						
N-divider ratio				64		
Reference frequency	f_{REF}				17	MHz
Charge pump current	I_{CP}		–40		40	µA
Phase Noise	PN_{VCO}	at 10 KHz offset		–74		dBc/Hz
		at 100 KHz offset		–95		dBc/Hz
Lock Time	τ_{lock}	PLL's lock time is set by the bandwidth of the external loop filter		5		ms
IF amplifier						
Frequency range			0.1	10.7	30	MHz
Input impedance	$Z_{in,IF}$			330		Ω
Output impedance	$Z_{out,IF}$			330		Ω
Limiter						
Frequency range			0.1	10.7	25	MHz
Input impedance	$Z_{in,IF}$			330		Ω
Output impedance	$Z_{out,IF}$			1K		Ω
RSSI						
RSSI dynamic range				70		dB
RSSI dc output range		R_{load} = 51 KΩ	0.5		2.5	V
FM/FSK Demodulator						
Demodulated output level (audio)	V_{OD}			70		mV_{rms}
FSK output duty ratio			40	50	60	%

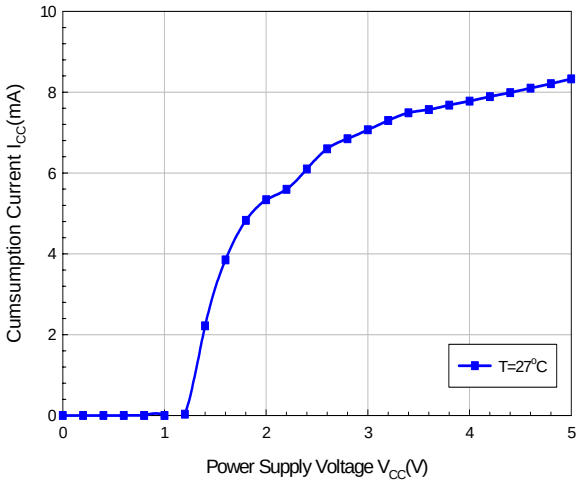
Application Circuit



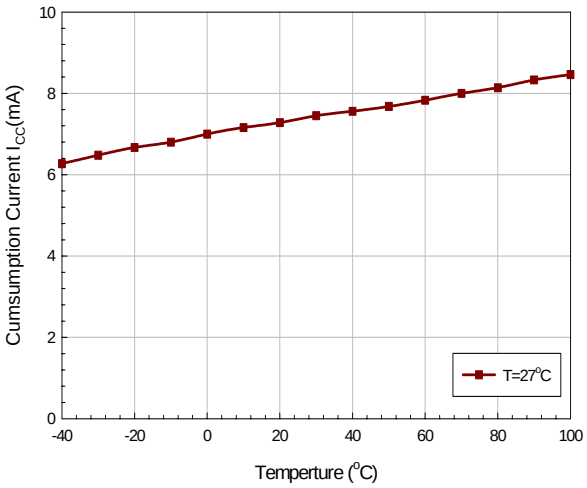
Frequency	L1,L2	C1	C2	C3	L3	L4	C4	R1	C5,C6	X1 (MHz)
905 MHz	3.9 nH	3.9 pF	3.3 pF	18 pF	6.8 nH	12 nH	4.7 pF	—	100 pF	14.31818
868 MHz	4.7 nH	2.2 pF	3.9 pF	22 pF	10 nH	12 nH	6.8 pF	—	100 pF	13.41050
434 MHz	18 nH	4.7 pF	2.2 pF	100 pF	27 nH	33 nH	10 pF	180	100 pF	6.612813
315 MHz	27 nH	10 pF	3.9 pF	100 pF	47 nH	47 nH	10 pF	—	100 pF	4.7546875

Measurement Results

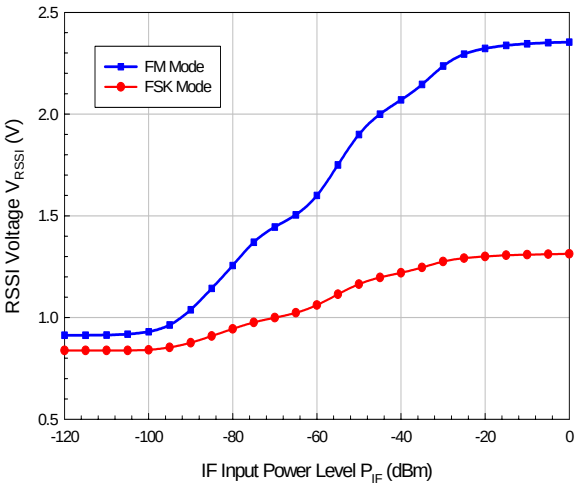
Consumption Current versus Supply Voltage



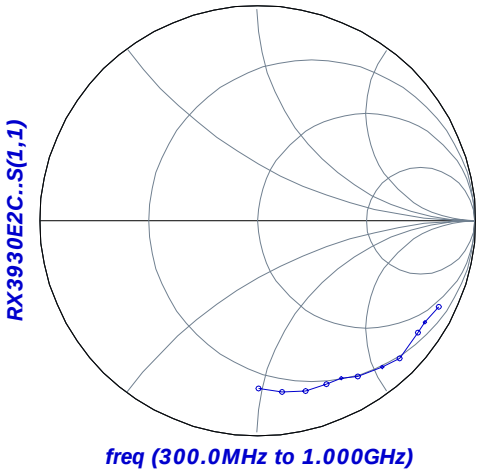
Consumption Current versus Temperture



RSSI Characteristic



LNA Input Impedance



Revision History

Date	Version Number	Author	Comments
6/11/2003	NC	Ivan N. Kao	Most up-to-date document
6/12/2003	B1	E. Lin	Many grammatical and style corrections. Globally changed font to Times New Roman.
8/14/2003	B2	Ivan N. Kao	Add the Smith chart of the LNA input impedance.