# FS8308 Low Power PLL Frequency Synthesizer IC

***Advance Information***



## Description

The FS8308 is a serial data input, phase-locked loop IC with programmable input and reference frequency dividers. When combined with a VCO, this IC becomes the core of a very low power frequency synthesizer well-suited for mobile communication applications, e.x. paging systems and family radio service (FRS). There are some features implemented in this IC, including an 18-bit programmable input frequency divider, a terminal for reference oscillator buffer output, as well as stand-by control through programming, and etc. Details are listed in the following.

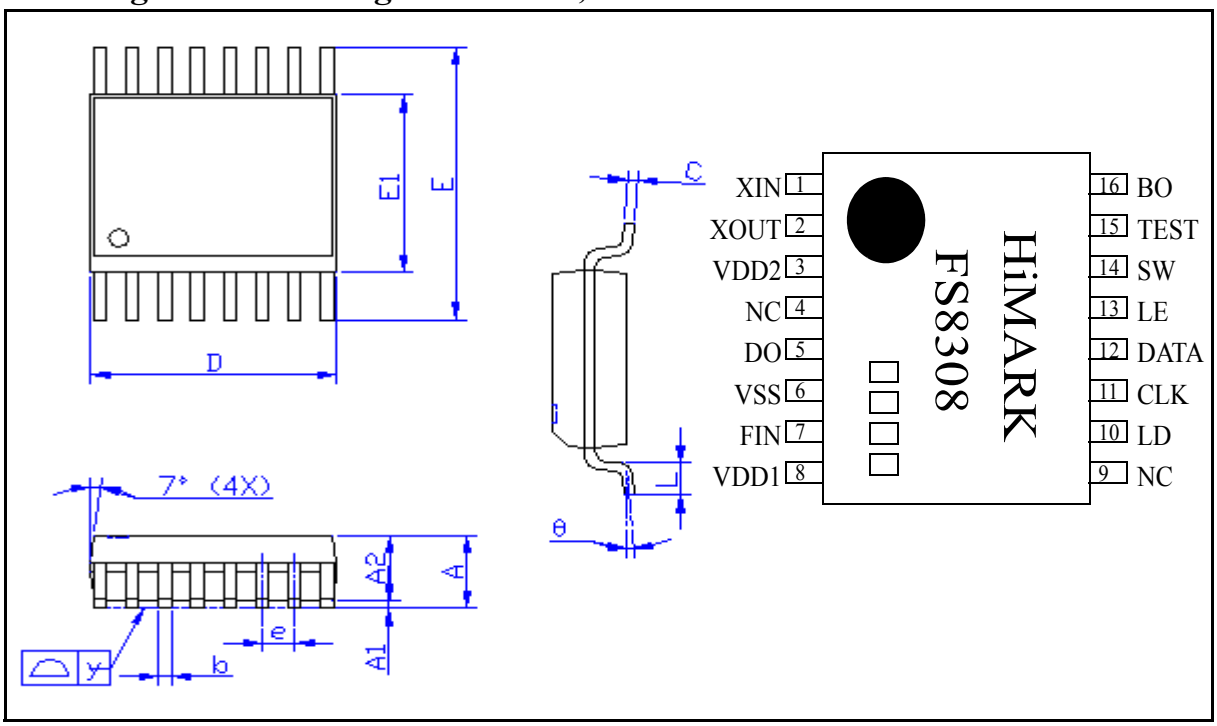
## Features

- Up to 40 MHz external crystal oscillator reference frequency under normal condition
- Low current consumption ($I_{DD,total}$ typically 1.2 mA at $f_{FIN}$ = 500 MHz and $V_{DD1}$ = 1.0 V)
- With Schmitt trigger added for noise-immune programming input
- 18-bit programmable input frequency divider (including a ÷ 64/65 prescaler) with divide ratio range from 4032 to 262143
- 13-bit programmable reference frequency divider (including a ÷ 8 prescaler) with divide ratio range from 40 to 65528
- Optional lock detector output (*LD*, $f_R/2$, $f_V/2$)
- Charge pump output for passive low-pass filter
- Wide tuning range of charge pump output for external VCO ($V_{SS}$+*0.5 to* $V_{DD2}$-*0.5*)
- Switchover terminal for constant of loop filter or general open drain output
- Reference oscillator buffer output
- Programmable stand-by control
- TSSOP 16L package (0.65mm pitch)

## Applications

- Pager
- Family radio service (FRS)
- Wireless communication system

## Package and Pin Assignment: 16L, TSSOP



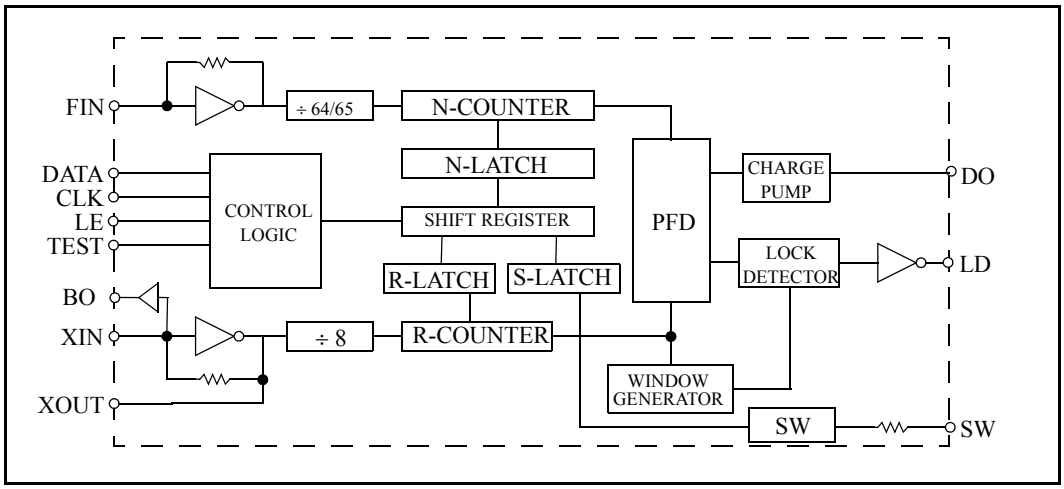

| Symbols | Dimensions in mm | | | Dimensions in inch | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | --- | --- | 1.20 | --- | --- | 0.048 |
| A1 | 0.05 | --- | 0.15 | 0.002 | --- | 0.006 |
| A2 | 0.80 | 1.00 | 1.05 | 0.031 | 0.039 | 0.041 |
| b | 0.19 | --- | 0.30 | 0.007 | --- | 0.012 |
| C | 0.09 | --- | 0.20 | 0.004 | --- | 0.008 |
| D | 4.90 | 5.00 | 5.10 | 0.193 | 0.197 | 0.201 |
| E | --- | 6.40 | --- | --- | 0.252 | --- |
| E1 | 4.30 | 4.40 | 4.50 | 0.169 | 0.173 | 0.177 |
| e | --- | 0.65 | --- | --- | 0.026 | --- |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| y | --- | --- | 0.10 | --- | --- | 0.004 |
| θ | 0° | --- | 8° | 0° | --- | 8° |

Note: Tolerance ± 0.1mm unless otherwise specified

## Pin Descriptions

| Number | Name | I/O | Description |
|---|---|---|---|
| 1 | XIN | I | Reference crystal oscillator or external clock input with internally biased amplifier (any external input to XIN must be ac-coupled) |
| 2 | XOUT | O | Reference crystal oscillator or external clock output |
| 3 | VDD2 | POWER | Nominal 3.0 V supply voltage |
| 4 | NC | NC | No connection |
| 5 | DO | O | Single-ended charge pump output for passive low-pass filter |
| 6 | VSS | GND | Ground |
| 7 | FIN | I | VCO frequency input with internally biased input amplifier (any external input to FIN must be ac-coupled) |
| 8 | VDD1 | POWER | Nominal 1.0 V supply voltage |
| 9 | NC | NC | No connection |
| 10 | LD | O | Lock detector output (high when PLL is locked) |
| 11 | CLK | I | Shift register clock input |
| 12 | DATA | I | Serial data input |
| 13 | LE | I | Latch enable input |
| 14 | SW | O | Switchover terminal for constant of loop filter or a general open drain output |
| 15 | TEST | I | Test mode control input with internal pull-down resistor |
| 16 | BO | O | Terminal of reference crystal oscillator buffer output |

## Block Diagram



## Absolute Maximum Ratings

$V_{SS}$ = 0 V

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage | $V_{DD1}$ | $V_{SS}$ – 0.3 to $V_{SS}$ + 2.0 | V |
| | $V_{DD2}$ | $V_{SS}$ – 0.3 to $V_{SS}$ + 6.0 | V |
| Input voltage range | $V_{FIN}$ | $V_{SS}$ – 0.3 to $V_{DD}$ + 0.3 | V |
| Operating temperature range | $T_{PS}$ | –30 to 60 | °C |
| Storage temperature range | $T_{STG}$ | –40 to 125 | °C |
| Soldering temperature range | $T_{SLD}$ | 255 | °C |
| Soldering time range | $t_{SLD}$ | 10 | s |

## Recommended Operating Conditions

$V_{SS}$ = 0 V

| Parameter | Symbol | Value | | | Unit |
|---|---|---|---|---|---|
| | | min. | typ. | max. | |
| Supply voltage range | $V_{DD1}$ | 0.95 | 1.0 | 2.0 | V |
| | $V_{DD2}$ | 2.4 | 3.0 | 3.6 | V |
| Operating temperature | $T_A$ | –30 | 25 | 60 | °C |

## Electrical Characteristics

($V_{DD1}$ = 0.95 to 2.0 V, $V_{DD2}$ = 2.4 to 3.6 V, $V_{SS}$ = 0 V, $T_A$ = 0 to 60°C unless otherwise noted)

| Parameter | Symbol | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | min. | typ. | max. | |
| Current consumption | $I_{DD,total}$ | $V_{DD1}$ = 1.0 V<br>$f_{FIN}$ = 500 MHz<br>$f_{XIN}$ =24 MHz | | 1.2 | 1.5 | mA |
| Standby current consumption | $I_{DD,standby}$ | PS="H" | | | 10 | µA |
| FIN operating frequency range | $f_{FIN}$ | $P_{FIN}$ = -15dBm<br>$V_{DD1}$ = 1.0 V, PS="L" | 20 | | 500 | MHz |
| XIN operating frequency range | $f_{XIN}$ | $V_{DD1}$ = 1.0 V | 7 | | 40 | MHz |
| FIN input voltage swing | $P_{FIN}$ | | -15 | | | dBm |
| XIN input voltage swing | $V_{XIN}$ | | 0.3 | | | $V_{pk-pk}$ |
| CLK, DATA, LE logic LOW input voltage | $V_{IL}$ | | | | 0.3 | V |
| CLK, DATA, LE logic HIGH input voltage | $V_{IH}$ | | $V_{DD}$-0.3 | | | V |
| XIN logic LOW input current | $I_{IL,XIN}$ | $V_{IL}$ = 0 V | | | 10 | µA |
| XIN logic HIGH input current | $I_{IH,XIN}$ | $V_{IH}$ = $V_{DD1}$ | | | 10 | µA |
| FIN logic LOW input current | $I_{IL,FIN}$ | $V_{IL}$ = 0 V | | | 60 | µA |
| FIN logic HIGH input current | $I_{IH,FIN}$ | $V_{IH}$ = $V_{DD1}$ | | | 60 | µA |
| Charge Pump Drive Current | $I_{DO}$ | $V_{DD2}$ = 3.0V, $V_{DO}$ = 1.5V | | 1.0 | | mA |
| Charge Pump Sink Current | $I_{DO}$ | $V_{DD2}$ = 3.0V, $V_{DO}$ = 1.5V | | 1.0 | | mA |
| LD, FV, FR logic LOW output current | $I_{OL}$ | $V_{OL}$ = 0.4 V | 0.1 | | | mA |
| LD, FV, FR logic HIGH output current | $I_{OH}$ | $V_{OH}$ = $V_{DD2}$ – 0.4 V | 0.1 | | | mA |
| SW logic LOW output current | $I_{SW,OFF}$ | SW = 'L'<br>$V_{SW}$ = $V_{DD2}$ = 3.0V | | | 10 | µA |
| SW logic HIGH output current | $I_{SW,ON}$ | SW = 'H'<br>$V_{SW}$ = $V_{DD2}$ = 3.0V | | 2.8 | | mA |
| DATA to CLK setup time | $t_{SU1}$ | | 2 | | | µs |
| CLK to LE setup time | $t_{SU2}$ | | 2 | | | µs |
| Hold time | $t_{HOLD}$ | | 2 | | | µs |

## Functional Description

### Programmable Input Frequency Divider

The VCO input to the FIN pin is divided by the programmable divider and then internally output to the phase/frequency detector (PFD) as $f_V$. The programmable input frequency divider consists of a ÷ 64/65 ($P$/$P$+1) dual-modulus prescaler in prior to a 18-bit ($N$) counter, which is further comprised of a 6-bit swallow ($A$) counter, and a 12-bit main ($B$) counter. The total divide ratio, $N$, is related to values for $P$, $A$, and $B$ through the relation

$$N = (P+1) \times A + P \times (B-A) = P \times B + A,$$

with $B \geq A$. The minimum available programmable divisor for continuous counting is given by $P \times (P-1) = 64 \times 63 = 4032$, and the valid total divide ratio range for the input divider is $M = 4032$ to $262143$.

Take N=10000 for example, since P=64 and hence that B=156 and A=16. Therefore, the binary codes of B and A should be 0000 1001 1100 and 010000, respectively. An alternative approach is to translate the decimal N into binary code directly. And then just take the last 6-bit as A and the remaining 12-bit as B. By far the binary code of N=10000 is 00 0010 0111 0001 0000. One can get the same result as the former method.

### Programmable Reference Frequency Divider

The crystal oscillator output is divided by the programmable divider and then internally output to the PFD as $f_R$. The programmable reference frequency divider consists of a fixed ÷ 8 ($S$) prescaler and a 13-bit reference ($R$) counter. The total divide ratio, $T$, is related to values for $S$ and $R$ through the relation

$$T = S \times R = 8 \times R.$$

The usable divisior range of the reference counter is $R = 5$ to $8191$ and therefore, the valid total divide ratio range for the reference divider is $T = 40$ to $65528$ (in steps of 8.)

### Serial Input Data Format

The divsors of the input and reference dividers are input using a 20-bit serial interface consisting of separate clock (CLK), data (DATA), and latch enable (LE) lines. The format of the serial data is shown in Fig. 1. The data on the DATA line is written to the shift register on the rising edge of the CLK signal and is input with MSB first. The last two bits are recognized as the latch select control bits. Data on the DATA line should be changed on the falling edge of CLK, and LE should be held low while data is being written to the shift register. Data is transferred from the shift register to either one of the frequency divider latches or the optional control latch when LE is set high. When the latch select control bits are set high-low or low-low, data is loaded to the 18-bit *N*-counter latch, and when the latch select control bits are set high-high, the 2 MSBs are ignored, the next 13 data bits are loaded to the 13-bit *R*-counter latch and the remaining 3 LSBs are used to control testing modes and should be set as follows for normal operation: R14 = high, R15 = low, R16 = low. To disable LD output (*i.e.* set LD low), R14 should be set low. When the latch select control bits are set low-high, the 2 MSBs are recognized as PS and SW, which are used as stand-by control and open drain output control, respectively. The detail of two control bits setting is summarized in Table 1. In normal work condition, PS is set to low. When PS is programmed to high, it will enter stand-by mode.

Serial input data timing waveforms are shown in Fig. 2.

Fig. 1 – Serial input data format

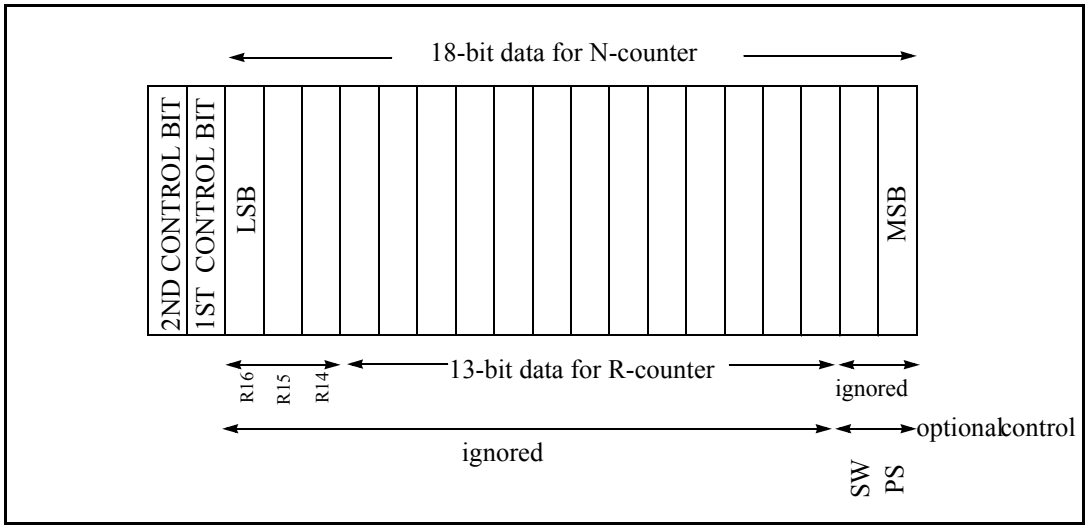
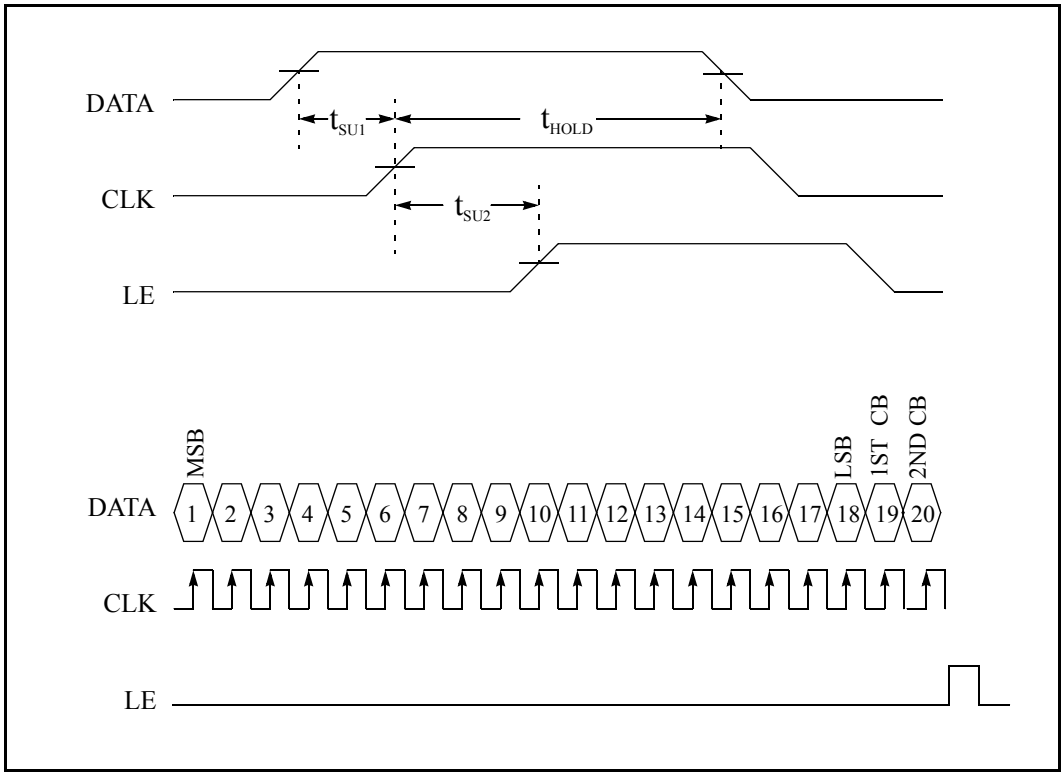



**Table 1: Control Bit Setting**

| 1st CB | 2nd CB | Fetching Target of Serial Data Input |
|---|---|---|
| X | 0 | N-counter |
| 0 | 1 | PS and SW |
| 1 | 1 | R-counter |

Fig. 2 – Serial input data timing waveforms



**Phase/Frequency Detector (PFD)**

The PFD compares an internal input frequency divider output signal, $f_V$, with an internal reference frequency divider output signal, $f_R$, and generates an error signal, DO, which is proportional to the phase error between $f_V$ and $f_R$. The DO output is intended for use with a passive filter as shown in Fig. 2.

**Lock Detector (LD)**

When phase comparator detects phase difference, LD terminal outputs "L". When phase comparator locks, LD terminal outputs "H". On standby, outputs "H". The criteria for lock condition is that the phase difference between $f_V$ and $f_R$ is less than *2/xin* and continues for more than three consecutive times.

The input/output waveforms for the PFD and LD are shown in Fig. 3.

Fig. 2 – Passive low-pass filter circuit

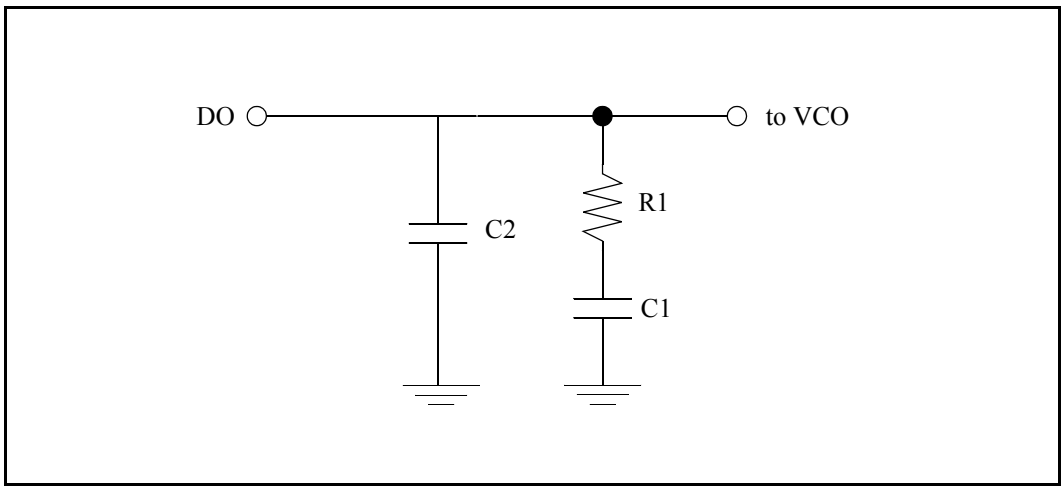
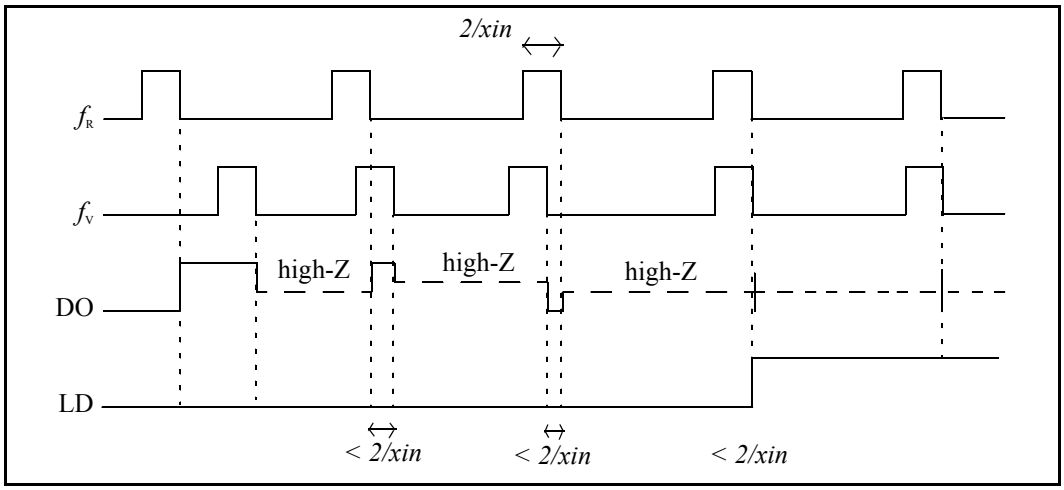



Fig. 3 – PFD input/output waveforms



### Stand-by Mode

The stand-by mode for the PLL is entered by programming the PS bit to high. In the stand-by mode, the XIN and FIN amplifiers, *N*-counter, and *R*-counter are stopped, as well as the internal current bias for charge pump block, the *N*- and *R*-counters are also reset, and the DO and DB outputs are set to the high impedance state. As long as voltage is supplied to $V_{DD2}$, data loaded to the latches is kept. To exit from stand-by mode to normal operation, the PS bit must be programmed to low.

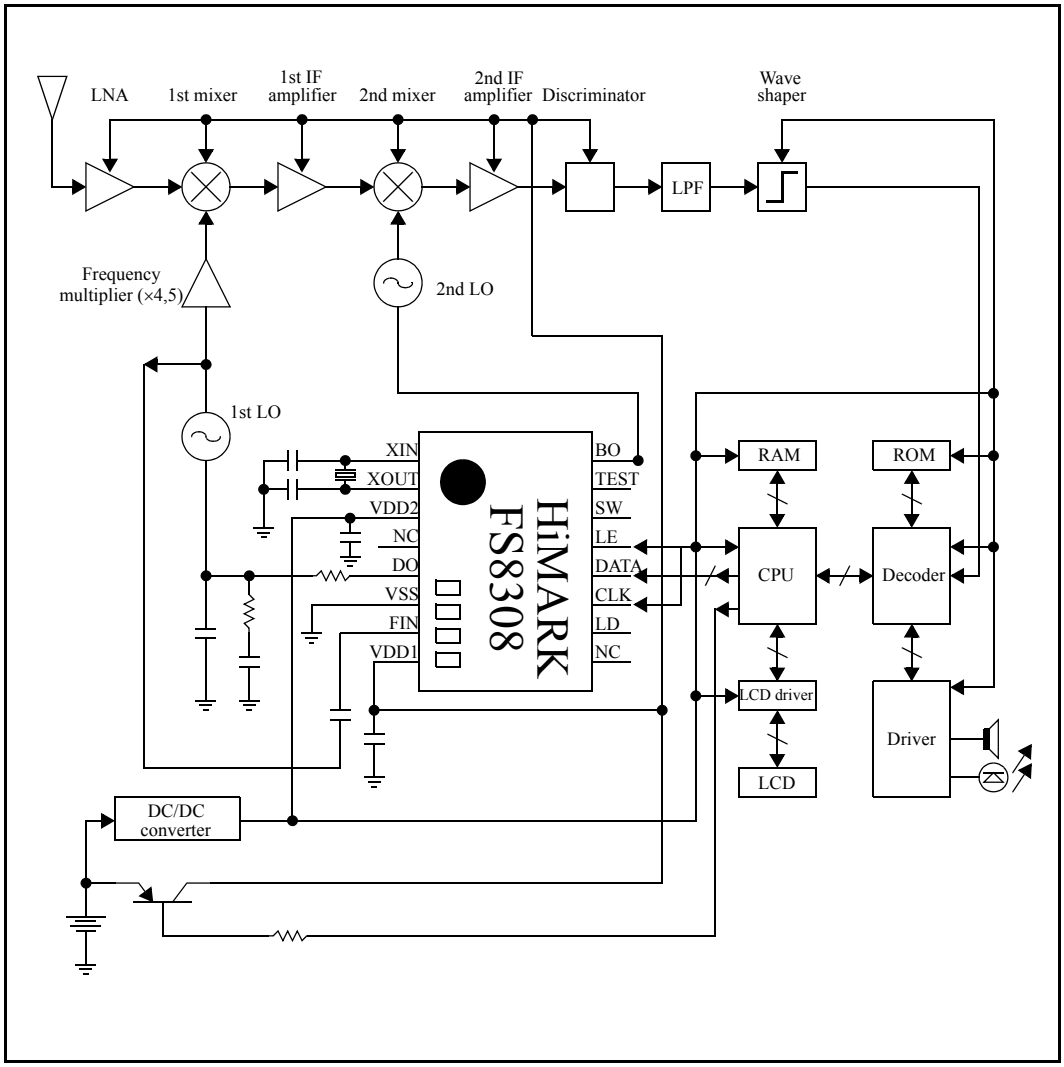
### Reference Crystal Oscillator Buffer Output (BO)

This IC provides a reference crystal oscillator buffer output intended to be used as a crystal local oscillator to a 2nd mixer. The terminal is represented as BO. For cases to enhance the buffer output swing, increasing $V_{DD1}$ will be an efficient way.

### Filter Switch Control (SW)

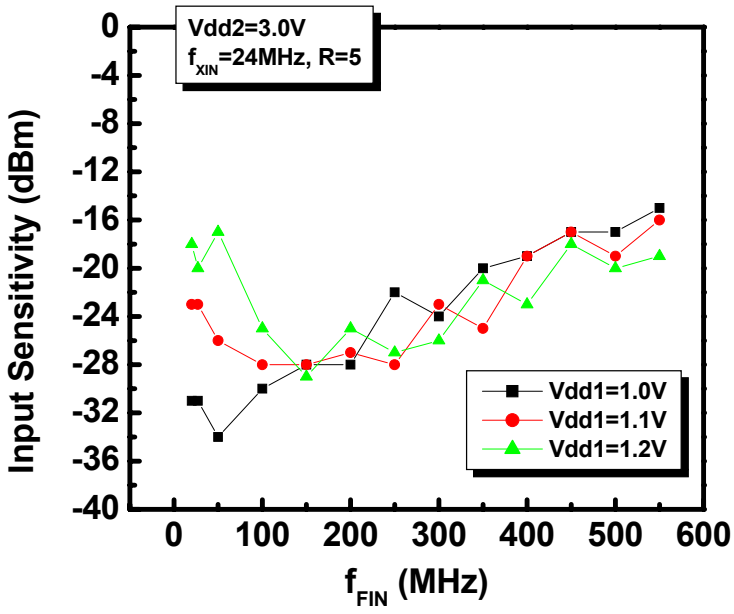
Control of SW terminal by "SW" bit. This terminal is for switching time-constant of loop filter. Output type of this terminal is open drain output. When constant of loop filter doesn't change by this switch, general open drain output is available. Note that there is an internal 200Ω resistor connected between and drain terminal and output pin.

## Application Circuit

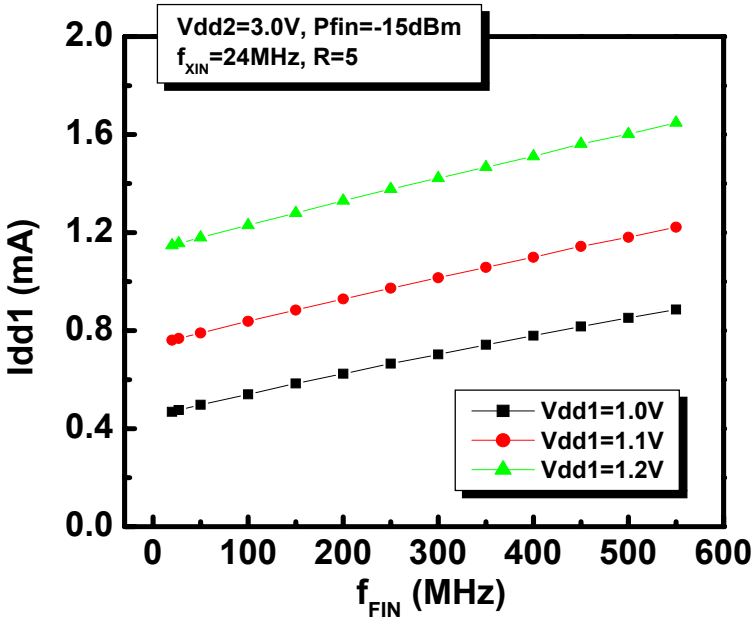


## Typical Characteristics

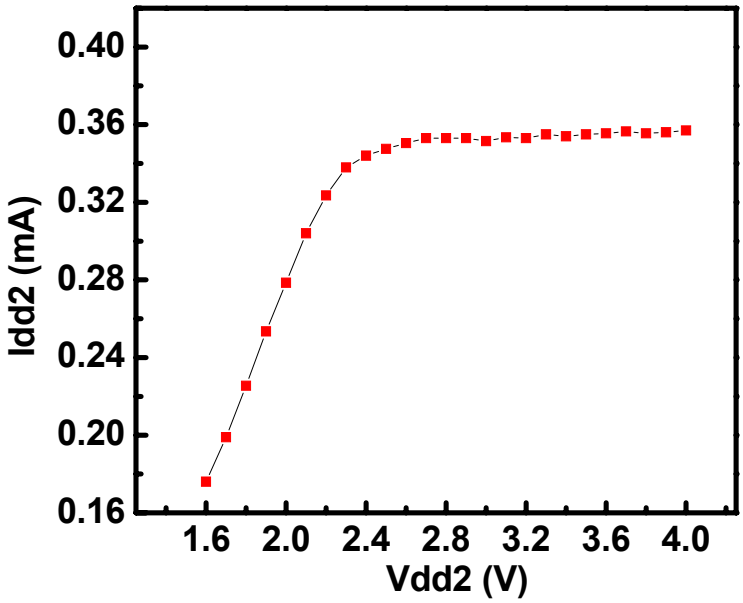
### FIN Input Sensitivity vs. Input Frequency



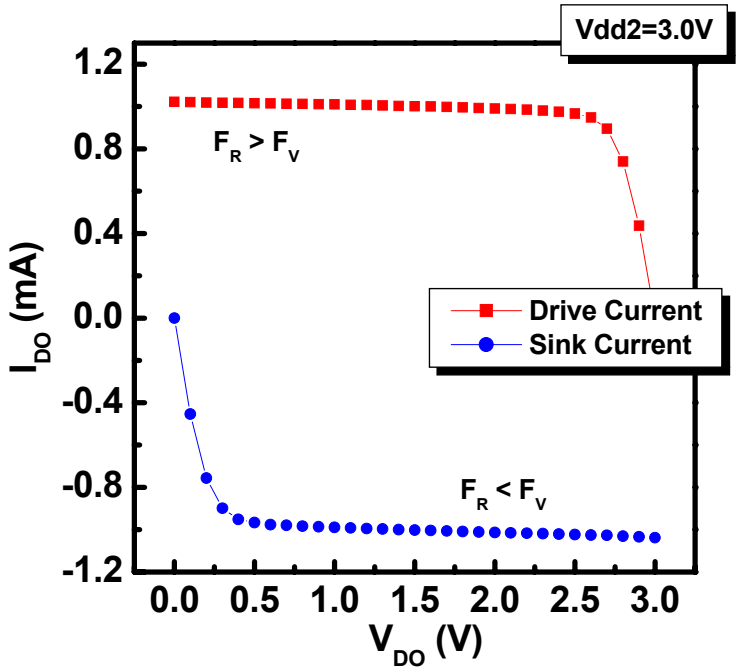
**Current Consumption of Idd1 vs. Operating Frequency**



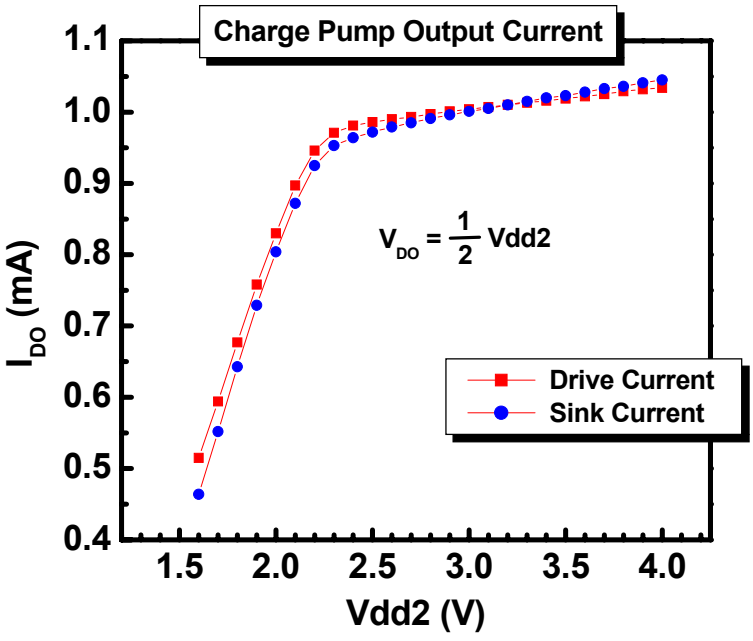

**Current Consumption of Idd2 vs. Supply Voltage Vdd2**



**Charge Pump Output Characteristics**

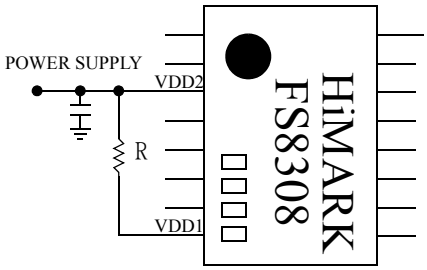



**Charge Pump Output Current vs. Power Supply Voltage**



## Single Voltage Operation

This IC requires two separate power supplies to operate. If only one voltage source is available, ex. use battery to serve as power source, the user can apply the configuration as shown in the following which is referred to as single voltage operation.




Since there is only one voltage source provided in the so-called single voltage configuration, which is directly connected to $V_{dd2}$, one needs to choose a reasonable R value to set $V_{dd1}$ to operate within the safe region, whose requirement is $V_{dd1} > 0.95V$. Keep in mind that the lower $V_{dd1}$ is, the less current this IC will consume, but the poorer crystal buffer output it drives. In order to balance the trade-off between the current consumption and crystal buffer driving capability, $V_{dd1}$ is suggested to be about 1.1V. $V_{dd1}$ vs. $V_{dd2}$ for various R at *fin=470MHz* is plotted in the following figure. Note that although smaller resistor R makes this IC consume more current, the reward is with wider power supply input range. Typical value of R is recommended to be around *1.6KΩ*..

**Single Voltage Characteristic: Vdd1 vs. Vdd2 for Various R**