ISD61S00 ChipCorder
Telephony Feature Chip

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1. GENERAL DESCRIPTION

The ISD61S00 is a feature chip for the security and telephony industry. The device incorporates audio storage with a powerful macro scripting ability to facilitate audio prompting in a multi-language environment and simple address-free recording and playback. It utilizes external serial flash memory for audio data storage. In addition, the device includes circuitry to perform telephony based data communications including DTMF detection and generation, FSK modem functions from 75-1200 baud, CAS and CPT (Call Progress Tone) detection and ring detection. The audio path of the device is designed to interface to both the air side and line side of a PSTN system. The air side includes a flexible microphone interface incorporating a bias generator and gain control and a differential analog output for driving a speaker or power amplifier. The line side incorporates a line driver to drive PSTN loads and two variable gain differential inputs. The audio path includes full and half-duplex acoustic and line echo cancellation to implement full and half-duplex speakerphone functions. The digital audio interface can be configured to I^2S or PCM mode for digital serial audio communication. Control, monitoring and device programming is perfomed via a SPI interface. The device package is LQFP-48L.

2. FEATURES

- External Memory:
  - The ISD61S00 supports the following flash:

Manufacturer	Winbond		Numonyx			MXIC
Family	25X	25Q	25P	25PX	25PE	25L / 25V
JEDEC ID	EF 30 1X	EF 40 1X	20 20 1X	20 71 1X	20 80 1X	C2 20 1X

  - The addressing ability of ISD61S00 is up to 128Mbit, which is 64-minute record/playback time based on 8kHz/4bit ADPCM.
- Fast pre-recording: Recording is limited by the write rate of the attached external flash.
- Operating voltage: 2.7-3.6V.
- Sampling frequency: Recording and playback sampling frequencies of 4, 5.3, 6.4, 8, 10.6, 12.8 and 16 kHz.
- Compression algorithm:
  - For record and playback:
  - ADPCM compression at 2, 3, 4 or 5 bits per sample.
  - µ-Law companding at 6, 7 or 8 bits per sample.
  - Differential µ-Law encoding at 6, 7 or 8 bits per sample.
  - PCM encoding at 8, 10 or 12 bits per sample.
- For pre-recorded audio playback (Voice prompts) additionally:
  - Enhanced ADPCM compression at 2, 3, 4 or 5 bits per sample.
  - Multi-Bit rate optimized compression. This allows best possible compression given a metric of SNR and background noise levels.
- Message Management:
  - Simple address free real-time recording.
  - Flexible Voice Prompt message management and Voice Macro scripting for pre-recorded messages.
- External serial flash memory interface: Support up to 128Mbit for audio and digital data storage, equivalent to 64 minutes based on 8khz 4bit ADPCM.
- Digital access to flash memory: Memory can be reserved on a 4Kbyte sector basis for use as

conventional digital memory by host.

- Telephony/Modem/Data Features at 8KHz CODEC sampling rate:
  - DTMF encoder with 20 digit dial string buffer.
  - DTMF detector.
  - FSK generation at 75/110/150/300/1200 baud for Bell 103, Bell 202, V.21 or V.23 modem standards. Transmit FIFO to reduce host interaction.
  - FSK detector at 75/110/150/300/1200 baud for Bell 103, Bell 202, V.21 or V.23 modem standards with receive FIFO.
  - Ring Detector.
  - Call Progress Tone (CPT) detector for detecting dial tones, busy tones etc.
  - CAS detector for caller ID type I, type II implementation.
  - Arbitrary dual tone generator.
  - Arbitrary tone detector.
- Acoustic Echo Cancellation (AEC), Line Echo Cancellation (LEC) and Automatic Gain Control (AGC) for on-chip speakerphone support.
- Up to 17 GPIO pins accessible through the SPI interface.
- Audio Input:
  - TI1 and TI2: Differential Analog inputs for PSTN interface (on-hook and off-hook).
  - MIC+/-: Analog interface to microphone.
- Audio Output:
  - PO: Differential Analog output for PSTN interface.
  - SPK: Differential output buffer for speaker driver.
- I/O:
  - SPI interface: MISO, MOSI, SCLK, SS for commands and digital audio data.
  - INT and R/B signal for signaling and flow control.
- Package: Green LQFP-48L
- Temperature: -40°C to 85°C

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3. PIN CONFIGURATION

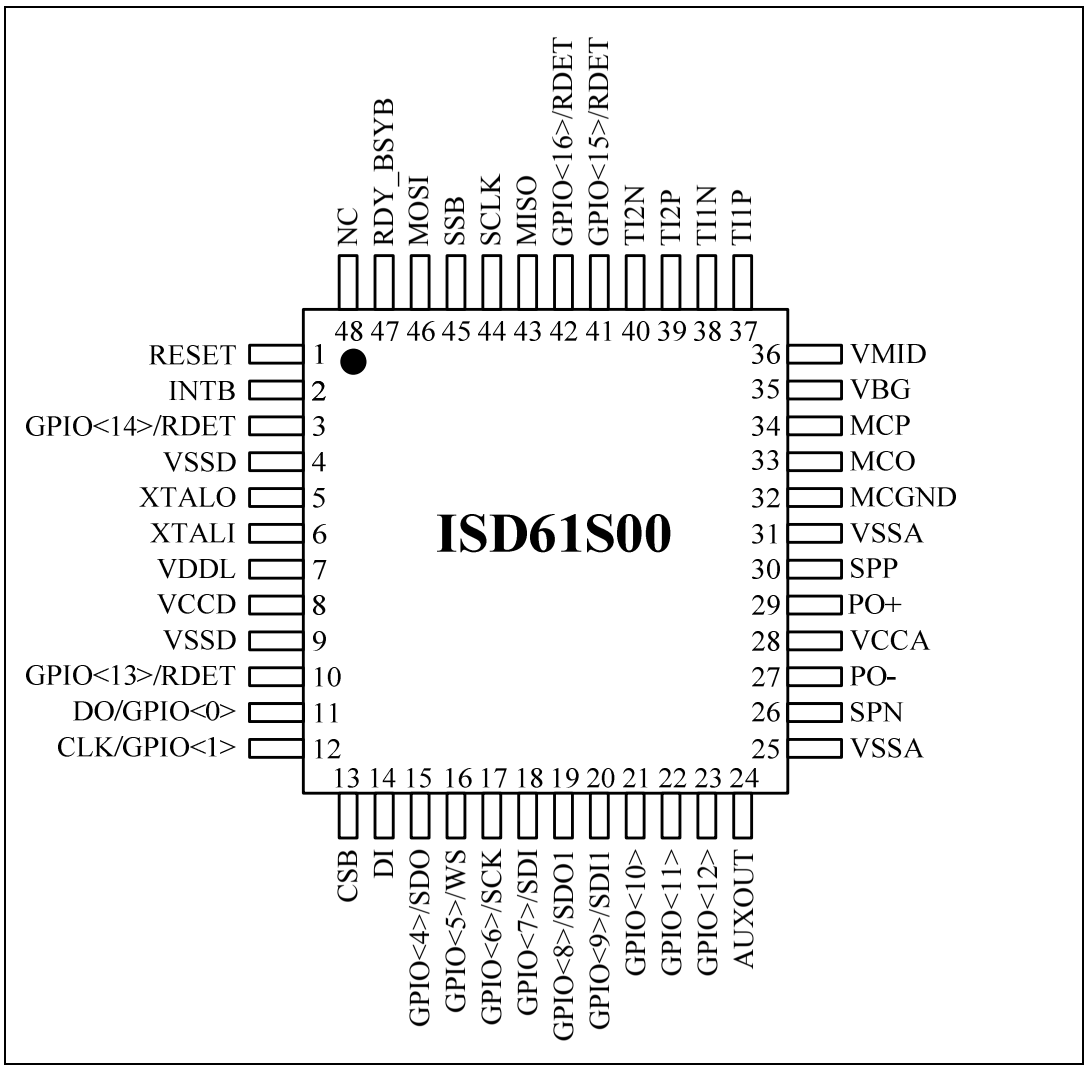


Figure 3-1 ISD61S00 48-Lead LQFP Pin Configuration.

4. PIN DESCRIPTION

Pin Number	Pin Name	I/O	Function	Drive
1	RESET	I	A 10ms high pulse (0V to VCC to 0V) will reset the chip	N/A
2	INTB	O	Active low interrupt request pin. This pin has an open drain output.	4/8mA
3	GPIO<14>/RDET	I/O*	General Purpose IO Pin or the Ring Detect input (RDET).	4/8mA
4	VSSD	G	Digital Ground.	N/A
5	XTALOUT	O	Crystal Interface output pin.	N/A
6	XTALIN	I	Crystal interface input pin. It can also be used to provide an external clock to the device.	N/A
7	VDDL	O	This pin has a nominal 1.8V output to supply the internal logic. A 2.2nF capacitor should be connected to this pin.	N/A
8	VCCD	P	Digital power supply pin	N/A
9	VSSD	G	Digital Ground.	N/A
10	GPIO<13>/RDET	I/O*	General Purpose IO Pin.	4/8mA
11	DO/GPIO<0>	I/O	Flash interface data out. Alternatively General Purpose IO Pin.	4/8mA
12	CLK/GPIO<1>	I/O	Flash interface clock. Alternatively General Purpose IO Pin.	4/8mA
13	CSB	O	Flash interface chip select bar.	4/8mA
14	DI	I	Flash interface data in.	4/8mA
15	GPIO<4>SDO	I/O*	General Purpose IO Pin. Serial Data Out for the I2S interface.	8/16mA
16	GPIO<5>/WS	I/O*	General Purpose IO Pin. Word Select (WS) output for the I2S Interface	8/16mA
17	GPIO<6>/SCK	I/O*	General Purpose IO Pin. Serial Clock output for the I2S Interface	8/16mA
18	GPIO<7>/SDI	I/O*	General Purpose IO Pin. Serial Data Input (SDI) input pin for the I2S Interface.	8/16mA
19	GPIO<8>/SDO1	I/O*	General Purpose IO Pin. Secondary Serial Data Out for the I2S interface.	4/8mA
20	GPIO<9>SDI1	I/O*	General Purpose IO Pin. Secondary Serial Data Input (SDI) input pin for the I2S Interface.	4/8mA

21	GPIO<10>	I/O*	General Purpose IO Pin.	4/8mA
22	GPIO<11>	I/O*	General Purpose IO Pin or the Ring Detect input (RDET).	4/8mA
23	GPIO<12>	I/O*	General Purpose IO Pin.	4/8mA
24	AUXOUT	O	Auxiliary output from PSTN or SPEAKER DAC.	N/A
25	VSSA	G	Analog Ground Pin	N/A
26	SPKN	O	Negative speaker driver output	N/A
27	PO-	O	Negative line driver output	N/A
28	VCCA	P	Analog Power Pin	N/A
29	PO+	O	Positive line driver output	N/A
30	SPKP	O	Positive speaker driver output	N/A
31	VSSA	G	Analog Ground Pin	N/A
32	MCGND	I	Analog ground pin for MIC. This pin should be connected to a quiet VSSA and used as the return for microphones connected to MCP.	N/A
33	MCO	I/O	MIC feedback signal	N/A
34	MCP	I	Positive MIC signal input.	N/A
35	VBG	I/O	Voltage reference, a 100nF capacitor should be connected to this pin.	N/A
36	VMID	I/O	Voltage reference, a 4.7uF capacitor should be connected to this pin.	N/A
37	TI1P	I	PSTN Line #1 positive input	N/A
38	TI1N	I	PSTN Line #1 negative input	N/A
39	TI2P	I	PSTN Line #2 positive input	N/A
40	TI2N	I	PSTN Line #2 negative input	N/A
41	GPIO<15>/RDET	I/O*	General Purpose IO Pin. Can be configured as Ring Detect (RDET) input.	4/8mA
42	GPIO<16>/RDET	I/O*	General Purpose IO Pin. Can be configured as Ring Detect (RDET) input.	4/8mA
43	MISO	O	SPI slave serial data output from the ISD61S00 to the host. This pin is tri-stated when SSB=1.	4/8mA
44	SCLK	I	SPI serial Clock input to the ISD61S00 from the host.	N/A
45	SSB	I	Slave select input to the ISD61S00 from the host	N/A
46	MOSI	I	SPI slave serial data input to the ISD61S00 from the host.	4/8mA

47	RDY/BSYB	O	This pin is at VCCD when the chip is ready to accept a new command/data and is at VSSD when device is busy.	4/8mA
48	NC	N/A	No Connect	N/A

* Default state for digital I/O pins is input with internal pull-up [38Kohms to 83Kohms] to VCCD supply

5. BLOCK DIAGRAM

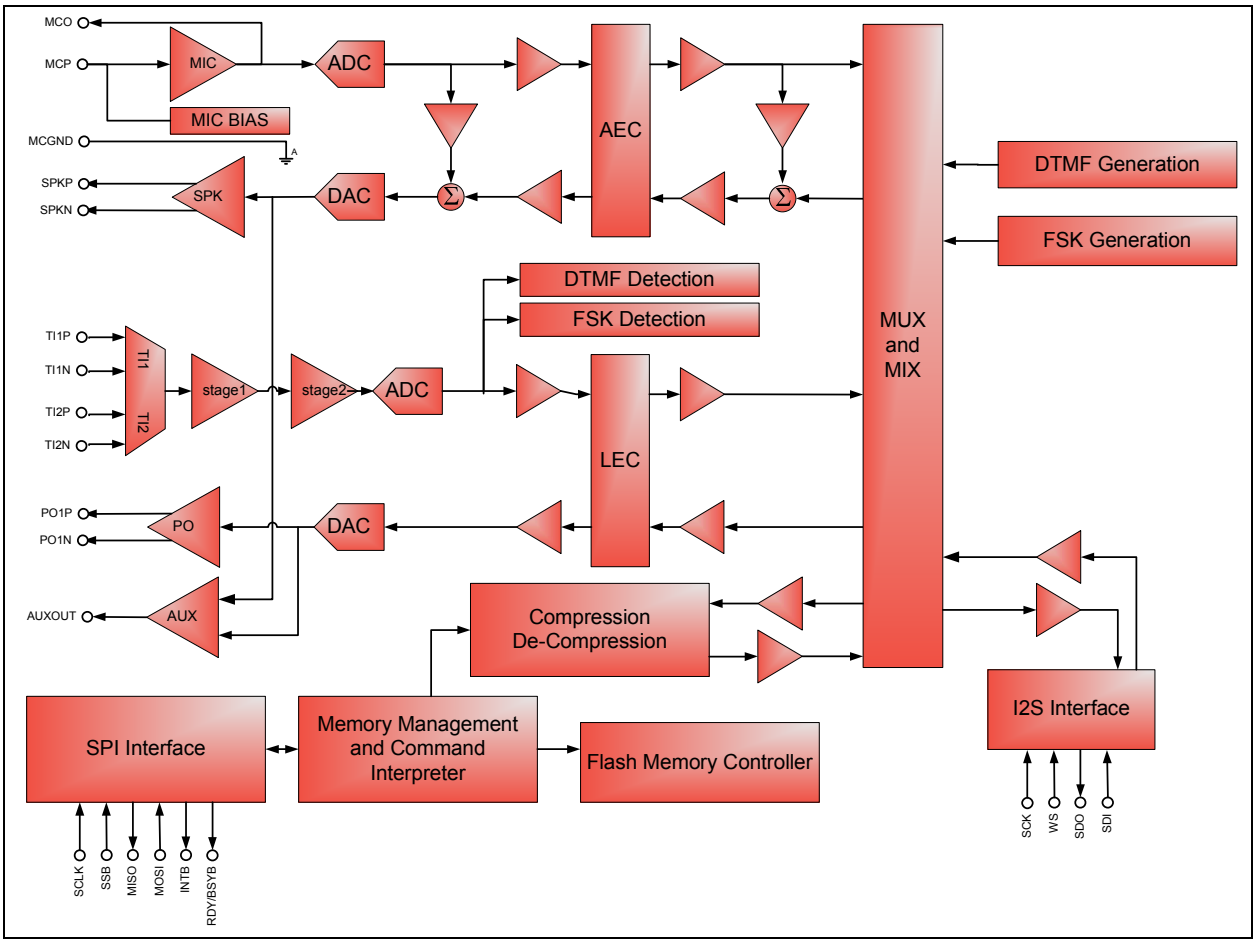


Figure 5-1 ISD61S00 Block Diagram

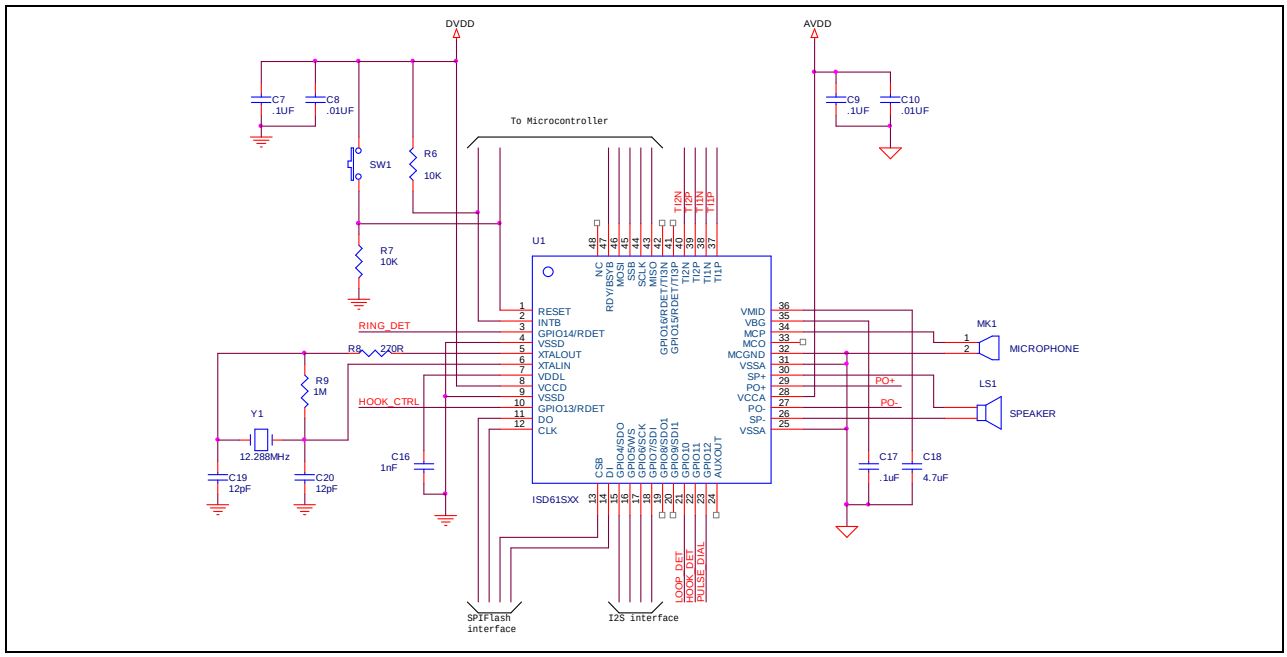
6. APPLICATION REFERENCE SCHEMATICS

The bottom part of Figure 6-1 shows a reference design for a PSTN interface to the ISD61S00. Two analog signal paths are provided for monitoring audio signals on TIP and RING. The Type 1 CID is for monitoring TIP and RING in an on-hook state to receive CID information. The Type II CID and speech interface is through a balanced configuration along with the output driver for use when the signal path is off-hook. Also included are optional circuits for line detection, ring detection and pulse dialing.

The Figure 6-2 illustrates a reference design for connecting the ISD61S00 to an integrated silicon DAA.

6.1 PCB Layout Guidelines

To gain maximum performance from the ISD61S00 it is important to provide clean analog supplies to the device. Separate Vcca and Vssa returns to the board low impedance point are essential for noise isolation. Good quality low ESR decoupliling capacitors on the supplies along with filter capacitors on Vbg and Vmid are also important for optimal performance. Care in shielding MIC connections from noise sources is imperative, these connections should be as short as possible and shielded with Vssa. The speaker and PO connections carry high currents and should be made as wide as possible. The TI inputs are differential and should be run as a pair and shielded with Vsaa. The flash SPI bus is a high speed serial bus and connections should be routed to the flash device in equal and short traces.



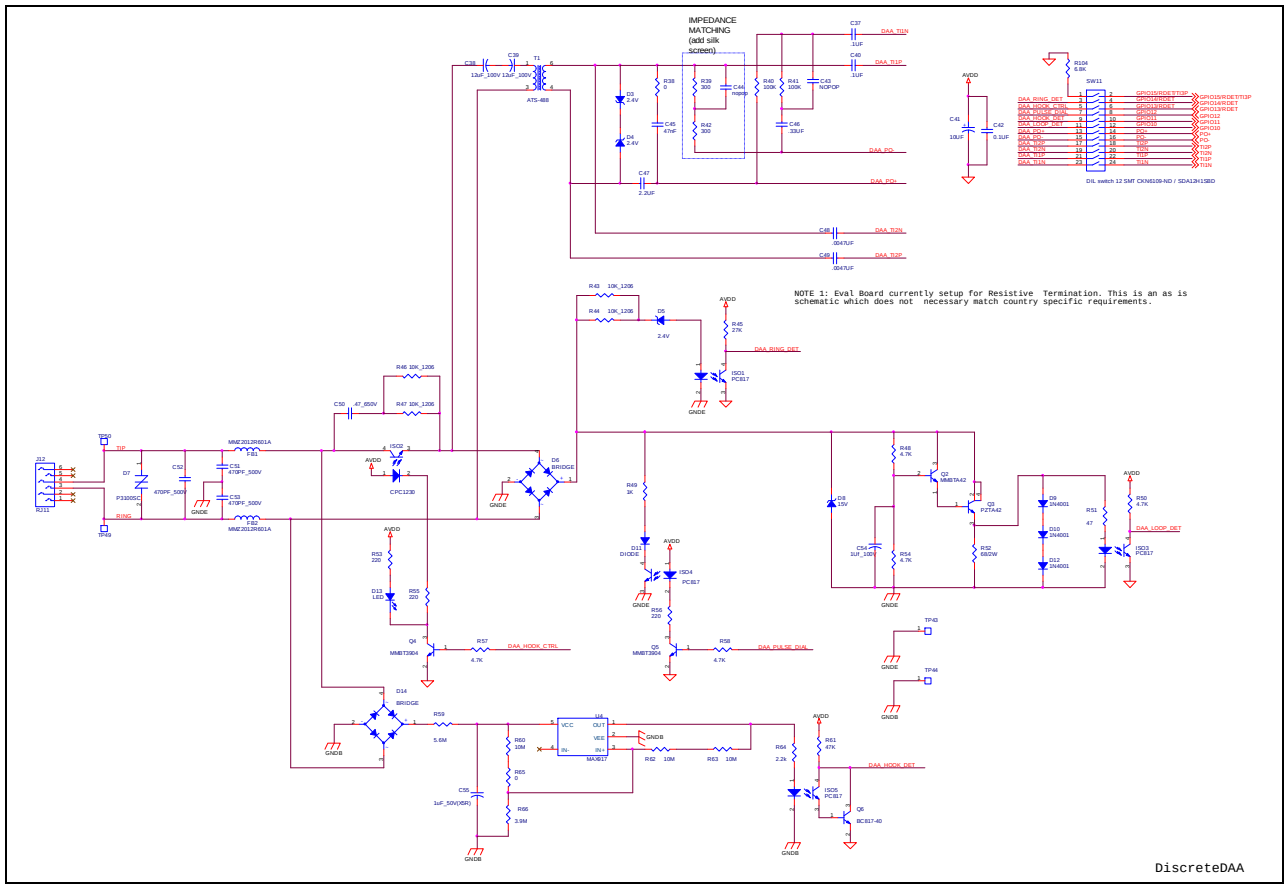
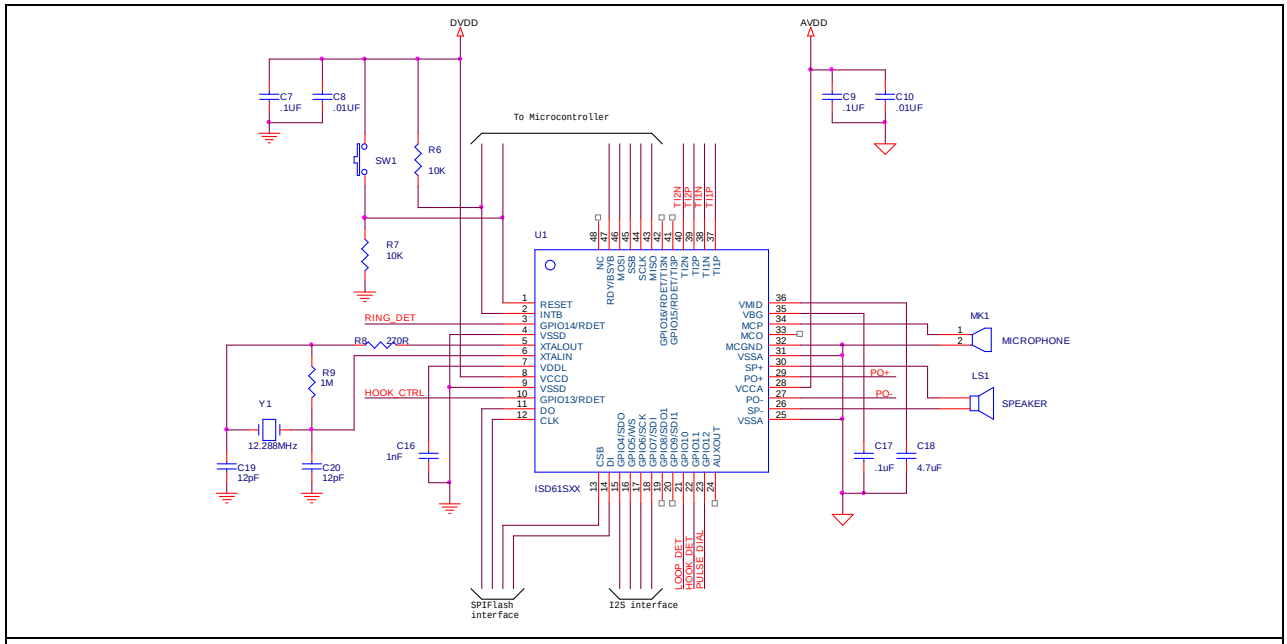
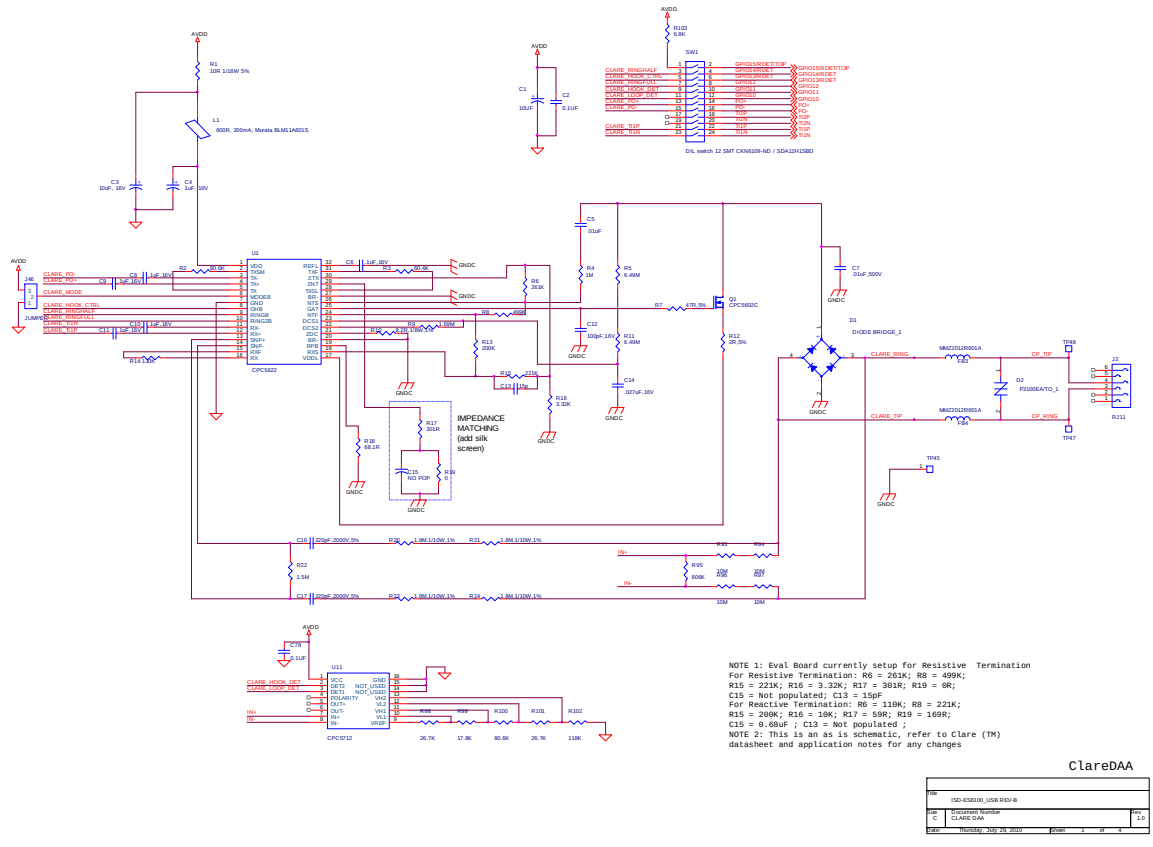


Figure 6-1 Application Reference Schematic with discrete DAA



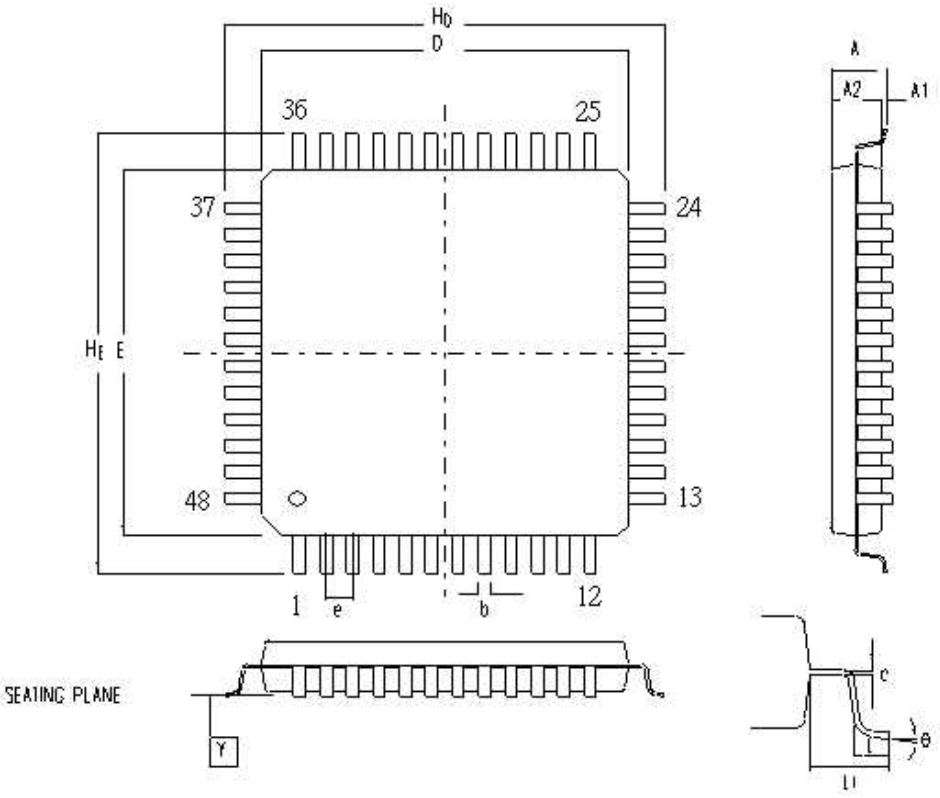


http://www.clare.com/Products/LITELINK.htm

Figure 6-2 Application Reference Schematic with integrated Clare DAA

7. PACKAGE SPECIFICATION

7.1 LQFP48L (7x7x1.4mm footprint 2.0mm)



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A1	0.002	0.004	0.006	0.05	0.10	0.15
A2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
HD	0.350	0.354	0.358	8.90	9.00	9.10
HE	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

8. ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

Condition	Value
Junction temperature	150^0C
Storage temperature range	-65^0C to $+150^0$C
Lead temperature (soldering – 10 seconds)	300^0C
LQFP-48L Thermal Resistance, typical	76 C/W (ASE) 60C/W (Greatek) TBD
Voltage applied to any pin	(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
Input current applied to any digital input pin	+/- 10 mA
ESD (Human Body Model)	2000 V
V_{DD} - V_{SS}	-0.5V to +3.63V
V_{DDL} - V_{SS}	-0.5V to + 1.98V
Device Power Dissipation	0.18 Watt (TBC)

- Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.

8.2 Operating Conditions

OPERATING CONDITIONS (COMMERCIAL PACKAGED PARTS)

CONDITIONS	VALUES
Operating temperature range (Case temperature)	0℃ to +70℃
Supply voltage (V_{DD})[1]	+2.7V to +3.6V
Ground voltage (V_{SS})[2]	0V
Input voltage (V_{DD})[1]	0V to 3.6V
Voltage applied to any pins.	(V_{SS} –0.3V) to (V_{DD} +0.3V)

OPERATING CONDITIONS (INDUSTRIAL PACKAGED PARTS)

CONDITIONS	VALUES
Operating temperature range (Case temperature)	-40°C to +85℃
Supply voltage (V_{DD}) [1]	+2.7V to +3.6V
Ground voltage (V_{SS}) [2]	0V
Input voltage (V_{DD}) [1]	0V to 3.6V

Voltage applied to any pins	(V_{SS} –0.3V) to (V_{DD} +0.3V)

NOTES: [1] $V_{DD} = V_{CCA} = V_{CCD}$
[2] $V_{SS} = V_{SSA} = V_{SSD}$

8.3 DC Parameters

PARAMETER	SYMBOL	MIN	TYP [1]	MAX	UNITS	CONDITIONS
Supply Voltage	V_{DD}	2.7		3.6	V	
Input Low Voltage	V_{IL}	V_{SS}-0.3		0.3xV_{DD}	V	
Input High Voltage	V_{IH}	0.7xV_{DD}		V_{DD}	V	
Schmitt trig. Low to High threshold point	VT+	1.49	1.54	1.58	V	
Schmitt trig. high to low threshold point	VT-	1.24	1.29	1.34	V	
Pull-up resistor	R_{PU}	38	54	83	kΩ	
Pull-down resistor	R_{PD}	25	49	110	kΩ	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 3μA
INTB Output Low Voltage	V_{OL1}			0.4	V	
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -10μA
Internal logic supply	V_{DDL}	1.65	1.8	1.95	V	
Analog outputs DC level	V_{DC}		AV_{DD}/ 2		V	@ +27C
Half supply reference	V_{MIB}		1.65		V	AV_{DD}= 3.3V @ +27C
Bandgap reference	V_{BG}		1.218		V	AV_{DD}= 3.3V @ +27C
Operating Current (outputs loaded: 8 Ohm 120 Ohm)	I_{DD_MAX}		150		mA	AV_{DD}= 3.6V, Loaded, Sampling freq = 8 kHz, all blocks enabled, full scale.
Operating Current (outputs not loaded: 8 Ohm 120 Ohm)	I_{DD_MAX}		45		mA	AV_{DD}= 3.6V, No load, Sampling freq = 8 kHz, all blocks enabled, full scale.
Standby Current	I_{SB}		11	20	μA	AV_{DD}= 3.6V @ +27C
Input Leakage Current	I_{IL}			±10	μA	Force AV_{DD}

Notes: [1] Conditions V_{DD}=3.3V, T_A=25℃ unless otherwise stated

8.4 Analog Transmission Characteristics

AVDD=3.3V ; V_{SS}=0V; T_A=+27°C; All ADC tests using Auxiliary input mode @ 0dB gain

PARAMETER	SYM	CONDITION	TYP	TRANSMIT (ADC)		RECEIVE (DAC)		UNIT
				MIN	MAX	MIN	MAX	
DC level	V_{DC}	DC level on the outputs SPP – SPN; POP - PON	AV_{DD}/2	--	--	1.35	1.8	V
Full Scale Level	T_{XMAX}	ADC (single ended) DAC (differential)	1.35 2.7	1.05 2.1	--- ---	1.05 2.1	--- ---	V_{PK} V_{PK}
Absolute Gain	G_{ABS}	-3dBFS @ 1020 Hz, AVDD =3.3V; T_A=+25°C;	0	-0.40	+0.40	-0.40	+0.40	dB
Absolute Gain variation with Supply Voltage	G_{ABSS}	AVDD=3.13V – 3.47V; -3dBFS @ 1020 Hz; T_A=+25°C	0	-0.50	+0.50	-0.50	+0.50	dB

8.5 Analog Distortion and Noise Parameters

All ADC tests using Auxiliary input mode @ 0dB gain

8.5.1 8kHz sampling

AVDD=3.3V; V_{SS}=0V; T_A=+27°C; 8kHz sampling,
high OSR selected (0x040[5]=1'b1),
dither turned off (0x151[0]=1'b0, 0x141[0]=1'b0)

PARAMETER	SYM	CONDITION	TRANSMIT (A/D)			RECEIVE (D/A)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Signal to Noise Ratio	SNR	Idle channel A-weighted	80	90	--	80	90	--	dB
Total Harmonic Distortion	THD	-3dBFS @ 1020 Hz, 8Ohm speaker load A-weighted	--	0.01	0.018	--	0.16	0.5	%
Frequency Response	F_{low}	-3dB Low pass cut-off		3.36			3.36		kHz
Power Supply Rejection	$PSRR_A$	V_{CCA}; 35mVrms DC to 3.4 kHz, differential inputs and outputs, A-weighted,	--	50	--	--	50	--	dB

8.5.2 16kHz sampling

AVDD=3.3V; V_{SS}=0V; T_A=+27°C; 8kHz sampling,
high OSR selected (0x040[5]=1'b1),
dither turned off (0x151[0]=1'b0, 0x141[0]=1'b0)

PARAMETER	SYM	CONDITION	TRANSMIT (A/D)			RECEIVE (D/A)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Signal to Noise Ratio	SNR	Idle channel A-weighted	80	90	--	80	90	--	dB
Total Harmonic Distortion	THD	-3dBFS @ 1020 Hz, 8Ohm speaker load A-weighted	--	0.01	0.018	--	0.16	0.5	%
Frequency Response	F_{low}	-3dB Low pass cut-off		6.73			6.73		kHz
Power Supply Rejection	$PSRR_A$	V_{CCA}; 35mVrms DC to 6.8 kHz, differential inputs an outputs, A-weighted	--	50	--	--	50	--	dB

8.6 SPI Timing

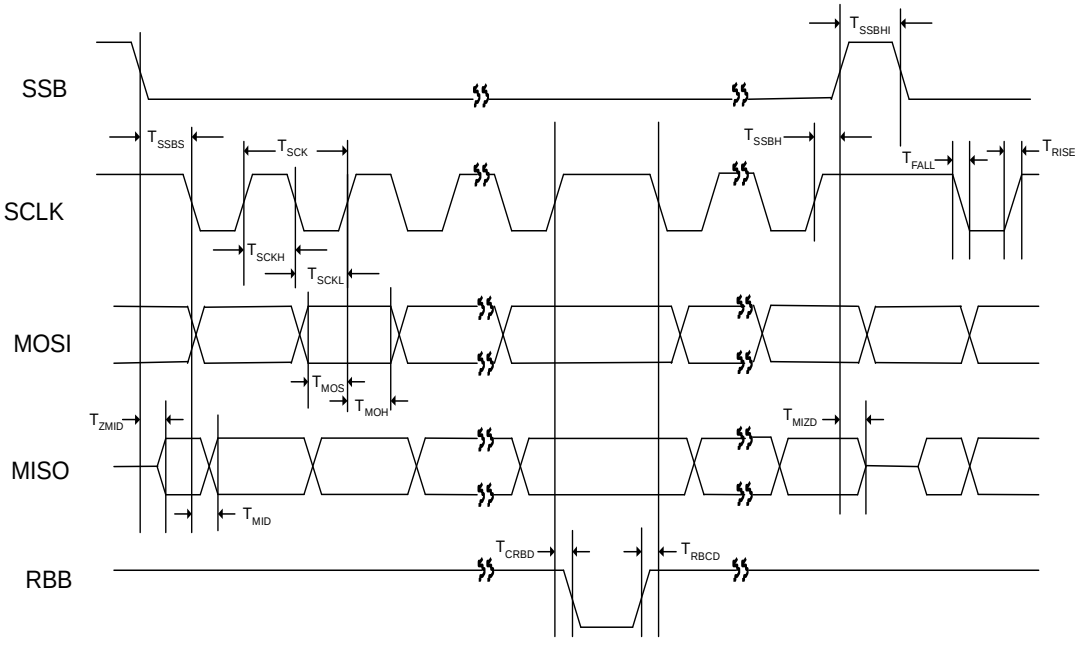


Figure 8-1 SPI Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{SCK}	SCLK Cycle Time	100	---	---	ns
T_{SCKH}	SCLK High Pulse Width	45	---	---	ns
T_{SCKL}	SCLK Low Pulse Width	45	---	---	ns
T_{RISE}	Rise Time for All Digital Signals	---	---	10	ns
T_{FALL}	Fall Time for All Digital Signals	---	---	10	ns
T_{SSBS}	SSB Falling Edge to 1st SCLK Falling Edge Setup Time	60	---	---	ns
T_{SSBH}	Last SCLK Rising Edge to SSB Rising Edge Hold Time	30	---	---	ns
T_{SSBHI}	SSB High Time between SSB Lows	50	---	---	ns
T_{MOS}	MOSI to SCLK Rising Edge Setup Time	45	---	---	ns
T_{MOH}	SCLK Rising Edge to MOSI Hold Time	15	---	---	ns
T_{ZMID}	Delay Time from SSB Falling Edge to MISO Active	--	--	12	ns
T_{MIZD}	Delay Time from SSB Rising Edge to MISO Tri-state	--	--	12	ns
T_{MID}	Delay Time from SCLK Falling Edge to MISO	---	---	40	ns
T_{CRBD}	Delay Time from SCLK Rising Edge to RBB Falling Edge	--	--	12	ns
T_{RBCD}	Delay Time from RBB Rising Edge to SCLK Falling Edge	0	--	--	ns

8.7 Recommended Clock/Crystal Specification

The following crystal or external master clock specifications are recommended for a correct operation.

Parameter	Limit values			Unit	Condition
	Min.	Typ.	Max.		
Frequency	7.56	12.288	32.768	MHz	Fundamental mode
Load capacitance		18		pF	
Dynamic capacitance Cc		22.12		fF	
Resonance resistance Rc		40		Ω	
Electrostatic capacitance		5.1		pF	

8.8 Dual Tone Alert Signal (CAS)

AC Electrical Characteristics – Dual Tone Alert Signal Detection

DESCRIPTION	SYM.	MIN	TYP	MAX	UNITS	NO TEST
Low tone frequency	f_L		2130		Hz	
High tone frequency	f_H		2750		Hz	
Frequency deviation acceptation		± 1.0		± 3.0	%	1
Frequency deviation rejection		± 3.5			%	2
Accept signal level per tone		-40 -37.78		-2 0.22	dBV dBm	S/N=20 3, 5, 7
Reject signal level per tone				-46 -43.78	dBV dBm	S/N=20 4, 5, 7
Positive and negative Twist accept		-10		10	dB	S/N=20 6, 7
Signal to Noise Ratio		20			dB	5, 6, 7

NOTES:

1. The range within which tones are accepted.
2. The range outside of which tones are rejected.
3. This applies BT specification that has covered the requirements of Bell core.
4. This applies MITEL MT8843 specification. Winbond W91030A: -44 dBm, newave NW6006: -47 dBV and CLI CMX602A: -46 dBV.
5. These characteristics are for AVDD=3.3V and 25°C.
6. Both tones have the same amplitude and at the nominal frequencies.

$$\text{Twist} = 20\log\left(\frac{f_H \text{amplitude}}{f_L \text{amplitude}}\right)$$

7. Band limited random noise 300~3400 Hz. Measurement valid only when the tone is present.

AC Timing Characteristics – Dual Tone Alert Signal Detection

Symbol	DESCRIPTION	MIN	TYP	MAX	UNITS	NOTES
t_{CASDP}	Alert signal present detect time	0.5	1.88	10	ms	1
t_{CASDA}	Alert signal absent detect time	0.5	1.46	10	ms	2

NOTES:

1. t_{CASDP} Typical time corresponding to 4 cycles of low tone
2. t_{CASDA} Typical time corresponding to 4 cycles of high tone

8.9 FSK Detection – 1200baud Bell 202, ITU V.23, 300 baud Bell 103, ITU V.21

AC Electrical Characteristics – FSK Detection

DESCRIPTION	SYM.	MIN	TYP	MAX	UNITS	NOTES
Input frequency detection Bell 202 '1' (Mark) Bell 202 '0' (Space) ITU-T V.23 '1' (Mark) ITU-T V.23 '0' (Space)	 f_{MARK} f_{SPACE} 	 1188 2178 1280.5 2068.5	 1200 2200 1300 2100	 1212 2222 1319.5 2131.5	 Hz 	
Transmission Rate			1200		Baud	± 1%
			150		Baud	± 1%
			75		Baud	± 1%
Input detection level per tone		-40 -37.78		-6.2 -4.0	dBV dBm	S/N=20 1,3
Reject signal level per tone				-48 -45.78	dBV dBm	S/N=20 1,3
Positive and negative Twist accept		-10		10	dB	S/N=20 2,3
Signal to Noise Ratio		20			dB	S/N=20 3

DESCRIPTION	SYM.	MIN	TYP	MAX	UNITS	NOTES
Input frequency detection Bell 103 '1' (Mark), high band Bell 103 '0' (Space), high band Bell 103 '1' (Mark), low band Bell 103 '0' (Space), low band ITU-T V.21 '1' (Mark), high band ITU-T V.21 '0' (Space), high band	 f_{MARK} f_{SPACE} f_{MARK} f_{SPACE} f_{MARK} f_{SPACE}	 2213 2013 1258 1058 1638 1838	 2225 2025 1270 1070 1650 1850	 2237 2037 1282 1082 1662 1862	 Hz Hz Hz Hz Hz Hz	
ITU-T V.21 '1' (Mark), low band	f_{MARK}	968	980	992	Hz	
ITU-T V.21 '0' (Space), low band	f_{SPACE}	1168	1180	1192	Hz	
Transmission Rate			300		Baud	± 1%
			110		Baud	± 1%
Input detection level per tone		-40 -37.78		-6.2 -4.0	dBV dBm	S/N=20 1,3
Reject signal level per tone				-48 -45.78	dBV dBm	S/N=20 1,3
Positive and negative Twist accept		-10		10	dB	S/N=20

						2,3
Signal to Noise Ratio		20			dB	S/N=20 3

NOTES:

1. These characteristics are for AVDD=+3.3V and 25°C.
2. Both mark and space have the same amplitude and at the nominal frequencies.

$$\text{Twist} = 20\log\left(\frac{\text{amplitude of } f_{MARK}}{\text{amplitude of } f_{SPACE}}\right)$$

3. Band limited random noise (200~3400 Hz). Measurement is valid only when the FSK signal is present. Note that the BT band is 300~3400 Hz, while the Bellcore band is 0~4K Hz.

8.10 FSK Transmitter – Bell 202, ITU-V.23, Bell 103, ITU-V.21

Modulation rates and characteristic frequencies for the forward data-transmission channel

DESCRIPTION	SYM	MIN	TYP	MAX	UNITS	NOTES
Twist		-0.5	0	0.5	%	
Baud Rate			1200		Baud	± 1%
Bell 202						
“1” (Mark)	f_{MARK}	1197	1200	1203		$\pm 3Hz$
“0” (Space)	f_{SPACE}	2197	2200	2203		$\pm 3Hz$
V.23						
“1” (Mark)	f_{MARK}	1297	1300	1303		$\pm 3Hz$
“0” (Space)	f_{SPACE}	2097	2100	2103		$\pm 3Hz$

DESCRIPTION	SYM	MIN	TYP	MAX	UNITS	NOTES
Twist		-0.5	0	0.5	%	
Baud Rate			300		Baud	± 1%
			110		Baud	± 1%
Bell 103						
“1” (Mark), high band	f_{MARK}	2222	2225	2228		$\pm 3Hz$
“0” (Space), high band	f_{SPACE}	2022	2025	2028		$\pm 3Hz$
“1” (Mark), high band	f_{MARK}	1267	1270	1273		$\pm 3Hz$
“0” (Space), high band	f_{SPACE}	1067	1070	1073		$\pm 3Hz$
V.21						
“1” (Mark), high band	f_{MARK}	1647	1650	1653		$\pm 3Hz$
“0” (Space), high band	f_{SPACE}	1847	1850	1853		$\pm 3Hz$
“1” (Mark), low band	f_{MARK}	977	980	983		$\pm 3Hz$
“0” (Space), low band	f_{SPACE}	1177	1180	1183		$\pm 3Hz$

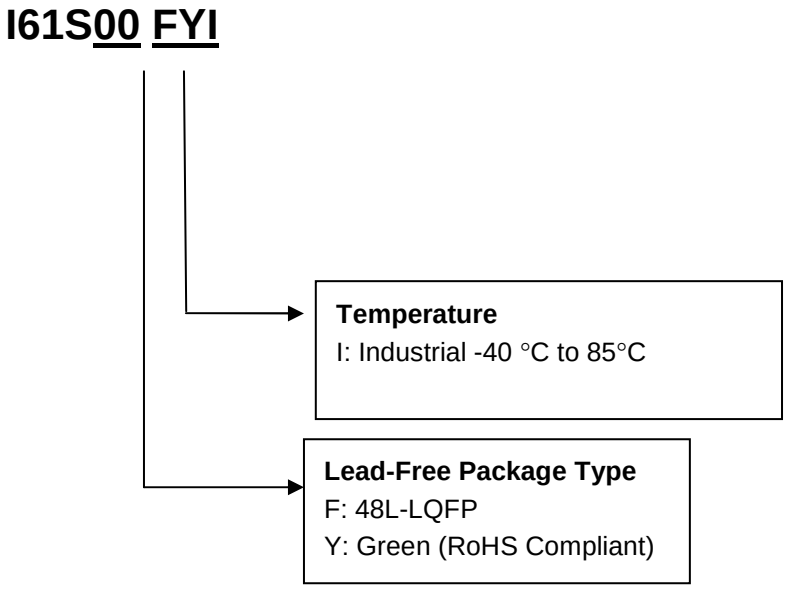
*Tx signal % baud or bit rate accuracy is the same as XTAL/CLOCK % frequency accuracy.

8.11 DTMF Detection

AC Electrical Characteristics – DTMF detection

Description	Sym	Min	Typ	Max	Units	Notes
Frequency Deviation Acceptation				±2.0	%	
Frequency Deviation Rejection		±3.5			%	
Accept signal level per tone		-36		-6	dBm	
Reject signal per tone				-46	dBm	
Positive and negative Twist accept				10	dB	S/N=20
Signal to Noise Ratio		20			dB	

9. ORDERING INFORMATION



10. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
2.5	May 5, 2010		• Update pin-out diagram. • Update block diagram.
2.6	Sep 28, 2010		• Add table of supported serial flash memory.
2.7	Mar 10, 2011		• Update SPI timing spec.

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