

ISD5100 SERIES

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SINGLE-CHIP

1 TO 16 MINUTES DURATION

VOICE RECORD/PLAYBACK DEVICES

WITH DIGITAL STORAGE CAPABILITY

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1. GENERAL DESCRIPTION

The ISD5100 ChipCorder® Series provide high quality, fully integrated, single-chip Record/Playback solutions for 1- to 16-minute messaging applications that are ideal for use in cellular phones, automotive communications, GPS/navigation systems and other portable products. The ISD5100 Series products are an enhancement of the ISD5000 architecture, providing: 1) the I²C serial port - address, control and duration selection are accomplished through an I²C interface to minimize pin count (ONLY two control lines required); 2) the capability of storing digital data, in addition to analog data. This feature allows customers to store phone numbers, system configuration parameters and message address locations for message management capability; 3) Various internal circuit blocks can be individually powered-up or -down for power saving.

The ISD5100 Series include:

- ISD5116 from 8 to 16 minutes
- ISD5108 from 4 to 8 minutes
- ISD5104 from 2 to 4 minutes
- ISD5102 from 1 to 2 minutes

Analog functions and audio gating have also been integrated into the ISD5100 Series products to allow easy interface with integrated digital cellular chip sets on the market. Audio paths have been designed to enable full duplex conversation record, voice memo, answering machine (including outgoing message playback) and call screening features. This product enables playback of messages while the phone is in standby, AND both simplex and duplex playback of messages while on a phone call.

Additional voice storage features for digital cellular phones include: 1) a personalized outgoing message can be sent to the person by getting caller-ID information from the host chipset, 2) a private call announce while on call can be heard from the host by giving caller-ID on call waiting information from the host chipset.

Logic Interface Options of 2.0V and 3.0V are supported by the ISD5100 Series to accommodate portable communication products (2.0- and 3.0-volt required).

Like other ChipCorder® products, the ISD5100 Series integrate the sampling clock, anti-aliasing and smoothing filters, and the multi-level storage array on a single-chip. For enhanced voice features, the ISD5100 Series eliminate external circuitry by integrating automatic gain control (AGC), a power amplifier/speaker driver, volume control, summing amplifiers, analog switches, and a car kit interface. Input level adjustable amplifiers are also included, providing a flexible interface for multiple applications.

Recordings are stored into on-chip nonvolatile memory cells, providing zero-power message storage. This unique, single-chip solution is made possible through Nuvoton's patented multilevel storage technology. Voice and audio signals are stored directly into solid-state memory in their natural, uncompressed form, providing superior quality on voice and music reproduction.

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2. FEATURES

Fully-Integrated Solution

- Single-chip voice record/playback solution
- Dual storage of digital and analog data
- Durations

Device	ISD5102	ISD5104	ISD5108	ISD5116
Duration	1 to 2 minutes	2 to 4 minutes	4 to 8 minutes	8 to 16 minutes

Low Power Consumption

- Supply Voltage
 - Commercial Temperature = +2.7V to +3.3V
 - Industrial Temperature = +2.7V to +3.3V (+2.7V to +3.6V for ISD5108 only)
- Supports 2.0V and 3.0V interface logic
- Operating Current:
 - $I_{CC\ Play} = 15\text{ mA}$ (typical)
 - $I_{CC\ Rec} = 30\text{ mA}$ (typical)
 - $I_{CC\ Feedthrough} = 12\text{ mA}$ (typical)
- Standby Current:
 - $I_{SB} = 1\mu\text{A}$ (typical)
- Most stages can be individually powered down to minimize power consumption

Enhanced Voice Features

- One or two-way conversation record
- One or two-way message playback
- Voice memo record and playback
- Private call screening
- In-terminal answering machine
- Personalized outgoing message
- Private call announce while on call

Digital Memory Features

Device	ISD5102	ISD5104	ISD5108	ISD5116
Storage	Up to 512Kb	Up to 1 Mb	Up to 2 Mb	Up to 4 Mb

- Storage of phone numbers, system configuration parameters and message address table in some application

Easy-to-use and Control

- No compression algorithm development required
- User-controllable sampling rates
- Programmable analog interface
- Standard & Fast mode I²C serial interface (100kHz – 400 kHz)
- Fully addressable for multiple messages

High Quality Solution

- High quality voice and music reproduction
- Nuvoton's standard 100-year message retention (typical)
- 100K record cycles (typical) for analog data
- 10K record cycles (typical) for digital data

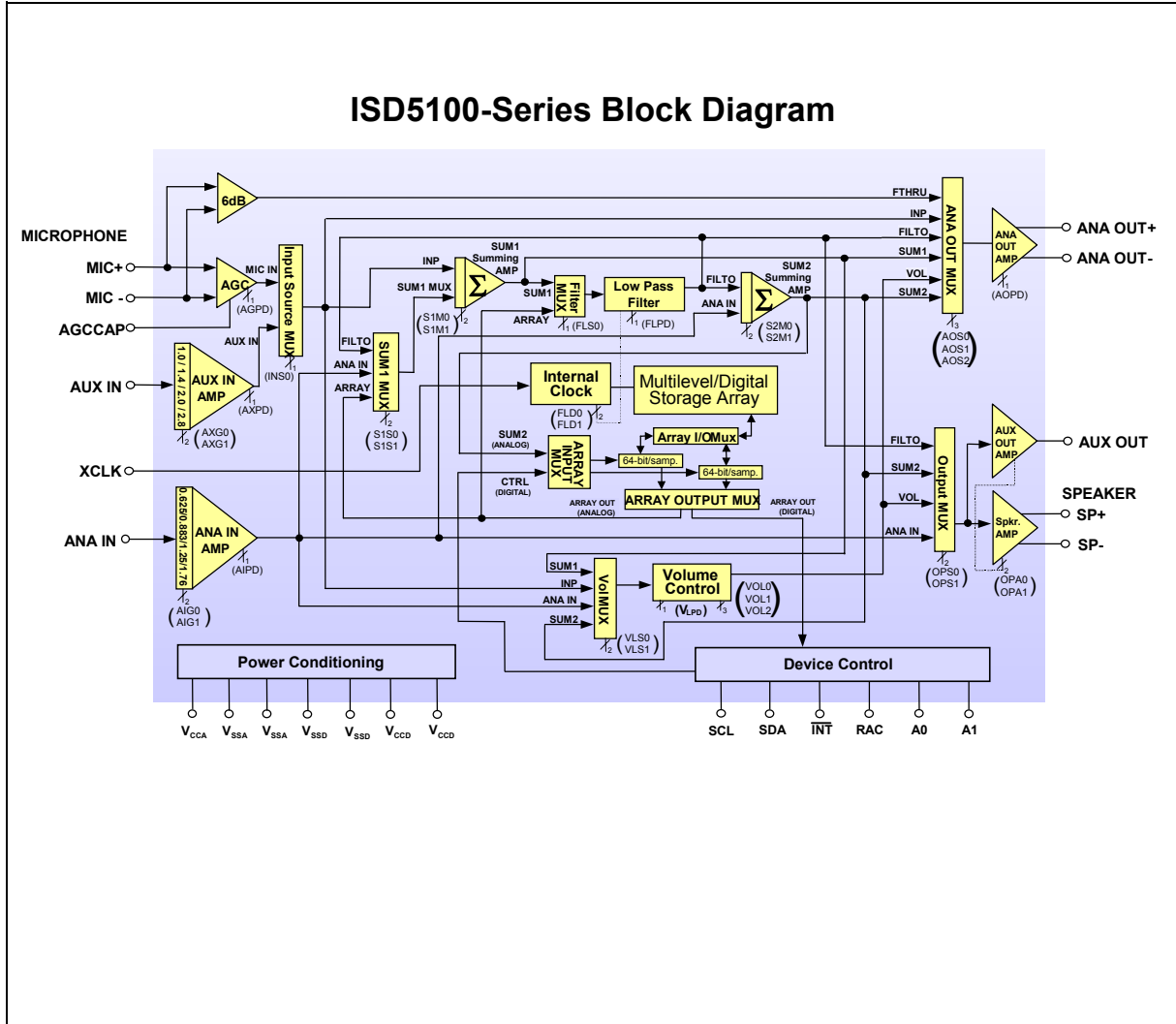
Options

- Available in die form, TSOP and SOIC and PDIP (ISD5116 Only)
- Temperature: Commercial – Packaged (0 to +70°C) & die (0 to +50°C); Industrial (-40 to +85°C)
- Pb-free package

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3. BLOCK DIAGRAM

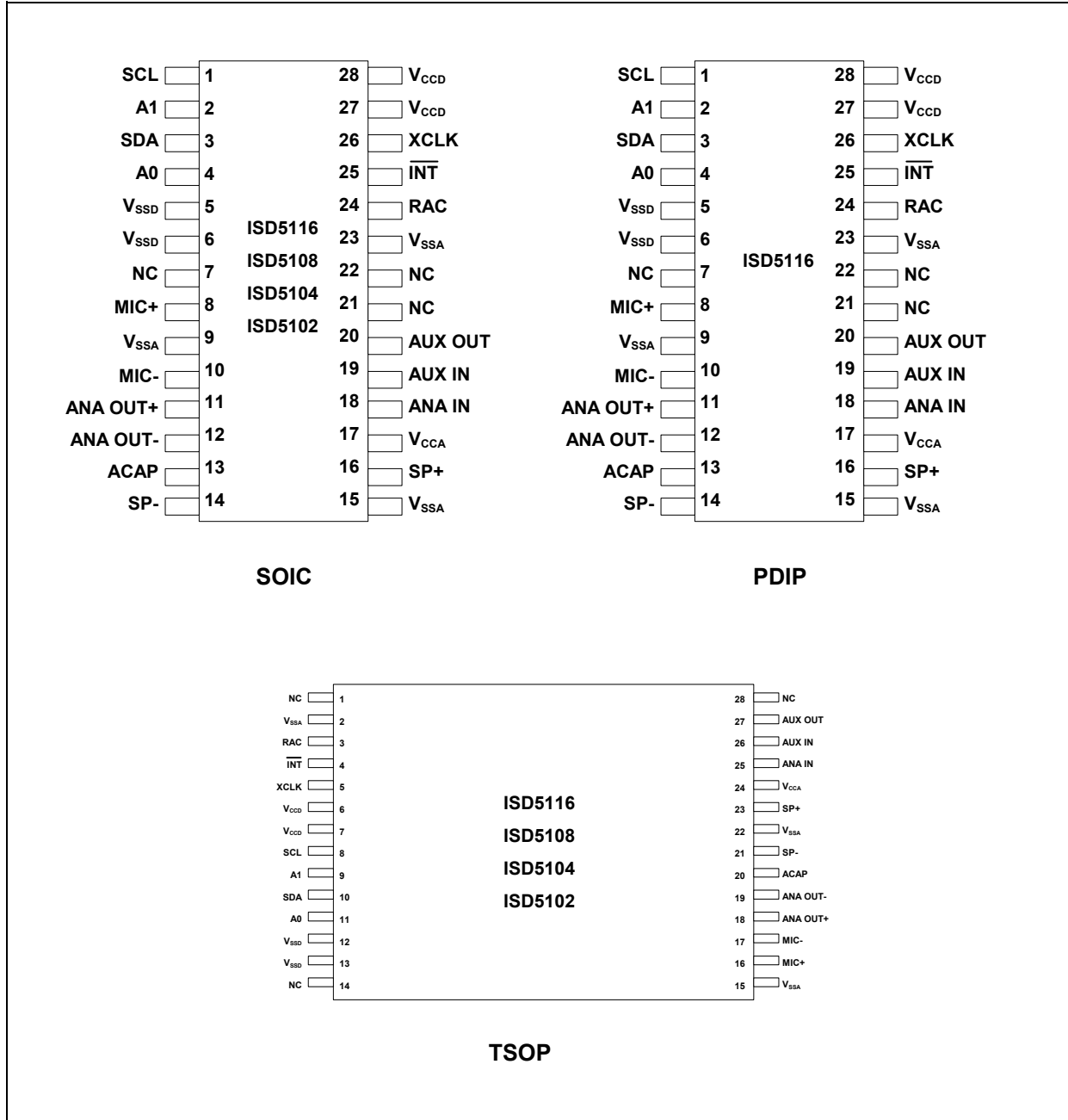


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4. PIN CONFIGURATION



ISD5100 SERIES**nuvoTon****5. PIN DESCRIPTION**

Pin Name	SOIC/PDIP	TSOP	Functionality
SCL	1	8	I ² C Serial Clock Line: to clock the data into and out of the I ² C interface.
A1	2	9	Input pin that supplies the LSB +1 bit for the I ² C Slave Address.
SDA	3	10	I ² C Serial Data Line: Data is passed between devices on the bus over this line.
A0	4	11	Input pin that supplies the LSB for the I ² C Slave Address.
V _{SSD}	5,6	12,13	Digital Ground.
NC	7,21,22	1,14,28	No Connect.
MIC+	8	16	Differential Positive Input for the microphone amplifier.
V _{SSA}	9,15,23	2,15,22	Analog Ground.
MIC-	10	17	Differential Negative Input for the microphone amplifier.
ANA OUT+	11	18	Differential Positive Analog Output for ANA OUT.
ANA OUT-	12	19	Differential Negative Analog Output for ANA OUT.
ACAP	13	20	AGC/AutoMute Capacitor: Required for the on-chip AGC amplifier during record and AutoMute function during playback.
SP-	14	21	Differential Negative Speaker Output: When the speaker outputs are in use, the AUX OUT output is disabled.
SP+	16	23	Differential Positive Speaker Output.
V _{CCA}	17	24	Analog Supply Voltage: This pin supplies power to the analog sections of the device. It should be carefully bypassed to Analog Ground to insure correct device operation.
ANA IN	18	25	Analog Input: one of the analog inputs with selectable gain.
AUX IN	19	26	Auxiliary Input: one of the analog inputs with selectable gain.
AUX OUT	20	27	Auxiliary Output: one the analog outputs of the device. When this output is used, the SP+ and SP- outputs are disabled.
RAC	24	3	Row Address Clock; an open drain output. The RAC pin goes LOW $T_{RACL}^{[1]}$ before the end of each row of memory and returns HIGH at exactly the end of each row of memory.
$\overline{\text{INT}}$	25	4	Interrupt Output; an open drain output that indicates that a set EOM bit has been found during Playback or that the chip is in an Overflow (OVF) condition. This pin remains LOW until a Read Status command is executed.
XCLK	26	5	This pin must be grounded for utilizing internal clock. For precision timing control, external clock signal can be applied through this pin.
V _{CCD}	27,28	6,7	Digital Supply Voltage. These pins supply power to the digital sections of the device. They must be carefully bypassed to Digital Ground to insure correct device operation.

^[1] See the [Parameters section](#)

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6. FUNCTIONAL DESCRIPTION

6.1. OVERVIEW

6.1.1 Speech/Voice Quality

The ISD5100 ChipCorder Series can be configured via software to operate at 4.0, 5.3, 6.4 or 8.0 kHz sampling frequency to select appropriate voice quality. Increasing the duration decreases the sampling frequency and bandwidth, which affects audio quality. The table in the following section shows the relationship between sampling frequency, duration and filter pass band.

6.1.2 Duration

To meet system requirements, the ISD5100 Series are single-chip solution, which provide 1 to 16 minutes of voice record and playback, depending upon the sample rates chosen.

Sample Rate (kHz)	Duration ^[1]				Typical Filter Knee (kHz)
	ISD5116	ISD5108	ISD5104	ISD5102	
8.0	8 min 44 sec	4 min 22 sec	2 min 11 sec	1 min 5 sec	3.4
6.4	10 min 55 sec	5 min 27 sec	2 min 43 sec	1 min 21 sec	2.7
5.3	13 min 6 sec	6 min 33 sec	3 min 17 sec	1 min 38 sec	2.3
4.0	17 min 28 sec	8 min 44 sec	4 min 22 sec	2 min 11 sec	1.7

^[1] Minus any pages selected for digital storage

6.1.3 Flash Technology

One of the benefits of Nuvoton's ChipCorder technology is the use of on-chip Flash memory, which provides zero-power message storage. The message is retained for up to 100 years (typically) without power. In addition, the device can be re-recorded over 10,000 times (typically) for the digital data and over 100,000 times (typically) for the analog messages.

A new feature has been added that allows memory space in the ISD5100 Series to be allocated to either digital or analog storage when recorded. The fact that a section has been assigned digital or analog data is stored in the Message Address Table by the system microcontroller when the recording is made.

6.1.4 Microcontroller Interface

The ISD5100 Series are controlled through an I²C 2-wire interface. This synchronous serial port allows commands, configurations, address data, and digital data to be loaded into the device, while allowing status, digital data and current address information to be read back from the device. In addition to the serial interface, two other status pins can feedback to the microcontroller for enhanced

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interface. These are the $\overline{\text{RAC}}$ timing pin and the $\overline{\text{INT}}$ pin for interrupts to the controller. Communications with all the internal registers of any operations are through the serial bus, as well as digital memory Read and Write operations.

6.1.5 Programming

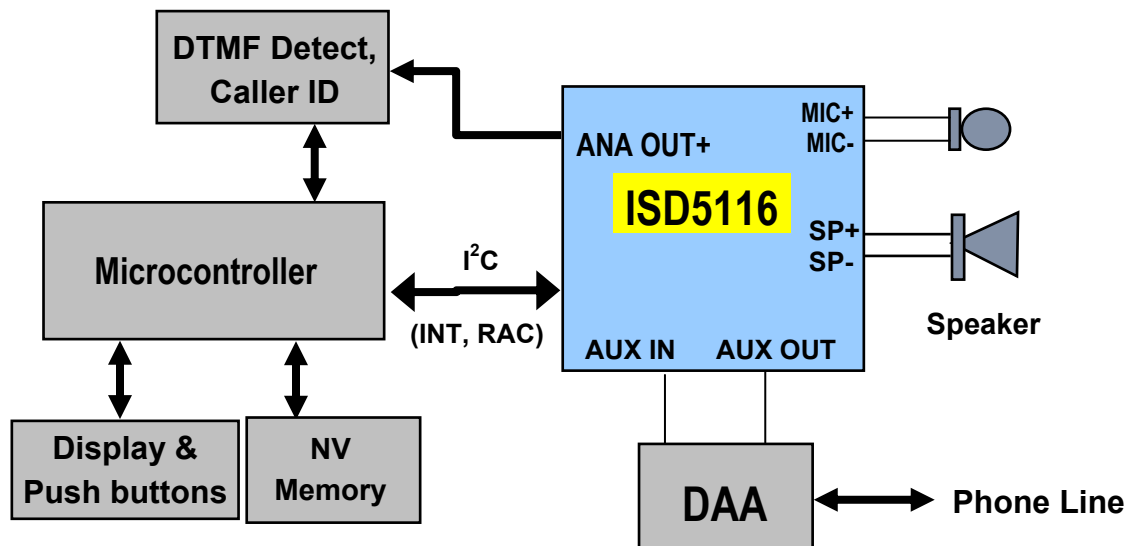
The ISD5100 Series are also ideal for playback-only applications, where single or multiple messages may be played back when desired. Playback is controlled through the I²C interface. Once the desired message configuration is created, duplicates can easily be generated via a third-party programmer. For more information on available application tools and programmers, please see the Nuvoton web site at www.Nuvoton-usa.com

6.2. FUNCTIONAL DETAILS

The ISD5100 Series are single chip solutions for analog and digital data storage. The array can be divided between analog and digital storage according to user's choice, when the device is configured.

The below block diagram shows that the ISD5116 device can be easily designed into a telephone answering machine (TAD). Both Mic inputs transmit the voice input signal from the microphone to perform OGM recording, as well as to record the speech during phone conversation (simplex).

When the TAD is activated, the voice of the other party from the phone line feeds into the AUX IN, and is recorded into the ISD5116 device. Then the new message is usually indicated with blinking new message LED. Hence, during playback, the recorded message is sent out to speaker with volume control. Two I²C pins are used for all communications between the ChipCorder and the microcontroller for analog and/or digital storage, and the two outputs, INT and RAC are feedback to microcontroller for message management.



For duplex recording, speech from Mic inputs and message from received path can be directly recorded into the array simultaneously, then playback afterwards. In addition, for speaker phone

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operation, voice from Mic inputs are fed to AUX OUT and transmitted to the phone line, while message from other party is input from the AUX IN, then fed through to the speaker for listening.

The ISD5100 device has the flexibility for other applications, because the audio paths can be configured differently, with each circuit block being powered-up or –down individually, according to the applications requirement.

6.2.1 Internal Registers

The ISD5100 Series have multiple internal registers that are used to store the address information and the configuration or set-up of the device. The two 16-bit configuration registers control the audio paths through the device, the sample frequency, the various gains and attenuations, power up and down of different sections, and the volume settings. These registers are discussed in detail in [section 7.3.5](#).

6.2.2 Memory Architecture

The ISD5100 Series memory array are arranged in various pages (or rows) of each 2048 bits as follows. The primary addressing for the pages are handled by 11 bits of address input in the analog mode.

A memory page is 2048 bits organized as thirty-two 64-bit "blocks" when used for digital storage. The contents of a page are either analog or digital. This is determined by instruction (opcode) at the time the data is written. A record of where is analog and where is digital, is stored in a message address table (MAT) by the system microcontroller. The MAT is a table kept in the microcontroller memory that defines the status of each message "page". It can be stored back into the ISD5100 Series if the power fails or the system is turned off. Using this table allows efficient message management. Segments of messages can be stored wherever there is available space in the memory array. [This is explained in detail for the ISD5008 in Applications Note #9 and will be similarly described in a later Note for the ISD5100-Series.]

Products	Pages (Rows)	Bits/Page	Memory Size
ISD5116	2048	2048	4,194,304 bits
ISD5108	1024	2048	2,097,152 bits
ISD5104	512	2048	1,048,576 bits
ISD5102	256	2048	524,288 bits

When a page is used for analog storage, the same 32 blocks are present but there are 8 EOM (End-of-Message) markers. This means that for each 4 blocks there is an EOM marker at the end. Thus, when recording, the analog recording will stop at any one of eight positions. At 8 kHz sampling frequency, this results in a resolution of 32 msec when ENDING an analog recording. Beginning an analog recording is limited to the 256 msec resolution provided by the 11-bit address. A recording does not immediately stop when the Stop command is given, but continues until the 32 millisecond block is filled. Then a bit is placed in the EOM memory to develop the interrupt that signals a message is finished playing in the Playback mode.

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Digital data is sent and received serially over the I²C interface. The data is serial-to-parallel converted and stored in one of two alternating (commutating) 64-bit shift registers. When an input register is full, it becomes the register that is parallel written into the array. The prior write register becomes the new serial input register. A mechanism is built-in to ensure there is always a register available for storing new data.

Storing data in the memory is accomplished by accepting data one byte at a time and issuing an acknowledge. If data is coming in faster than it can be written, the chip issues an acknowledge to the host microcontroller, but holds SCL LOW until it is ready to accept more data. (See section 7.5.2 for details).

The read mode is the opposite of the write mode. Data is read into one of two 64-bit registers from the array and serially sent to the I²C interface. (See [section 7.5.3](#) for details).

6.3. OPERATIONAL MODES DESCRIPTION

6.3.1 I²C Interface

To use more than four ISD5100 Series devices in an application requires some external switching of the I²C interface.

I²C interface

Important note: *The rest of this data sheet will assume that the reader is familiar with the I²C serial interface. Additional information on I²C may be found in [section 10](#) on page 72 of this document. If you are not familiar with this serial protocol, please read this section to familiarize yourself with it. A large amount of additional information on I²C can also be found on the Philips web page at <http://www.philips.com/>.*

I²C Slave Address

The ISD5100 Series have 7-bit slave address of <100 00xy> where x and y are equal to the state, respectively, of the external address pins A1 and A0. Because all data bytes are required to be 8 bits, the LSB of the address byte is the Read/Write selection bit that tells the slave whether to transmit or receive data. Therefore, there are 8 possible slave addresses for the ISD5100-Series. These are:

ISD5100 SERIES**nuvoTon****Pinout Table**

A1	A0	Slave Address	$\overline{\text{R/W}}$ Bit	HEX Value
0	0	<100 0000>	0	80
0	1	<100 0001>	0	82
1	0	<100 0010>	0	84
1	1	<100 0011>	0	86
0	0	<100 0000>	1	81
0	1	<100 0001>	1	83
1	0	<100 0010>	1	85
1	1	<100 0011>	1	87

ISD5100 Series I²C Operation Definitions

There are many control functions used to operate the ISD5100-Series. Among them are:

6.3.1.1. Read Status Command:

The Read Status command is a read request from the Host processor to the ISD5100 Series without delivering a Command Byte. The Host supplies all the clocks (SCL). In each case, the entity sending the data drives the data line (SDA). The Read Status Command is executed by the following I²C sequence.

1. Host executes I²C START
2. Send Slave Address with R/W bit = "1" (Read) 81h
3. Slave (ISD5100-Series) responds back to Host an Acknowledge (ACK) followed by 8-bit Status word
4. Host sends an Acknowledge (ACK) to Slave
5. Wait for SCL to go HIGH
6. Slave responds with Upper Address byte of internal address register
7. Host sends an ACK to Slave
8. Wait for SCL to go HIGH
9. Slave responds with Lower Address byte of internal address register (A[4:0] will always return set to 0.)
10. Host sends a NO ACK to Slave, then executes I²C STOP

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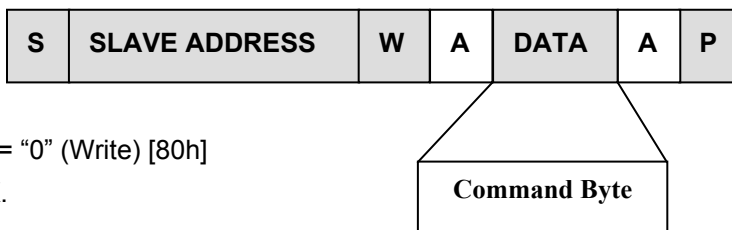
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6.3.1.2. Load Command Byte Register (Single Byte Load):

A single byte may be written to the Command Byte Register in order to power up the device, start or stop Analog Record (if no address information is needed), or do a Message Cueing function. The Command Byte Register is loaded as follows:

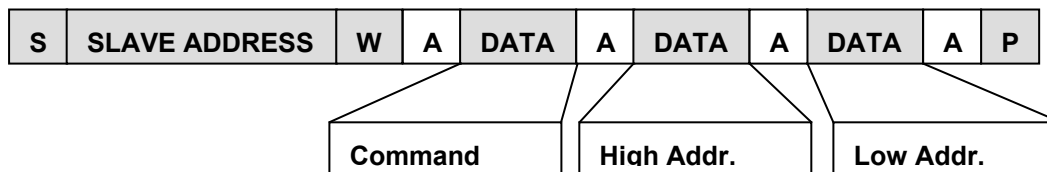


1. Host executes I²C START
2. Send Slave Address with R/W bit = "0" (Write) [80h]
3. Slave responds back with an ACK.
4. Wait for SCL to go HIGH
5. Host sends a command byte to Slave
6. Slave responds with an ACK
7. Wait for SCL to go HIGH
8. Host executes I²C STOP

6.3.1.3. Load Command Byte Register (Address Load)

For the normal addressed mode the Registers are loaded as follows:

1. Host executes I²C START
2. Send Slave Address with R/W bit = "0" (Write)
3. Slave responds back with an ACK.
4. Wait for SCL to go HIGH
5. Host sends a byte to Slave - (Command Byte)
6. Slave responds with an ACK
7. Wait for SCL to go HIGH
8. Host sends a byte to Slave - (High Address Byte)
9. Slave responds with an ACK
10. Wait for SCL to go HIGH
11. Host sends a byte to Slave - (Low Address Byte)
12. Slave responds with an ACK
13. Wait for SCL to go HIGH
14. Host executes I²C STOP



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6.3.2 I²C Control Registers

The ISD5100 Series are controlled by loading commands to, or, reading from, the internal command, configuration and address registers. The Command byte sent is used to start and stop recording, write or read digital data and perform other functions necessary for the operation of the device.

Command Byte

Control of the ISD5100 Series are implemented through an 8-bit command byte, sent after the 7-bit device address and the 1-bit Read/Write selection bit. The 8 bits are:

- Global power up bit
- DAB bit: determines whether device is performing an analog or digital function
- 3 function bits: these determine which function the device is to perform in conjunction with the DAB bit.
- 3 register address bits: these determine if and when data is to be loaded to a register

Power Up Bit

C7	C6	C5	C4	C3	C2	C1	C0
PU	DAB	FN2	FN1	FN0	RG2	RG1	RG0
Function Bits					Register Bits		

Function Bits

The command byte function bits are detailed in the table to the right. C6, the DAB bit, determines whether the device is performing an analog or digital function. The other bits are decoded to produce the individual commands. Not all decode combinations are currently used, and are reserved for future use. Out of 16 possible codes, the ISD5100 Series uses 7 for normal operation. The other 9 are undefined

Function Bits				Function
C6	C5	C4	C3	
DAB	FN2	FN1	FN0	
0	0	0	0	STOP (or do nothing)
0	1	0	1	Analog Play
0	0	1	0	Analog Record
0	1	1	1	Analog MC
1	1	0	0	Digital Read
1	0	0	1	Digital Write
1	0	1	0	Erase (row)

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Register Bits

The register load may be used to modify a command sequence (such as load an address) or used with the null command sequence to load a configuration or test register. Not all registers are accessible to the user. [RG2 is always 0 as the four additional combinations are undefined.]

RG2	RG1	RG0	Function
C2	C1	C0	
0	0	0	No action
0	0	1	Reserved
0	1	0	Load CFG0
0	1	1	Load CFG1

6.3.3 Opcode Summary

OpCode Command Description

The following commands are used to access the chip through the I²C interface.

- Play: analog play command
- Record: analog record command
- Message Cue: analog message cue command
- Read: digital read command
- Write: digital write command
- Erase: digital page and block erase command
- Power up: global power up/down bit. (C7)
- Load CFG0: load configuration register 0
- Load CFG1: load configuration register 1
- Read STATUS: Read the interrupt status and address register, including a hardwired device ID

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OPCODE	HEX	Pwr	Function Bits				Register Bits		
		PU	DAB	FN2	FN1	FN0	RG2	RG1	RG0
COMMAND BIT NUMBER	CMD	C7	C6	C5	C4	C3	C2	C1	C0
POWER UP	80	1	0	0	0	0	0	0	0
POWER DOWN	00	0	0	0	0	0	0	0	0
STOP (DO NOTHING) STAY ON	80	1	0	0	0	0	0	0	0
STOP (DO NOTHING) STAY OFF	00	0	0	0	0	0	0	0	0
LOAD CFG0	82	1	0	0	0	0	0	1	0
LOAD CFG1	83	1	0	0	0	0	0	1	1
RECORD ANALOG	90	1	0	0	1	0	0	0	0
RECORD ANALOG @ ADDR	91	1	0	0	1	0	0	0	1
PLAY ANALOG	A8	1	0	1	0	1	0	0	0
PLAY ANALOG @ ADDR	A9	1	0	1	0	1	0	0	1
MSG CUE ANALOG	B8	1	0	1	1	1	0	0	0
MSG CUE ANALOG @ ADDR	B9	1	0	1	1	1	0	0	1
ENTER DIGITAL MODE	C0	1	1	0	0	0	0	0	0
EXIT DIGITAL MODE	40	0	1	0	0	0	0	0	0
DIGITAL ERASE PAGE	D0	1	1	0	1	0	0	0	0
DIGITAL ERASE PAGE @ ADDR	D1	1	1	0	1	0	0	0	1
DIGITAL WRITE	C8	1	1	0	0	1	0	0	0
DIGITAL WRITE @ ADDR	C9	1	1	0	0	1	0	0	1
DIGITAL READ	E0	1	1	1	0	0	0	0	0
DIGITAL READ @ ADDR	E1	1	1	1	0	0	0	0	1
READ STATUS ¹	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

1. See [section 7.2](#) on page 12 for details.

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6.3.4 Data Bytes

In the I²C write mode, the device can accept data sent after the command byte. If a register load option is selected, the next two bytes are loaded into the selected register. The format of the data is MSB first, the I²C standard. Thus to load DATA<15:0> into the device, DATA<15:8> is sent first, the byte is acknowledged, and DATA<7:0> is sent next. The address register consists of two bytes. The format of the address is as follows:

ADDRESS<15:0> = PAGE_ADDRESS<10:0>, BLOCK_ADDRESS<4:0>

Note: if an analog function is selected, the block address bits must be set to 0000. Digital Read and Write are block addressable.

When the device is polled with the Read Status command, it will return three bytes of data. The first byte is the status byte, the next the upper address byte and the last the lower address byte. The status register is one byte long and its bit function is:

STATUS<7:0> = EOM, OVF, READY, PD, PRB, DEVICE_ID<2:0>

Lower address byte will always return the block address bits as zero, either in digital or analog mode.

The functions of the bits are:

EOM	BIT 7	Indicates whether an EOM interrupt has occurred.
OVF	BIT 6	Indicates whether an overflow interrupt has occurred.
READY	BIT 5	Indicates the internal status of the device – if READY is LOW no new commands should be sent to device, i.e. Not Ready.
PD	BIT 4	Device is powered down if PD is HIGH.
PRB	BIT 3	Play/Record mode indicator. HIGH=Play/LOW=Record.
DEVICE_ID	BIT 0, 1, 2	An internal device ID. ISD5116 = 001; ISD5108 = 010; ISD5104 = 100 and ISD5102 = 101.

It is recommended that you read the status register after a Write or Record operation to ensure that the device is ready to accept new commands. Depending upon the $\overline{\text{design}}$ and the number of pins available on the controller, the polling overhead can be reduced. If $\overline{\text{INT}}$ and $\overline{\text{RAC}}$ are tied to the microcontroller, it does not have to poll as frequently to determine the status of the ISD5100-SERIES.

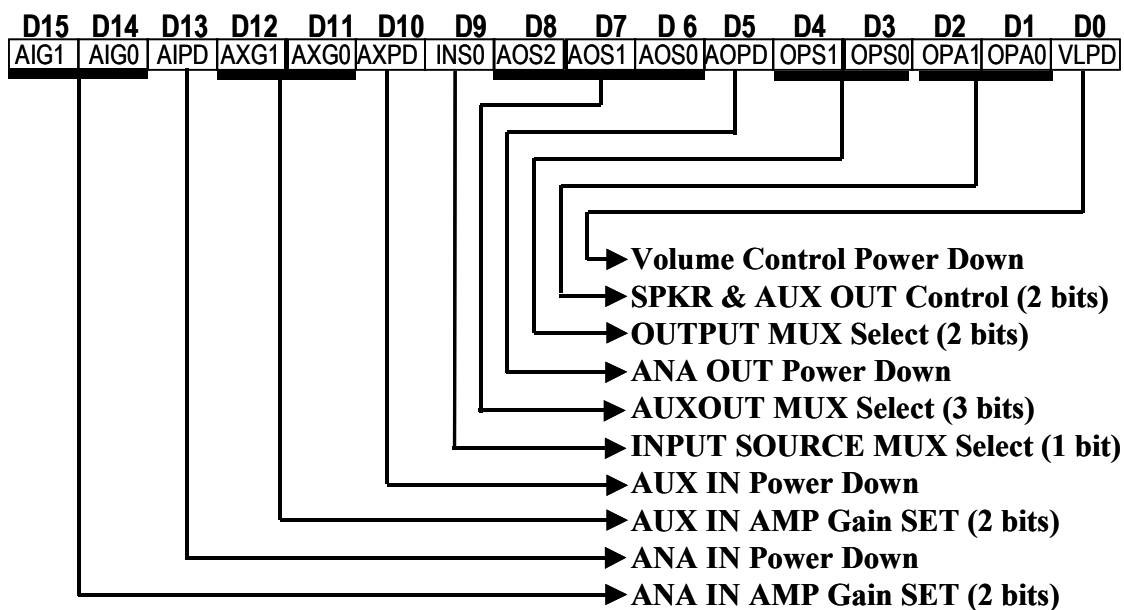
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6.3.5 Configuration Register Bytes

The configuration register bytes are defined, in detail, in the drawings of [section 7.4](#) on page 29. The drawings display how each bit enables or disables a function of the audio paths in the ISD5100-Series. The tables below give a general illustration of the bits. There are two configuration registers, CFG0 and CFG1, so there are four 8-bit bytes to be loaded during the set-up of the device.

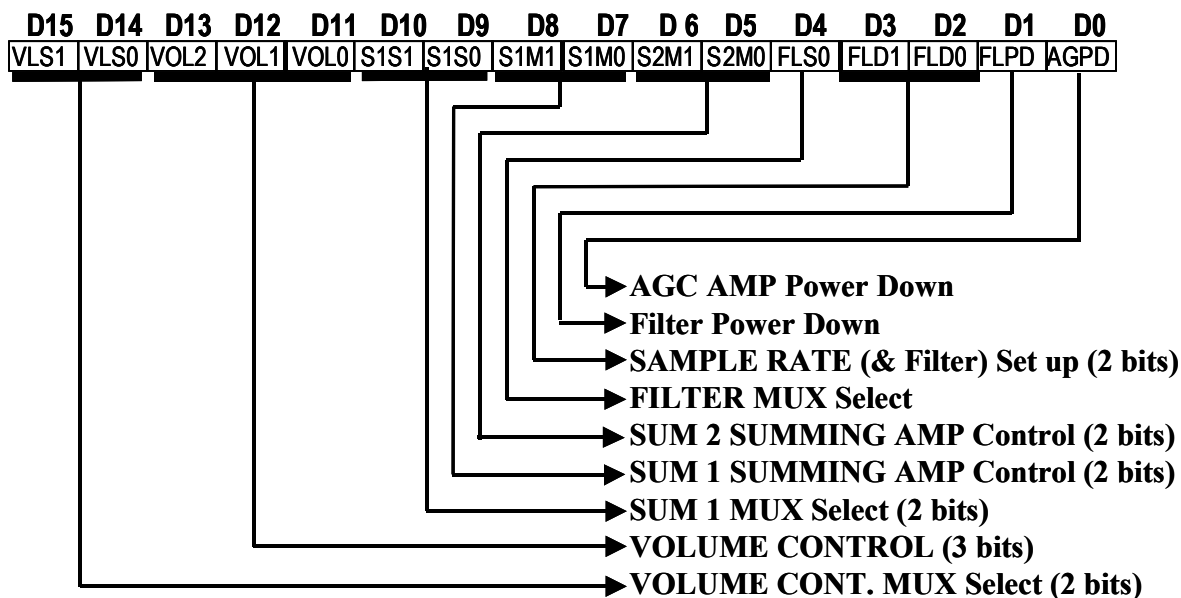
Configuration Register 0 (CFG0)



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Configuration Register 1 (CFG1)



6.3.6 Power-up Sequence

This sequence prepares the ISD5100 Series for an operation to follow, waiting the T_{pud} time before sending the next command sequence.

1. Send I²C POWER UP
2. Send one byte 10000000 {Slave Address, R/W = 0} 80h
3. Slave ACK
4. Wait for SCL High
5. Send one byte 10000000 {Command Byte = Power Up} 80h
6. Slave ACK
7. Wait for SCL High
8. Send I²C STOP

Playback Mode

The command sequence for an analog Playback operation can be handled several ways. The most straightforward approach would be to incorporate a single four byte exchange, which consists of the Slave Address (80h), the Command Byte (A9h) for Play Analog @ Address, and the two address bytes.

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Record Mode

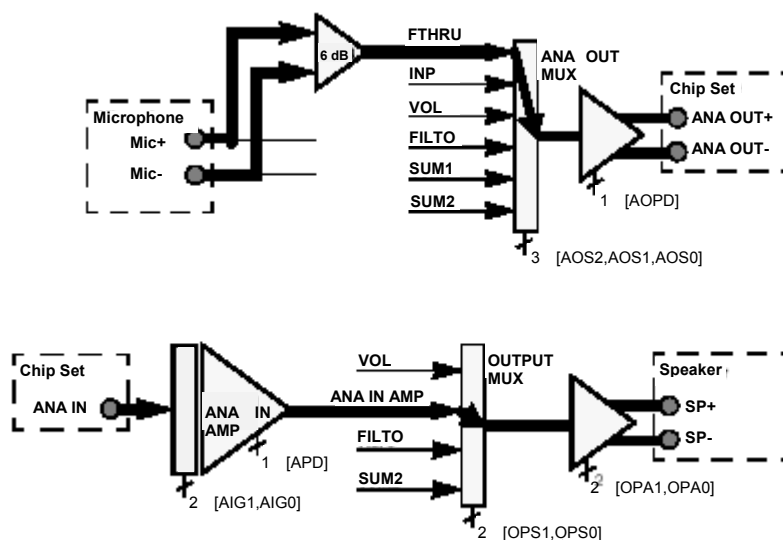
The command sequence for an Analog Record would be a four byte sequence consisting of the Slave Address (80h), the Command Byte (91h) for Record Analog @ Address, and the two address bytes. See [“Load Command Byte Register \(Address Load\)”](#) in section 7.3.2 on page 17.

6.3.7 Feed Through Mode

The previous examples were dependent upon the device already being powered up and the various paths being set through the device for the desired operation. To set up the device for the various paths requires loading the two 16-bit Configuration Registers with the correct data. For example, in the Feed Through Mode the device only needs to be powered up and a few paths selected.

This mode enables the ISD5100 Series to connect to a cellular or cordless base band phone chip set without affecting the audio source or destination. There are two paths involved, the transmit path and the receive path. The transmit path connects the Nuvoton chip's microphone source through to the microphone input on the base band chip set. The receive path connects the base band chip set's speaker output through to the speaker driver on the Nuvoton chip. This allows the Nuvoton chip to substitute for those functions and incidentally gain access to the audio to and from the base band chip set.

To set up the environment described above, a series of commands need to be sent to the ISD5100-Series. First, the chip needs to be powered up as described in this section. Then the Configuration Registers must be filled with the specific data to connect the paths desired. In the case of the Feed Through Mode, most of the chip can remain powered down. The following figure illustrates the affected paths.



The figure above shows the part of the ISD5100 Series block diagram that is used in Feed Through Mode. The rest of the chip will be powered down to conserve power. The bold lines highlight the audio paths. Note that the Microphone to ANA OUT +/- path is differential.

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To select this mode, the following control bits must be configured in the ISD5100 Series configuration registers. To set up the transmit path:

1. Select the FTHRU path through the ANA OUT MUX—Bits AOS0, AOS1 and AOS2 control the state of the ANA OUT MUX. These are the D6, D7 and D8 bits respectively of Configuration Register 0 (CFG0) and they should all be ZERO to select the FTHRU path.
2. Power up the ANA OUT amplifier—Bit AOPD controls the power up state of ANA OUT. This is bit D5 of CFG0 and it should be a ZERO to power up the amplifier.

To set up the receive path:

1. Set up the ANA IN amplifier for the correct gain—Bits AIG0 and AIG1 control the gain settings of this amplifier. These are bits D14 and D15 respectively of CFG0. The input level at this pin determines the setting of this gain stage. The [ANA IN Amplifier Gain Settings table](#) on page 36 will help determine this setting. In this example, we will assume that the peak signal never goes above 1 volt p-p single ended. That would enable us to use the 9 dB attenuation setting, or where D14 is ONE and D15 is ZERO.
2. Power up the ANA IN amplifier—Bit AIPD controls the power up state of ANA IN. This is bit D13 of CFG0 and should be a ZERO to power up the amplifier.
3. Select the ANA IN path through the OUTPUT MUX—Bits OPS0 and OPS1 control the state of the OUTPUT MUX. These are bits D3 and D4 respectively of CFG0 and they should be set to the state where D3 is ONE and D4 is ZERO to select the ANA IN path.
4. Power up the Speaker Amplifier—Bits OPA0 and OPA1 control the state of the Speaker and AUX amplifiers. These are bits D1 and D2 respectively of CFG0. They should be set to the state where D1 is ONE and D2 is ZERO. This powers up the Speaker Amplifier and configures it for its higher gain setting for use with a piezo speaker element and also powers down the AUX output stage.

The status of the rest of the functions in the ISD5100 Series chip must be defined before the configuration registers settings are updated:

1. Power down the Volume Control Element—Bit VLPD controls the power up state of the Volume Control. This is bit D0 of CFG0 and it should be set to a ONE to power down this stage.
2. Power down the AUX IN amplifier—Bit AXPD controls the power up state of the AUX IN input amplifier. This is bit D10 of CFG0 and it should be set to a ONE to power down this stage.
3. Power down the SUM1 and SUM2 Mixer amplifiers—Bits S1M0 and S1M1 control the SUM1 mixer and bits S2M0 and S2M1 control the SUM2 mixer. These are bits D7 and D8 in CFG1 and bits D5 and D6 in CFG1 respectively. All 4 bits should be set to a ONE to power down these two amplifiers.
4. Power down the FILTER stage—Bit FLPD controls the power up state of the FILTER stage in the device. This is bit D1 in CFG1 and should be set to a ONE to power down the stage.
5. Power down the AGC amplifier—Bit AGPD controls the power up state of the AGC amplifier. This is bit D0 in CFG1 and should be set to a ONE to power down this stage.

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6. Don't Care bits—The following stages are not used in Feed Through Mode. Their bits may be set to either level. In this example, we will set all the following bits to a ZERO. (a). Bit INS0, bit D9 of CFG0 controls the Input Source Mux. (b). Bits AXG0 and AXG1 are bits D11 and D12 respectively in CFG0. They control the AUX IN amplifier gain setting. (c). Bits FLD0 and FLD1 are bits D2 and D3 respectively in CFG1. They control the sample rate and filter band pass setting. (d). Bit FLS0 is bit D4 in CFG1. It controls the FILTER MUX. (e). Bits S1S0 and S1S1 are bits D9 and D10 of CFG1. They control the SUM1 MUX. (f). Bits VOL0, VOL1 and VOL2 are bits D11, D12 and D13 of CFG1. They control the setting of the Volume Control. (g). Bits VLS0 and VLS1 are bits D14 and D15 of CFG1. They control the Volume Control MUX.

The end result of the above set up is

CFG0=0100 0100 0000 1011 (hex 440B)

and

CFG1=0000 0001 1110 0011 (hex 01E3).

Since both registers are being loaded, CFG0 is loaded, followed by the loading of CFG1. These two registers must be loaded in this order. The internal set up for both registers will take effect synchronously with the rising edge of SCL.

6.3.8 Call Record

The call record mode adds the ability to record an incoming phone call. In most applications, the ISD5100 Series would first be set up for Feed Through Mode as described above. When the user wishes to record the incoming call, the setup of the chip is modified to add that ability. For the purpose of this explanation, we will use the 6.4 kHz sample rate during recording.

The block diagram of the ISD5100 Series shows that the Multilevel Storage array is always driven from the SUM2 SUMMING amplifier. The path traces back from there through the LOW PASS Filter, THE FILTER MUX, THE SUM1 SUMMING amplifier, the SUM1 MUX, then from the ANA in amplifier. Feed Through Mode has already powered up the ANA IN amp so we only need to power up and enable the path to the Multilevel Storage array from that point:

1. Select the ANA IN path through the SUM1 MUX—Bits S1S0 and S1S1 control the state of the SUM1 MUX. These are bits D9 and D10 respectively of CFG1 and they should be set to the state where both D9 and D10 are ZERO to select the ANA IN path.
2. Select the SUM1 MUX input (only) to the S1 SUMMING amplifier—Bits S1M0 and S1M1 control the state of the SUM1 SUMMING amplifier. These are bits D7 and D8 respectively of CFG1 and they should be set to the state where D7 is ONE and D8 is ZERO to select the SUM1 MUX (only) path.

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3. Select the SUM1 SUMMING amplifier path through the FILTER MUX—Bit FLS0 controls the state of the FILTER MUX. This is bit D4 of CFG1 and it must be set to ZERO to select the SUM1 SUMMING amplifier path.
4. Power up the LOW PASS FILTER—Bit FLPD controls the power up state of the LOW PASS FILTER stage. This is bit D1 of CFG1 and it must be set to ZERO to power up the LOW PASS FILTER STAGE.
5. Select the 6.4 kHz sample rate—Bits FLD0 and FLD1 select the Low Pass filter setting and sample rate to be used during record and playback. These are bits D2 and D3 of CFG1. To enable the 6.4 kHz sample rate, D2 must be set to ONE and D3 set to ZERO.
6. Select the LOW PASS FILTER input (only) to the S2 SUMMING amplifier—Bits S2M0 and S2M1 control the state of the SUM2 SUMMING amplifier. These are bits D5 and D6 respectively of CFG1 and they should be set to the state where D5 is ZERO and D6 is ONE to select the LOW PASS FILTER (only) path.

In this mode, the elements of the original PASS THROUGH mode do not change. The sections of the chip not required to add the record path remain powered down. In fact, CFG0 does not change and remains

CFG0=0100 0100 0000 1011 (hex 440B).

CFG1 changes to

CFG1=0000 0000 1100 0101 (hex 00C5).

Since CFG0 is not changed, it is only necessary to load CFG1. Note that if only CFG0 was changed, it would be necessary to load both registers.

6.3.9 Memo Record

The Memo Record mode sets the chip up to record from the local microphone into the chip's Multilevel Storage Array. A connected cellular telephone or cordless phone chip set may remain powered down and is not active in this mode. The path to be used is microphone input to AGC amplifier, then through the INPUT SOURCE MUX to the SUM1 SUMMING amplifier. From there the path goes through the FILTER MUX, the LOW PASS FILTER, the SUM2 SUMMING amplifier, then to the MULTILEVEL STORAGE ARRAY. In this instance, we will select the 5.3 kHz sample rate. The rest of the chip may be powered down.

1. Power up the AGC amplifier—Bit AGPD controls the power up state of the AGC amplifier. This is bit D0 of CFG1 and must be set to ZERO to power up this stage.
2. Select the AGC amplifier through the INPUT SOURCE MUX—Bit INS0 controls the state of the INPUT SOURCE MUX. This is bit D9 of CFG0 and must be set to a ZERO to select the AGC amplifier.
3. Select the INPUT SOURCE MUX (only) to the S1 SUMMING amplifier—Bits S1M0 and S1M1 control the state of the SUM1 SUMMING amplifier. These are bits D7 and D8 respectively of CFG1 and they should be set to the state where D7 is ZERO and D8 is ONE to select the INPUT SOURCE MUX (only) path.

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4. Select the SUM1 SUMMING amplifier path through the FILTER MUX—Bit FLS0 controls the state of the FILTER MUX. This is bit D4 of CFG1 and it must be set to ZERO to select the SUM1 SUMMING amplifier path.
5. Power up the LOW PASS FILTER—Bit FLPD controls the power up state of the LOW PASS FILTER stage. This is bit D1 of CFG1 and it must be set to ZERO to power up the LOW PASS FILTER STAGE.
6. Select the 5.3 kHz sample rate—Bits FLD0 and FLD1 select the Low Pass filter setting and sample rate to be used during record and playback. These are bits D2 and D3 of CFG1. To enable the 5.3 kHz sample rate, D2 must be set to ZERO and D3 set to ONE.
7. Select the LOW PASS FILTER input (only) to the S2 SUMMING amplifier—Bits S2M0 and S2M1 control the state of the SUM2 SUMMING amplifier. These are bits D5 and D6 respectively of CFG1 and they should be set to the state where D5 is ZERO and D6 is ONE to select the LOW PASS FILTER (only) path.

To set up the chip for Memo Record, the configuration registers are set up as follows:

CFG0=0010 0100 0010 0001 (hex 2421).

CFG1=0000 0001 0100 1000 (hex 0148).

Only those portions necessary for this mode are powered up.

6.3.10 Memo and Call Playback

This mode sets the chip up for local playback of messages recorded earlier. The playback path is from the MULTILEVEL STORAGE ARRAY to the FILTER MUX, then to the LOW PASS FILTER stage. From there, the audio path goes through the SUM2 SUMMING amplifier to the VOLUME MUX, through the VOLUME CONTROL then to the SPEAKER output stage. We will assume that we are driving a piezo speaker element. This audio was previously recorded at 8 kHz. All unnecessary stages will be powered down.

1. Select the MULTILEVEL STORAGE ARRAY path through the FILTER MUX—Bit FLS0, the state of the FILTER MUX. This is bit D4 of CFG1 and must be set to ONE to select the MULTILEVEL STORAGE ARRAY.
2. Power up the LOW PASS FILTER—Bit FLPD controls the power up state of the LOW PASS FILTER stage. This is bit D1 of CFG1 and it must be set to ZERO to power up the LOW PASS FILTER STAGE.
3. Select the 8.0 kHz sample rate—Bits FLD0 and FLD1 select the Low Pass filter setting and sample rate to be used during record and playback. These are bits D2 and D3 of CFG1. To enable the 8.0 kHz sample rate, D2 and D3 must be set to ZERO.
4. Select the LOW PASS FILTER input (only) to the S2 SUMMING amplifier —Bits S2M0 and S2M1 control the state of the SUM2 SUMMING amplifier. These are bits D5 and D6 respectively of CFG1 and they should be set to the state where D5 is ZERO and D6 is ONE to select the LOW PASS FILTER (only) path.

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5. Select the SUM2 SUMMING amplifier path through the VOLUME MUX—Bits VLS0 and VLS1 control the state VOLUME MUX. These bits are bits D14 and D15, respectively of CFG1. They should be set to the state where D14 is ONE and D15 is ZERO to select the SUM2 SUMMING amplifier.
6. Power up the VOLUME CONTROL LEVEL—Bit VLPD controls the power-up state of the VOLUME CONTROL attenuator. This is Bit D0 of CFG0. This bit must be set to a ZERO to power-up the VOLUME CONTROL.
7. Select a VOLUME CONTROL LEVEL—Bits VOL0, VOL1, and VOL2 control the state of the VOLUME CONTROL LEVEL. These are bits D11, D12, and D13, respectively, of CFG1. A binary count of 000 through 111 controls the amount of attenuation through that state. In most cases, the software will select an attenuation level according to the desires of the current users of the product. In this example, we will assume the user wants an attenuation of -12 dB. For that setting, D11 should be set to ONE, D12 should be set to ONE, and D13 should be set to a ZERO.
8. Select the VOLUME CONTROL path through the OUTPUT MUX—These are bits D3 and D4, respectively, of CFG0. They should be set to the state where D3 is ZERO and D4 is a ZERO to select the VOLUME CONTROL.
9. Power up the SPEAKER amplifier and select the HIGH GAIN mode—Bits OPA0 and OPA1 control the state of the speaker (SP+ and SP-) and AUX OUT outputs. These are bits D1 and D2 of CFG0. They must be set to the state where D1 is ONE and D2 is ZERO to power-up the speaker outputs in the HIGH GAIN mode and to power-down the AUX OUT.

To set up the chip for Memo or Call Playback, the configuration registers are set up as follows:

CFG0=0010 0100 0010 0100 (hex 2424).

CFG1=0101 1001 1101 0001 (hex 59D1).

Only those portions necessary for this mode are powered up.

6.3.11 Message Cueing

Message cueing allows the user to skip through analog messages without knowing the actual physical location of the message. This operation is used during playback. In this mode, the messages are skipped 512 times faster than in normal playback mode. It will stop when an EOM marker is reached. Then, the internal address counter will be pointing to the next message.

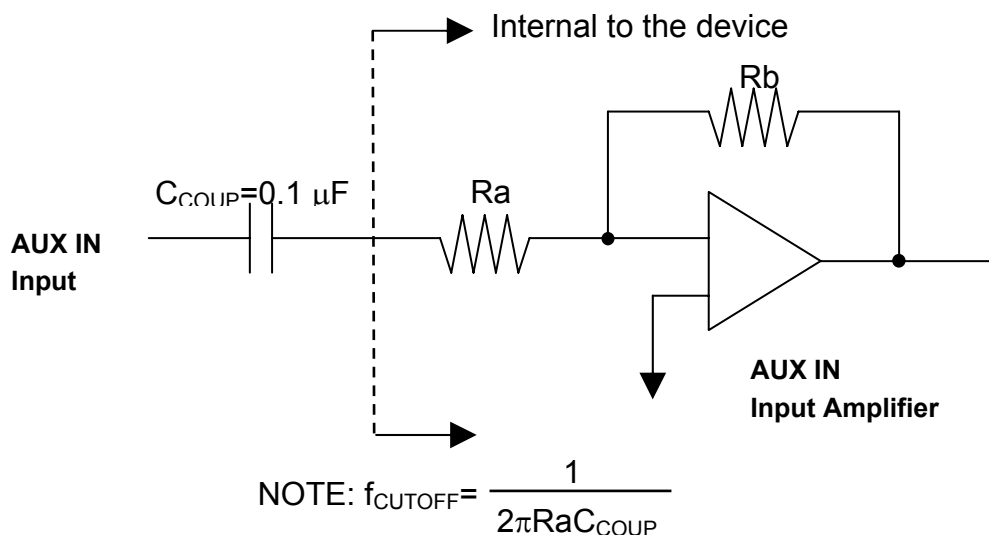
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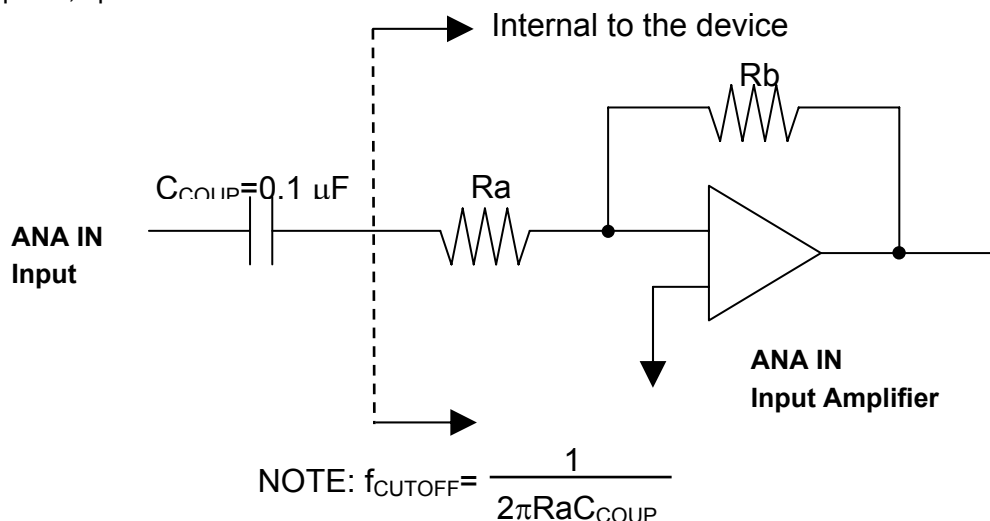
6.4. ANALOG MODE

6.4.1 Aux In and Ana In Description

The AUX IN is an additional audio input to the ISD5100-Series, such as from the microphone circuit in a mobile phone “car kit.” This input has a nominal 694 mV p-p level at its minimum gain setting (0 dB). See the [AUX IN Amplifier Gain Settings table](#) on page 37. Additional gain is available in 3 dB steps (controlled by the I²C serial interface) up to 9 dB.



The ANA IN pin is the analog input from the telephone chip set. It can be switched (by the serial bus) to the speaker output, the array input or to various other paths. This pin is designed to accept a nominal 1.11 V_{p-p} when at its minimum gain (6 dB) setting. See the [ANA IN Amplifier Gain Settings table](#) on page 37. There is additional gain available in 3 dB steps controlled from the I²C interface, if required, up to 15 dB.

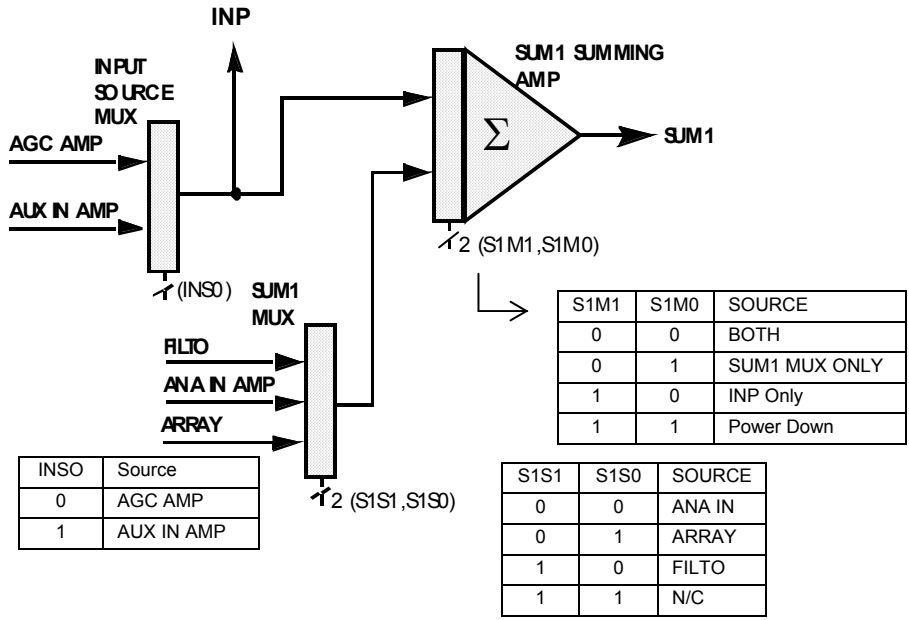


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6.4.2 ISD5100 Series Analog Structure (left half) Description

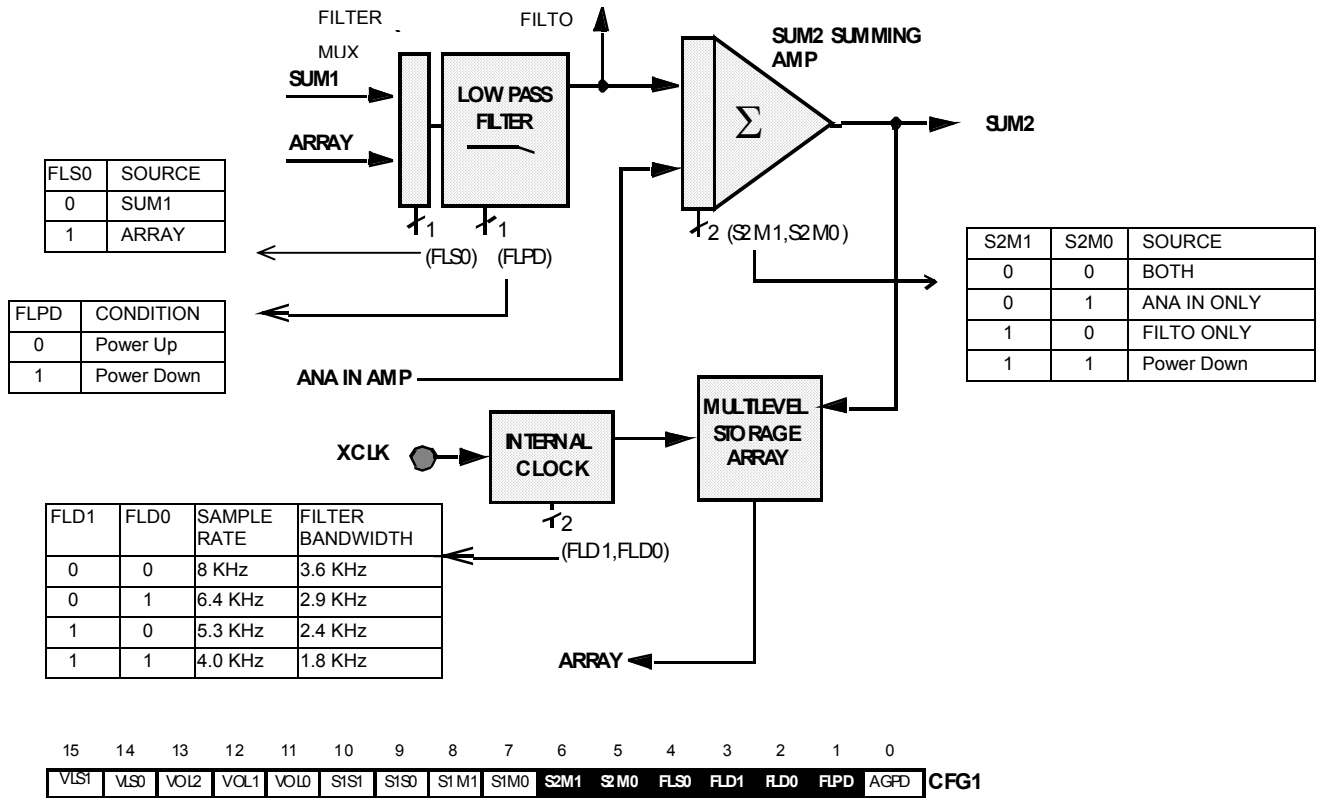


15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	C FG 0
AIG1	AIG0	AIFD	AXG1	AXG0	AXPD	INS0	ACSZ	AOSI	AOS0	AOPD	OPSI	OPSO	OPA1	OPA0	VLPD	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	C FG 1
VLS1	VLS0	VOL2	VOL1	VOL0	S1S1	S1S0	S1M1	S1M0	S2M1	S2M0	FLS0	FLD1	FLD0	FLPD	AGPD	

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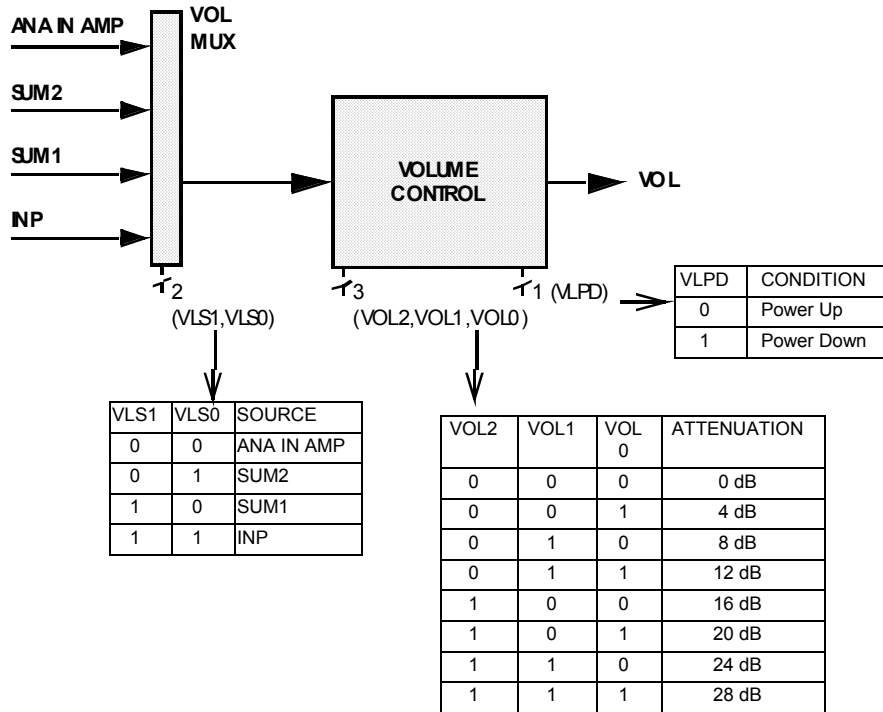
6.4.3 ISD5100 Series Analog Structure (right half) Description



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6.4.4 Volume Control Description

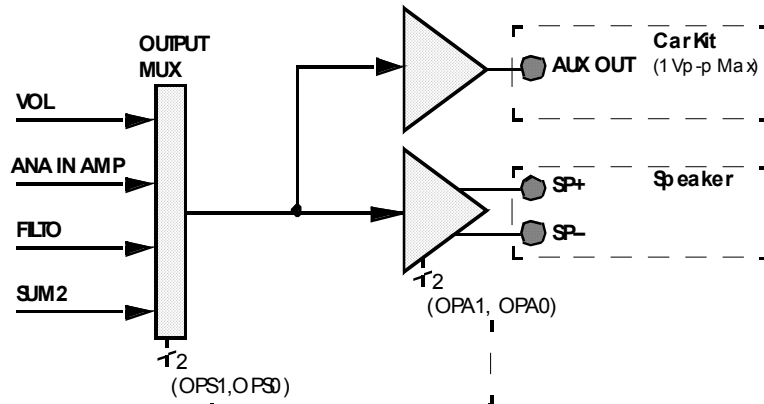


CFG1	AGP0	AGP1	AGP2	AGP3	AGP4	AGP5	AGP6	AGP7	AGP8	AGP9	AGP10	AGP11	AGP12	AGP13	AGP14	AGP15	AGP16	AGP17	AGP18	AGP19	AGP20	AGP21	AGP22	AGP23	AGP24	AGP25	AGP26	AGP27	AGP28	AGP29	AGP30	AGP31	AGP32	AGP33	AGP34	AGP35	AGP36	AGP37	AGP38	AGP39	AGP40	AGP41	AGP42	AGP43	AGP44	AGP45	AGP46	AGP47	AGP48	AGP49	AGP50	AGP51	AGP52	AGP53	AGP54	AGP55	AGP56	AGP57	AGP58	AGP59	AGP60	AGP61	AGP62	AGP63	AGP64	AGP65	AGP66	AGP67	AGP68	AGP69	AGP70	AGP71	AGP72	AGP73	AGP74	AGP75	AGP76	AGP77	AGP78	AGP79	AGP80	AGP81	AGP82	AGP83	AGP84	AGP85	AGP86	AGP87	AGP88	AGP89	AGP90	AGP91	AGP92	AGP93	AGP94	AGP95	AGP96	AGP97	AGP98	AGP99	AGP100	AGP101	AGP102	AGP103	AGP104	AGP105	AGP106	AGP107	AGP108	AGP109	AGP110	AGP111	AGP112	AGP113	AGP114	AGP115	AGP116	AGP117	AGP118	AGP119	AGP120	AGP121	AGP122	AGP123	AGP124	AGP125	AGP126	AGP127	AGP128	AGP129	AGP130	AGP131	AGP132	AGP133	AGP134	AGP135	AGP136	AGP137	AGP138	AGP139	AGP140	AGP141	AGP142	AGP143	AGP144	AGP145	AGP146	AGP147	AGP148	AGP149	AGP150	AGP151	AGP152	AGP153	AGP154	AGP155	AGP156	AGP157	AGP158	AGP159	AGP160	AGP161	AGP162	AGP163	AGP164	AGP165	AGP166	AGP167	AGP168	AGP169	AGP170	AGP171	AGP172	AGP173	AGP174	AGP175	AGP176	AGP177	AGP178	AGP179	AGP180	AGP181	AGP182	AGP183	AGP184	AGP185	AGP186	AGP187	AGP188	AGP189	AGP190	AGP191	AGP192	AGP193	AGP194	AGP195	AGP196	AGP197	AGP198	AGP199	AGP200	AGP201	AGP202	AGP203	AGP204	AGP205	AGP206	AGP207	AGP208	AGP209	AGP210	AGP211	AGP212	AGP213	AGP214	AGP215	AGP216	AGP217	AGP218	AGP219	AGP220	AGP221	AGP222	AGP223	AGP224	AGP225	AGP226	AGP227	AGP228	AGP229	AGP230	AGP231	AGP232	AGP233	AGP234	AGP235	AGP236	AGP237	AGP238	AGP239	AGP240	AGP241	AGP242	AGP243	AGP244	AGP245	AGP246	AGP247	AGP248	AGP249	AGP250	AGP251	AGP252	AGP253	AGP254	AGP255	AGP256	AGP257	AGP258	AGP259	AGP260	AGP261	AGP262	AGP263	AGP264	AGP265	AGP266	AGP267	AGP268	AGP269	AGP270	AGP271	AGP272	AGP273	AGP274	AGP275	AGP276	AGP277	AGP278	AGP279	AGP280	AGP281	AGP282	AGP283	AGP284	AGP285	AGP286	AGP287	AGP288	AGP289	AGP290	AGP291	AGP292	AGP293	AGP294	AGP295	AGP296	AGP297	AGP298	AGP299	AGP300	AGP301	AGP302	AGP303	AGP304	AGP305	AGP306	AGP307	AGP308	AGP309	AGP310	AGP311	AGP312	AGP313	AGP314	AGP315	AGP316	AGP317	AGP318	AGP319	AGP320	AGP321	AGP322	AGP323	AGP324	AGP325	AGP326	AGP327	AGP328	AGP329	AGP330	AGP331	AGP332	AGP333	AGP334	AGP335	AGP336	AGP337	AGP338	AGP339	AGP340	AGP341	AGP342	AGP343	AGP344	AGP345	AGP346	AGP347	AGP348	AGP349	AGP350	AGP351	AGP352	AGP353	AGP354	AGP355	AGP356	AGP357	AGP358	AGP359	AGP360	AGP361	AGP362	AGP363	AGP364	AGP365	AGP366	AGP367	AGP368	AGP369	AGP370	AGP371	AGP372	AGP373	AGP374	AGP375	AGP376	AGP377	AGP378	AGP379	AGP380	AGP381	AGP382	AGP383	AGP384	AGP385	AGP386	AGP387	AGP388	AGP389	AGP390	AGP391	AGP392	AGP393	AGP394	AGP395	AGP396	AGP397	AGP398	AGP399	AGP400	AGP401	AGP402	AGP403	AGP404	AGP405	AGP406	AGP407	AGP408	AGP409	AGP410	AGP411	AGP412	AGP413	AGP414	AGP415	AGP416	AGP417	AGP418	AGP419	AGP420	AGP421	AGP422	AGP423	AGP424	AGP425	AGP426	AGP427	AGP428	AGP429	AGP430	AGP431	AGP432	AGP433	AGP434	AGP435	AGP436	AGP437	AGP438	AGP439	AGP440	AGP441	AGP442	AGP443	AGP444	AGP445	AGP446	AGP447	AGP448	AGP449	AGP450	AGP451	AGP452	AGP453	AGP454	AGP455	AGP456	AGP457	AGP458	AGP459	AGP460	AGP461	AGP462	AGP463	AGP464	AGP465	AGP466	AGP467	AGP468	AGP469	AGP470	AGP471	AGP472	AGP473	AGP474	AGP475	AGP476	AGP477	AGP478	AGP479	AGP480	AGP481	AGP482	AGP483	AGP484	AGP485	AGP486	AGP487	AGP488	AGP489	AGP490	AGP491	AGP492	AGP493	AGP494	AGP495	AGP496	AGP497	AGP498	AGP499	AGP500	AGP501	AGP502	AGP503	AGP504	AGP505	AGP506	AGP507	AGP508	AGP509	AGP510	AGP511	AGP512	AGP513	AGP514	AGP515	AGP516	AGP517	AGP518	AGP519	AGP520	AGP521	AGP522	AGP523	AGP524	AGP525	AGP526	AGP527	AGP528	AGP529	AGP530	AGP531	AGP532	AGP533	AGP534	AGP535	AGP536	AGP537	AGP538	AGP539	AGP540	AGP541	AGP542	AGP543	AGP544	AGP545	AGP546	AGP547	AGP548	AGP549	AGP550	AGP551	AGP552	AGP553	AGP554	AGP555	AGP556	AGP557	AGP558	AGP559	AGP560	AGP561	AGP562	AGP563	AGP564	AGP565	AGP566	AGP567	AGP568	AGP569	AGP570	AGP571	AGP572	AGP573	AGP574	AGP575	AGP576	AGP577	AGP578	AGP579	AGP580	AGP581	AGP582	AGP583	AGP584	AGP585	AGP586	AGP587	AGP588	AGP589	AGP590	AGP591	AGP592	AGP593	AGP594	AGP595	AGP596	AGP597	AGP598	AGP599	AGP600	AGP601	AGP602	AGP603	AGP604	AGP605	AGP606	AGP607	AGP608	AGP609	AGP610	AGP611	AGP612	AGP613	AGP614	AGP615	AGP616	AGP617	AGP618	AGP619	AGP620	AGP621	AGP622	AGP623	AGP624	AGP625	AGP626	AGP627	AGP628	AGP629	AGP630	AGP631	AGP632	AGP633	AGP634	AGP635	AGP636	AGP637	AGP638	AGP639	AGP640	AGP641	AGP642	AGP643	AGP644	AGP645	AGP646	AGP647	AGP648	AGP649	AGP650	AGP651	AGP652	AGP653	AGP654	AGP655	AGP656	AGP657	AGP658	AGP659	AGP660	AGP661	AGP662	AGP663	AGP664	AGP665	AGP666	AGP667	AGP668	AGP669	AGP670	AGP671	AGP672	AGP673	AGP674	AGP675	AGP676	AGP677	AGP678	AGP679	AGP680	AGP681	AGP682	AGP683	AGP684	AGP685	AGP686	AGP687	AGP688	AGP689	AGP690	AGP691	AGP692	AGP693	AGP694	AGP695	AGP696	AGP697	AGP698	AGP699	AGP700	AGP701	AGP702	AGP703	AGP704	AGP705	AGP706	AGP707	AGP708	AGP709	AGP710	AGP711	AGP712	AGP713	AGP714	AGP715	AGP716	AGP717	AGP718	AGP719	AGP720	AGP721	AGP722	AGP723	AGP724	AGP725	AGP726	AGP727	AGP728	AGP729	AGP730	AGP731	AGP732	AGP733	AGP734	AGP735	AGP736	AGP737	AGP738	AGP739	AGP740	AGP741	AGP742	AGP743	AGP744	AGP745	AGP746	AGP747	AGP748	AGP749	AGP750	AGP751	AGP752	AGP753	AGP754	AGP755	AGP756	AGP757	AGP758	AGP759	AGP760	AGP761	AGP762	AGP763	AGP764	AGP765	AGP766	AGP767	AGP768	AGP769	AGP770	AGP771	AGP772	AGP773	AGP774	AGP775	AGP776	AGP777	AGP778	AGP779	AGP780	AGP781	AGP782	AGP783	AGP784	AGP785	AGP786	AGP787	AGP788	AGP789	AGP790	AGP791	AGP792	AGP793	AGP794	AGP795	AGP796	AGP797	AGP798	AGP799	AGP800	AGP801	AGP802	AGP803	AGP804	AGP805	AGP806	AGP807	AGP808	AGP809	AGP810	AGP811	AGP812	AGP813	AGP814	AGP815	AGP816	AGP817	AGP818	AGP819	AGP820	AGP821	AGP822	AGP823	AGP824	AGP825	AGP826	AGP827	AGP828	AGP829	AGP830	AGP831	AGP832	AGP833	AGP834	AGP835	AGP836	AGP837	AGP838	AGP839	AGP840	AGP841	AGP842	AGP843	AGP844	AGP845	AGP846	AGP847	AGP848	AGP849	AGP850	AGP851	AGP852	AGP853	AGP854	AGP855	AGP856	AGP857	AGP858	AGP859	AGP860	AGP861	AGP862	AGP863	AGP864	AGP865	AGP866	AGP867	AGP868	AGP869	AGP870	AGP871	AGP872	AGP873	AGP874	AGP875	AGP876	AGP877	AGP878	AGP879	AGP880	AGP881	AGP882	AGP883	AGP884	AGP885	AGP886	AGP887	AGP888	AGP889	AGP890	AGP891	AGP892	AGP893	AGP894	AGP895	AGP896	AGP897	AGP898	AGP899	AGP900	AGP901	AGP902	AGP903	AGP904	AGP905	AGP906	AGP907	AGP908	AGP909	AGP910	AGP911	AGP912	AGP913	AGP914	AGP915	AGP916	AGP917	AGP918	AGP919	AGP920	AGP921	AGP922	AGP923	AGP924	AGP925	AGP926	AGP927	AGP928	AGP929	AGP930	AGP931	AGP932	AGP933	AGP934	AGP935	AGP936	AGP937	AGP938	AGP939	AGP940	AGP941	AGP942	AGP943	AGP944	AGP945	AGP946	AGP947	AGP948	AGP949	AGP950	AGP951	AGP952	AGP953	AGP954	AGP955	AGP956	AGP957	AGP958	AGP959	AGP960	AGP961	AGP962	AGP963	AGP964	AGP965	AGP966	AGP967	AGP968	AGP969	AGP970	AGP971	AGP972	AGP973	AGP974	AGP975	AGP976	AGP977	AGP978	AGP979	AGP980	AGP981	AGP982	AGP983	AGP984	AGP985	AGP986	AGP987	AGP988	AGP989	AGP990	AGP991	AGP992	AGP993	AGP994	AGP995	AGP996	AGP997	AGP998	AGP999	AGP1000	AGP1001	AGP1002	AGP1003	AGP1004	AGP1005	AGP1006	AGP1007	AGP1008	AGP1009	AGP1010	AGP1011	AGP1012	AGP1013	AGP1014	AGP1015	AGP1016	AGP1017	AGP1018	AGP1019	AGP1020	AGP1021	AGP1022	AGP1023	AGP1024	AGP1025	AGP1026	AGP1027	AGP1028	AGP1029	AGP1
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ISD5100 SERIES



6.4.5 Speaker and Aux Out Description



OPS1	OPS0	SOURCE
0	0	VOL
0	1	ANA IN
1	0	FILTO
1	1	SUM2

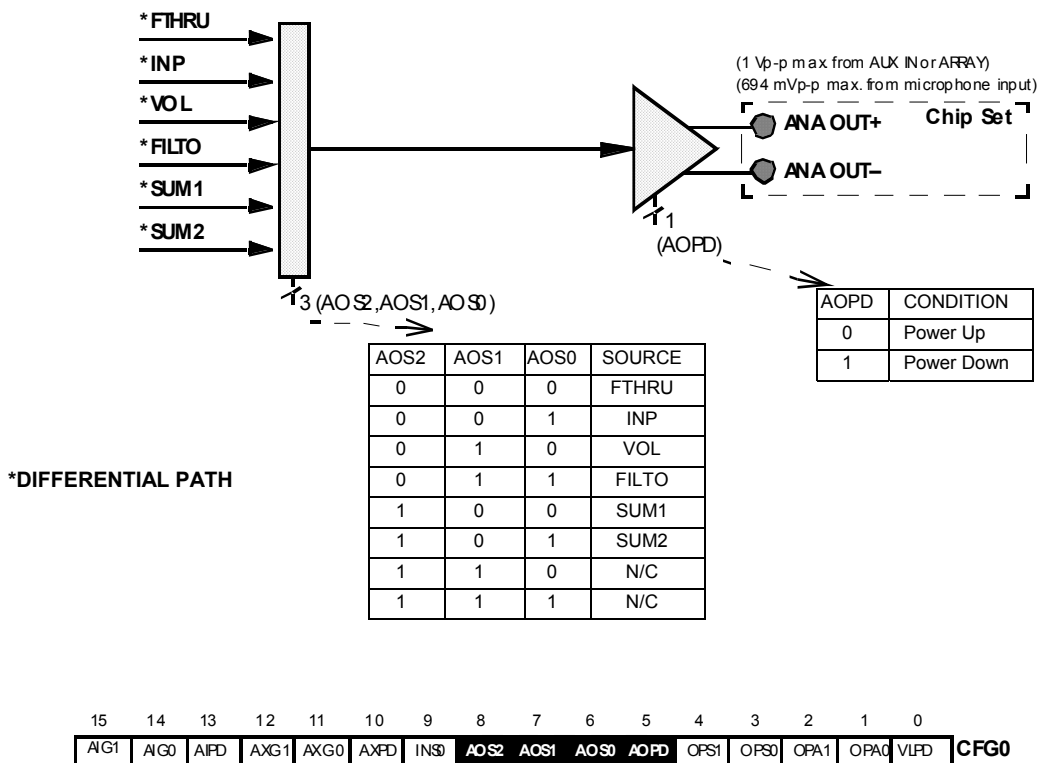
OPA1	OPA0	SPKR DRIVE	AUX OUT
0	0	Power Down	Power Down
0	1	3.6 V _{P-P} @ 150 Ω	Power Down
1	0	23.5 mWatt @ 8 Ω	Power Down
1	1	Power Down	1 V _{P-P} Max @ 5 KΩ

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	CFG0
AIG1	AIG0	APD	AXG1	AXG0	AXPD	INS0	AOΣ	AOS1	AOS0	AOPD	OPS1	OPS0	OPA1	OPA0	VLPD	

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6.4.6 Ana Out Description



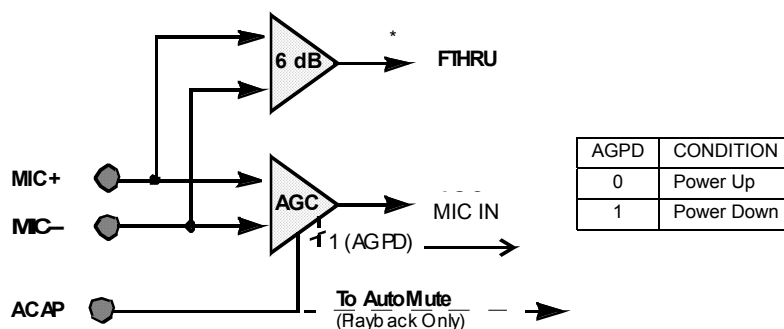
6.4.7 Analog Inputs

Microphone Inputs

The microphone inputs transfer the voice signal to the on-chip AGC preamplifier or directly to the ANA OUT MUX, depending on the selected path. The direct path to the ANA OUT MUX has a gain of 6 dB so a 208 mV p-p signal across the differential microphone inputs would give 416 mV p-p across the ANA OUT pins. The AGC circuit has a range of 45 dB in order to deliver a nominal 694 mV p-p into the storage array from a typical electric microphone output of 2 to 20 mV p-p. The input impedance is typically 10kΩ.

The ACAP pin provides the capacitor connection for setting the parameters of the microphone AGC circuit. It should have a 4.7 μF capacitor connected to ground. It cannot be left floating. This is because the capacitor is also used in the playback mode for the AutoMute circuit. This circuit reduces the amount of noise present in the output during quiet pauses. Tying this pin to ground gives maximum gain; to VCCA gives minimum gain for the AGC amplifier but will cancel the AutoMute function.

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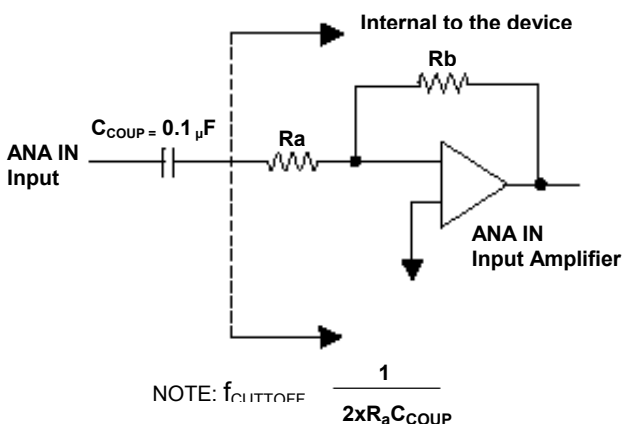
AGPD	CONDITION
0	Power Up
1	Power Down

* Differential Path

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
VL5	VL0	VOL2	VOL1	VL0	SL5	SL0	SIM1	SIM0	S2M1	S2M0	FL0	FLD1	FLD0	FLP	AGPD	CFG1

ANA IN (Analog Input)

The ANA IN pin is the analog input from the telephone chip set. It can be switched (by the I²C interface) to the speaker output, the array input or to various other paths. This pin is designed to accept a nominal 1.11 V p-p when at its minimum gain (6 dB) setting. There is additional gain available, if required, in 3 dB steps, up to 15 dB. The gain settings are controlled from the I²C interface.



Gain Setting	Resistor Ratio (Rb/Ra)	Gain	Gain ² (dB)
00	63.9 / 102	0.625	-4.1
01	77.9 / 88.1	0.883	-1.1
10	92.3 / 73.8	1.250	1.9
11	106 / 60	1.767	4.9

Note: Ra & Rb are in kΩ

ANA IN Amplifier Gain Settings

Setting ⁽¹⁾	OTLP Input V _{P-P} ⁽³⁾	CFG0		Gain ⁽²⁾	Array In/Out V _{P-P}	Speaker Out V _{P-P} ⁽⁴⁾
		AIG1	AIG0			
6 dB	1.110	0	0	0.625	0.694	2.22
9 dB	0.785	0	1	0.883	0.694	2.22
12 dB	0.555	1	0	1.250	0.694	2.22
15 dB	0.393	1	1	1.767	0.694	2.22

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Revision 1.42

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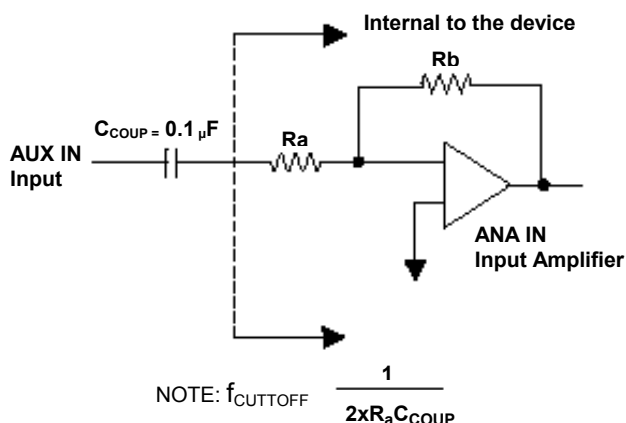
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1. Gain from ANA IN to SP+/-
2. Gain from ANA IN to ARRAY IN
3. 0TLP Input is the reference Transmission Level Point that is used for testing. This level is typically 3 dB below clipping
4. Speaker Out gain set to 1.6 (High). (Differential)

AUX IN (Auxiliary Input)

The AUX IN is an additional audio input to the ISD5100-Series, such as from the microphone circuit in a mobile phone "car kit." This input has a nominal 694 mV p-p level at its minimum gain setting (0 dB). See the following table. Additional gain is available in 3 dB steps (controlled by the I²C interface) up to 9 dB.

AUX IN Input Modes



Gain Setting	Resistor Ratio (Rb/Ra)	Gain	Gain ⁽²⁾ (dB)
00	40.1 / 40.1	1.0	0
01	47.0 / 33.2	1.414	3
10	53.5 / 26.7	2.0	6
11	59.2 / 21	2.82	9

Note: Ra & Rb are in kΩ

AUX IN Amplifier Gain Settings

Setting ⁽¹⁾	0TLP Input V _{P-P} ⁽³⁾	CFG0		Gain ⁽²⁾	Array In/Out V _{P-P}	Speaker Out V _{P-P} ⁽⁴⁾
		AXG1	AXG0			
0 dB	0.694	0	0	1.00	0.694	0.694
3 dB	0.491	0	1	1.41	0.694	0.694
6 dB	0.347	1	0	2.00	0.694	0.694
9 dB	0.245	1	1	2.82	0.694	0.694

1. Gain from AUX IN to ANA OUT
2. Gain from AUX IN to ARRAY IN
3. 0TLP Input is the reference Transmission Level Point that is used for testing. This level is typically 3 dB below clipping
4. Differential

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6.5. DIGITAL MODE

6.5.1 Erasing Digital Data

The Digital Erase command can only erase an entire page at a time. This means that the D1 command only needs to include the 11-bit page address; the 5-bit for block address are left at 00000.

Once a page has been erased, each block may be written separately, 64 bits at a time. But, if a block has been previously written then the entire page of 2048 bits must be erased in order to re-write (or change) a block.

A sequence might be look like:

- read the entire page
- store it in RAM
- change the desired bit(s)
- erase the page
- write the new data from RAM to the entire page

6.5.2 Writing Digital Data

The Digital Write function allows the user to select a portion of the array to be used as digital memory. The partition between analog and digital memory is left up to the user. A page can only be either Digital or Analog, but not both. The minimum addressable block of memory in the digital mode is one block or 64 bits, when reading or writing. The address sent to the device is the 11-bit row (or page) address with the 5-bit scan (or block) address. However, one must send a Digital Erase before attempting to change digital data on a page. This means that even when changing only one of the 32 blocks, all 32 blocks will need to be rewritten to the page. Command Sequence: The chip enters digital mode by sending the ENTER DIGITAL MODE command from power down. Send the DIGITAL WRITE @ ADDR command with the row address. After the address is entered, the data is sent in one-byte packets followed by an I²C acknowledge generated by the chip. Data for each block is sent MSB first. The data transfer is ended when the master generates an I²C STOP condition. If only a partial block of data is sent before the STOP condition, "zero" is written in the remaining bytes; that is, they are left at the erase level. An erased page (row) will be read as all zeros. The device can buffer up to two blocks of data. If the device is unable to accept more data due to the internal write process, the SCL line will be held LOW indicating to the master to halt data transfer. If the device encounters an overflow condition, it will respond by generating an interrupt condition and an I²C Not Acknowledge signal after the last valid byte of data. Once data transfer is terminated, the device needs up to two cycles (64 us) to complete its internal write cycle before another command is sent. If an active command is sent before the internal cycle is finished, the part will hold SCL LOW until the current command is finished. After writing is complete, send the EXIT DIGITAL MODE command.

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6.5.3 Reading Digital Data

The Digital Read command utilizes the combined I²C command format. That is, a command is sent to the chip using the write data direction. Then the data direction is reversed by sending a repeated start condition, and the slave address with R/W set to 1. After this, the slave device (ISD5100-Series) begins to send data to the master until the master generates a NACK. If the part encounters an overflow condition, the $\overline{\text{INT}}$ pin is pulled LOW. No other communication with the master is possible due to the master generating ACK signals.

Digital Write and Digital Read can be done a “block” at a time. Thus, only 64 bits need be read in each Digital Read command sequence.

6.5.4 Example Command Sequences

An explanation and graphical representation of the Erase, Write and Read operations are found below.

Note: All sequences assumes that the chip is in power-down mode before the commands are sent.

6.5.4.1. Erase Digital Data

Erase

=====

I2CStart

SendByte(0x80) - Write, Slave address zero

WaitACK

WaitSCLHigh

SendByte(0xc0) - Enter Digital Mode Command

WaitACK

WaitSCLHigh

I2CStop

I2CStart

SendByte(0x80) - Write, Slave address zero

WaitACK

WaitSCLHigh

SendByte(0xd1) - Digital Erase Command

WaitACK

WaitSCLHigh

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SendByte(row/256) - high address byte

WaitACK

WaitSCLHigh

SendByte(row%256) - low address byte

WaitACK

WaitSCLHigh

I2CStop

repeat until the number of RAC pulses are one less
than the number of rows to delete

```
{  
    wait RAC low  
    WAIT RAC high  
}
```

Note: If only one row is going to be erased,
send the following STOP command immediately after
ERASE command and skip the loop above

I2CStart

SendByte(0x80) - Write, Slave address zero

WaitACK

WaitSCLHigh

SendByte(0xc0) - Stop digital erase

WaitACK

WaitSCLHigh

I2CStop

wait until erase of the last row has completed

```
{  
    wait RAC low  
    WAIT RAC high  
}
```

I2CStart

SendByte(0x80) - Write, Slave address zero

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WaitACK

WaitSCLHigh

SendByte(0x40) - Exit Digital Mode Command

WaitACK

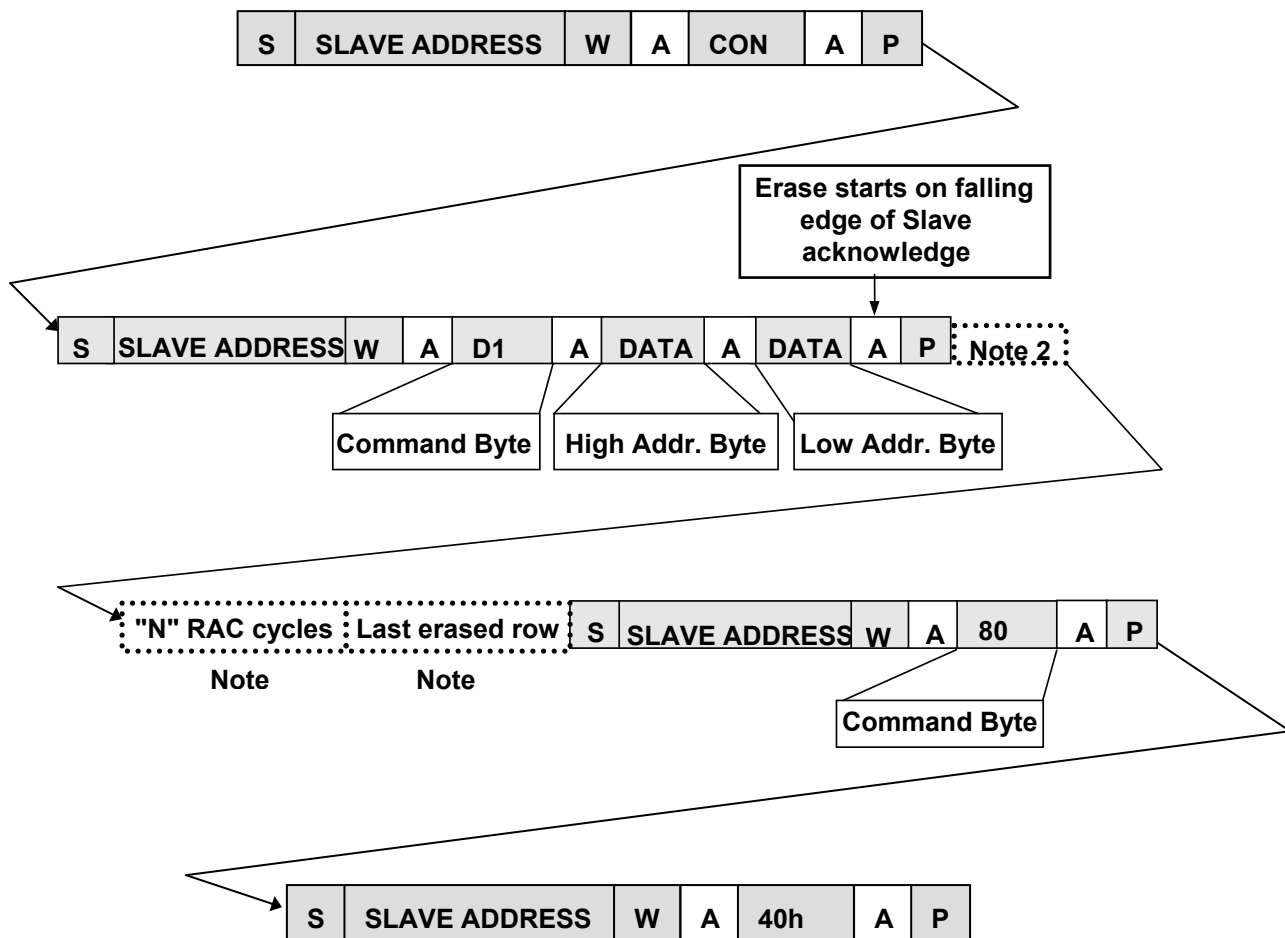
WaitSCLHigh

I2Cstop

Notes

1. Erase operations must be addressed on a Row boundary. The 5 LSB bits of the Low Address Byte will be ignored.
2. I²C bus is released while erase proceeds. Other devices may use the bus until it is time to execute the STOP command that causes the end of the Erase operation.
3. Host processor must count RAC cycles to determine where the chip is in the erase process, one row per RAC cycle. RAC pulses LOW for 0.25 millisecond at the end of each erased row. The erase of the "next" row begins with the rising edge of RAC. See the [Digital Erase RAC](#) timing diagram on page 51.
4. When the erase of the last desired row begins, the following STOP command (Command Byte = 80 hex) must be issued. This command must be completely given, including receiving the ACK from the Slave before the RAC pin goes HIGH at the end of the row.

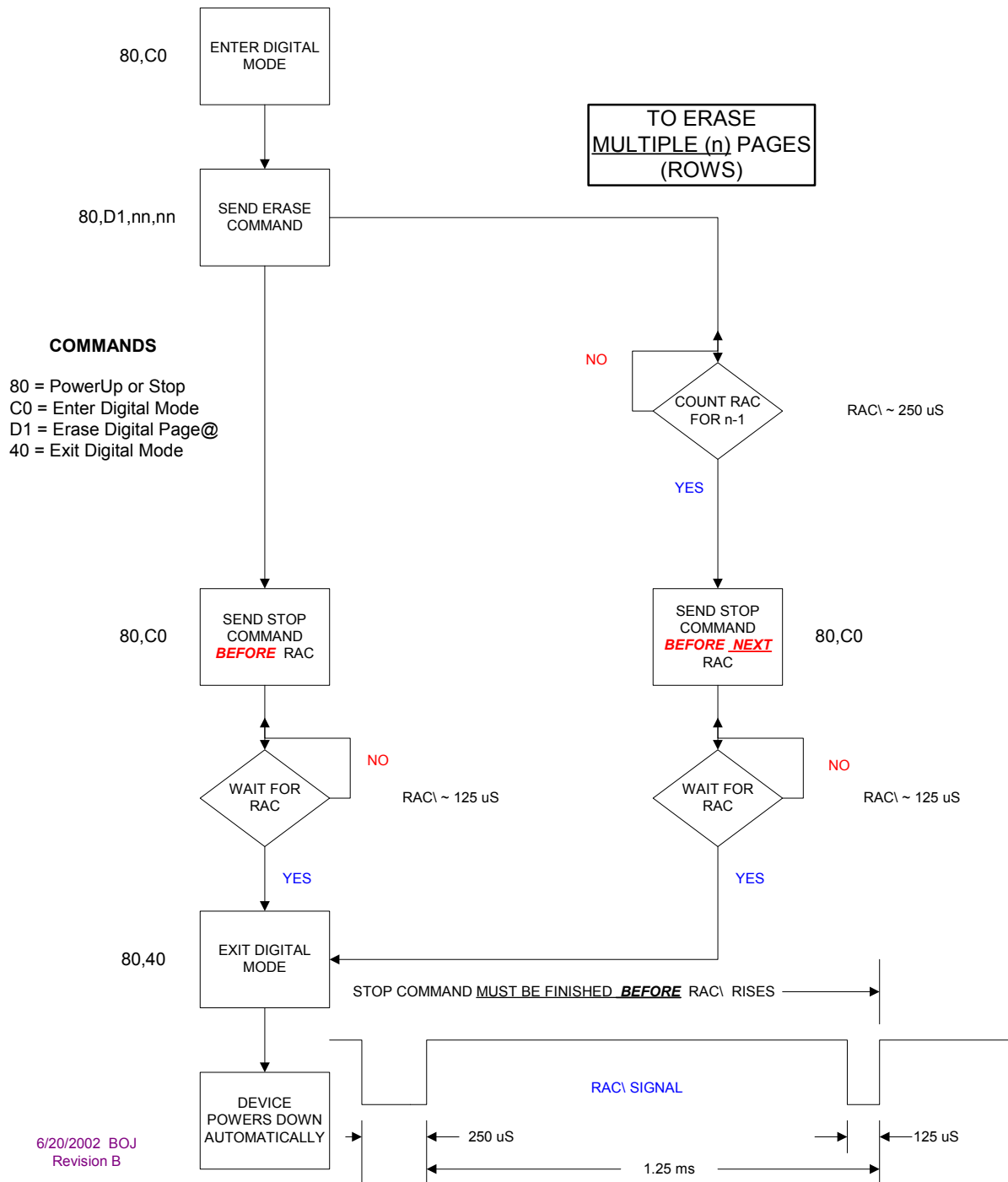
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SUGGESTED FLOW FOR DIGITAL ERASE IN ISD5100-Series



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6.5.4.2. Write Digital Data

Write

=====

I2CStart

SendByte(0x80) - Write, Slave address zero

WaitACK

WaitSCLHigh

SendByte(0xc0) - Enter Digital Mode Command

WaitACK

WaitSCLHigh

I2CStop

I2CStart

SendByte(0x80) - Write, Slave address zero

WaitACK

WaitSCLHigh

SendByte(0xc9) - Write Digital Data Command

WaitACK

WaitSCLHigh

SendByte(row/256) - high address byte

WaitACK

WaitSCLHigh

SendByte(row%256) - low address byte

WaitACK

WaitSCLHigh

repeat until all data is sent

{

 SendByte(data) - send data byte

 WaitACK()

 WaitSCLHigh()

}

I2CStop

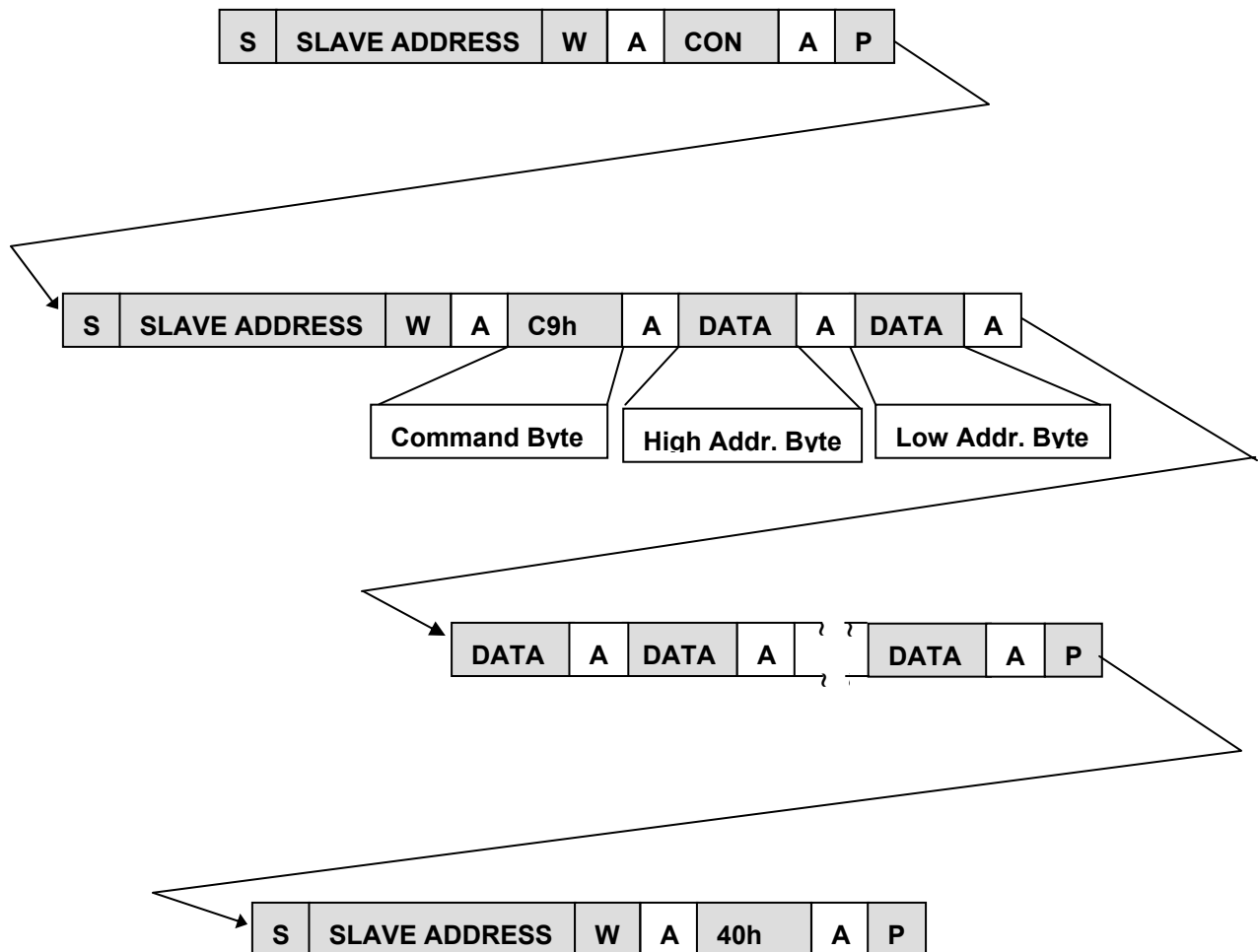
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I2CStart
 SendByte(0x80) - Write, Slave address zero
 WaitACK
 WaitSCLHigh
 SendByte(0x40) - Exit Digital Mode Command
 WaitACK
 WaitSCLHigh
 I2CStop



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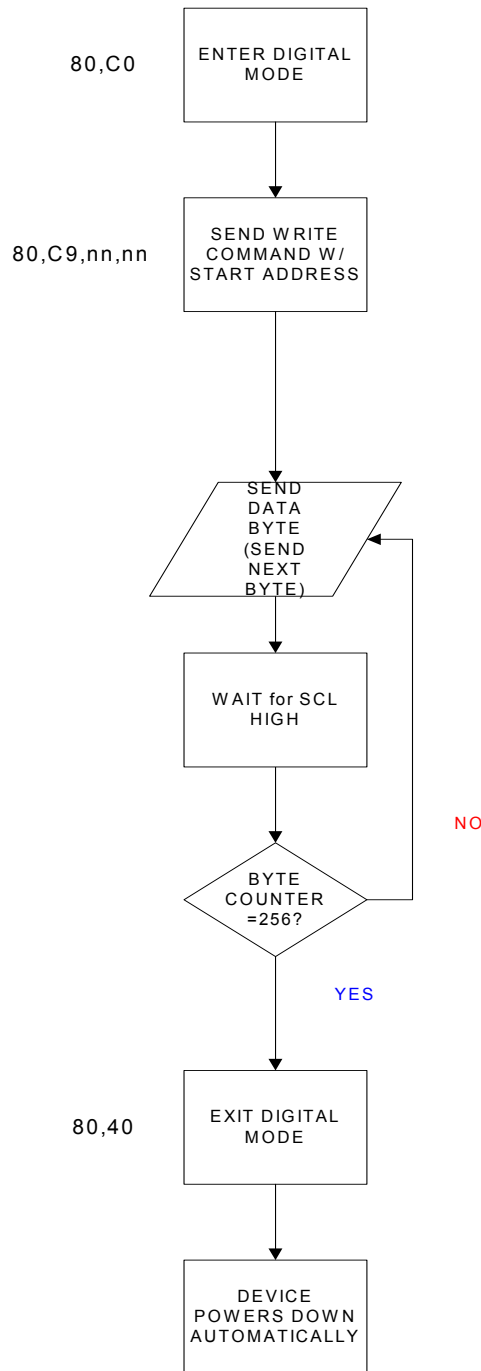
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SUGGESTED FLOW FOR DIGITAL WRITE IN ISD5100-Series

COMMANDS

- 80 = PowerUp or Stop
- C0 = Enter Digital Mode
- C9 = Write Digital Page@
- 40 = Exit Digital Mode



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6.5.4.3. Read Digital Data

Read

=====

I2CStart

SendByte(0x80) - Write, Slave address zero

WaitACK

WaitSCLHigh

SendByte(0xc0) - Enter Digital Mode

WaitACK

WaitSCLHigh

I2CStop

I2CStart

SendByte(0x80) - Write, Slave address zero

WaitACK

WaitSCLHigh

SendByte(0xe1) - Read Digital Data Command

WaitACK

WaitSCLHigh

SendByte(row/256) - high address byte

WaitACK

WaitSCLHigh()

SendByte(row%256) - low address byte

WaitACK

WaitSCLHigh

I2CStart - Send repeat start command

SendByte(0x81) - Read, Slave address zero

repeat until all data is read

{

data = ReadByte() - send clocks to read data byte

SendACK - send NACK on the last byte

WaitSCLHigh - The only flow control available

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}

I2CStop()

I2CStart

SendByte(0x80) - Write, Slave address zero

WaitACK

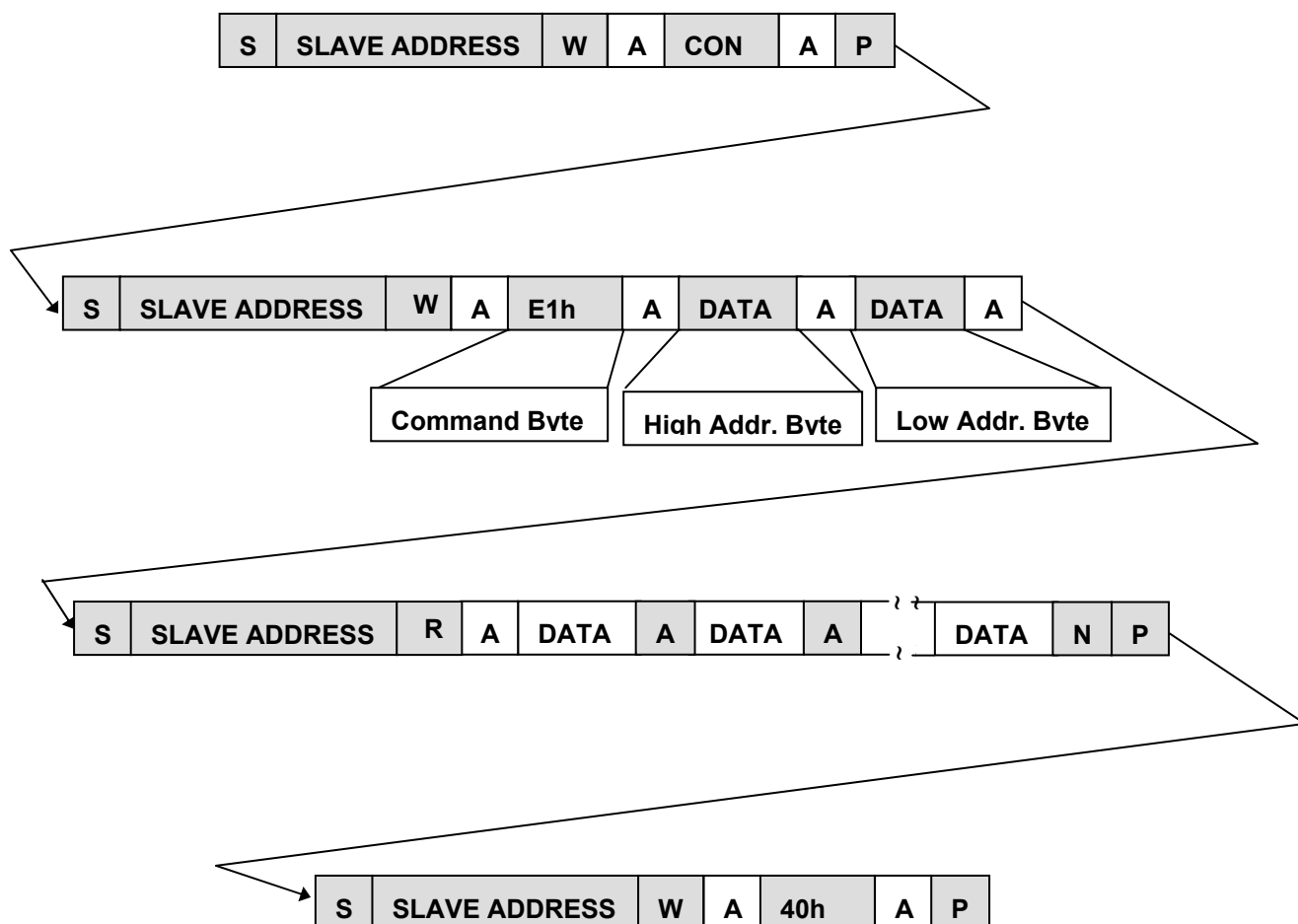
WaitSCLHigh

SendByte(0x40) - Exit Digital Mode

WaitACK

WaitSCLHigh

I2CStop



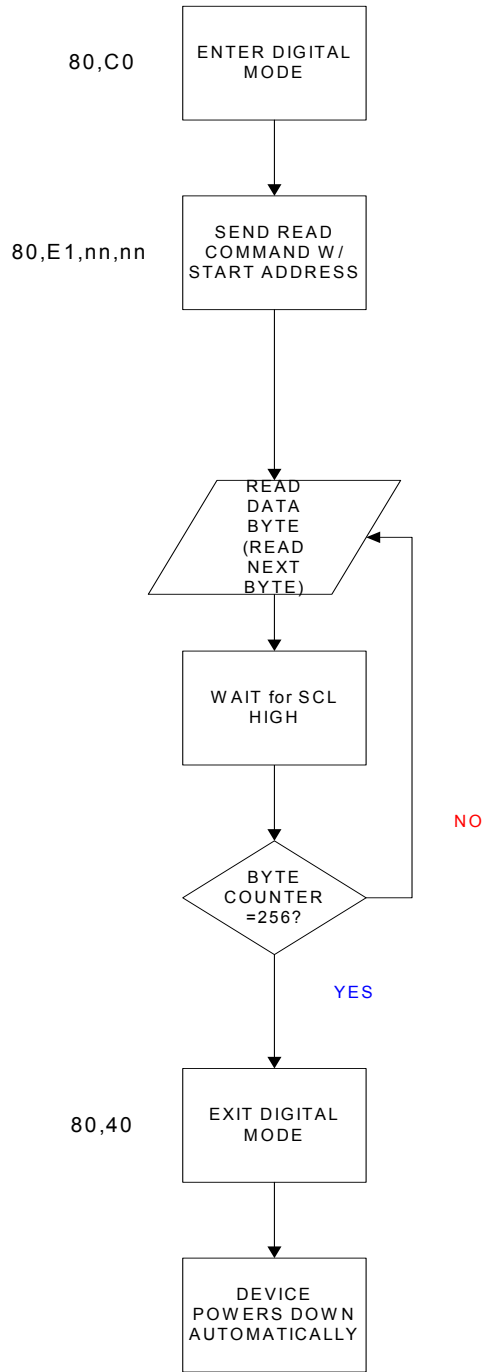
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SUGGESTED FLOW FOR DIGITAL READ IN ISD5100-Series

COMMANDS
 80 = PowerUp or Stop
 C0 = Enter Digital Mode
 E1 = Read Digital Page@
 40 = Exit Digital Mode



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6.6. PIN DETAILS

6.6.1 Digital I/O Pins

SCL (Serial Clock Line)

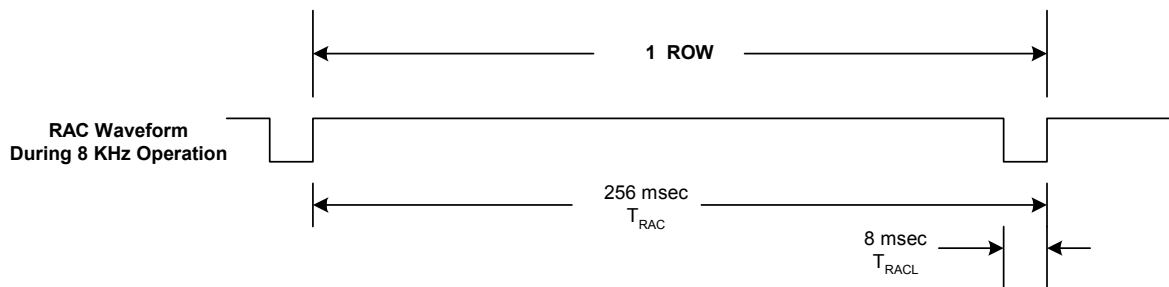
The Serial Clock Line is a bi-directional clock line. It is an open-drain line requiring a pull-up resistor to Vcc. It is driven by the "master" chips in a system and controls the timing of the data exchanged over the Serial Data Line.

SDA (Serial Data Line)

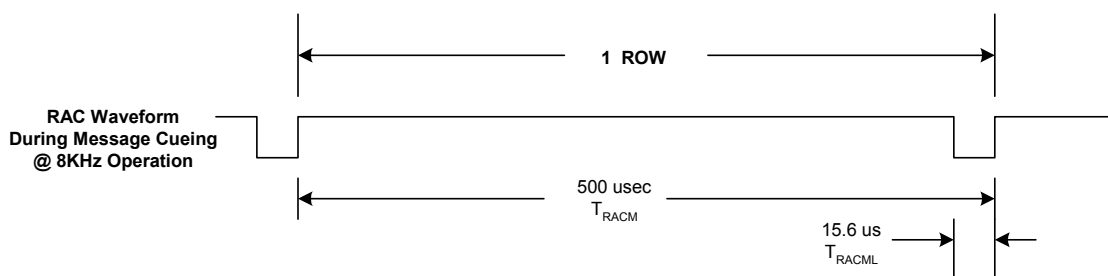
The Serial Data Line carries the data between devices on the I²C interface. Data must be valid on this line when the SCL is HIGH. State changes can only take place when the SCL is LOW. This is a bi-directional line requiring a pull-up resistor to Vcc.

RAC (Row Address Clock)

RAC is an open drain output pin that normally marks the end of a row. At the 8 kHz sample frequency, the duration of this period is 256 ms. RAC stays HIGH for 248 ms and stays LOW for the remaining 8 ms before it reaches the end of a row. There are 2048 rows of memory in the ISD5116 devices, 1024 rows in the ISD5108, 512 rows in the ISD5104 and 256 rows in the ISD5102.



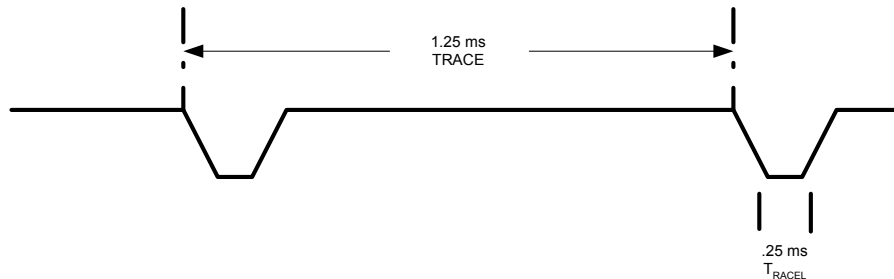
The RAC pin remains HIGH for 500 μ sec and stays LOW for 15.6 μ sec under the Message Cueing mode. See the [Timing Parameters table](#) on page 64 for RAC timing information at other sample rates. When a record command is first initiated, the RAC pin remains HIGH for an extra T_{RACML} period, to load sample and hold circuits internal to the device. The RAC pin can be used for message management techniques.



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RAC Waveform During Digital Erase @ 8kHz Operation



INT (Interrupt)

INT is an open drain output pin. The ISD5100 Series interrupt pin goes LOW and stays LOW when an Overflow (OVF) or End of Message (EOM) marker is detected. Each operation that ends in an EOM or OVF generates an interrupt, including the message cueing cycles. The interrupt is cleared by a READ STATUS instruction that will give a status byte out the SDA line.

XCLK (External Clock Input)

This is the external clock input. To use internal clock, this pin must be grounded (suggest connecting to V_{SSD}). While in internal clock mode, the ISD5100 Series are operated at one of four internal rates selected for its internal oscillator by the Sample Rate Select bits. For precision timing control, external clock signal can be applied through this pin. In the external clock mode, the device can be clocked through the XCLK pin at 4.096 MHz as described in [section 7.4.3](#) on page 32.

Because the anti-aliasing and smoothing filters track the Sample Rate Select bits, one must, for optimum performance, maintain the external clock at 4.096 MHz *AND* set the Sample Rate Configuration bits to one of the four values to properly set the filters to the correct cutoff frequency as described in [section 7.4.3](#) on page 32. The duty cycle on the input clock is not critical, as the clock is immediately divided by two internally.

External Clock Input Table

ISD5116 Duration (Minutes)	ISD5108 Duration (Minutes)	ISD5104 Duration (Minutes)	ISD5102 Duration (Minutes)	Sample Rate (kHz)	Required Clock (kHz)	FLD1	FLD0	Filter Knee (kHz)
8.73	4.36	2.18	1.08	8.0	4096	0	0	3.4
10.9	5.45	2.72	1.35	6.4	4096	0	1	2.7
13.1	6.55	3.27	1.63	5.3	4096	1	0	2.3
17.5	8.75	4.37	2.18	4.0	4096	1	1	1.7

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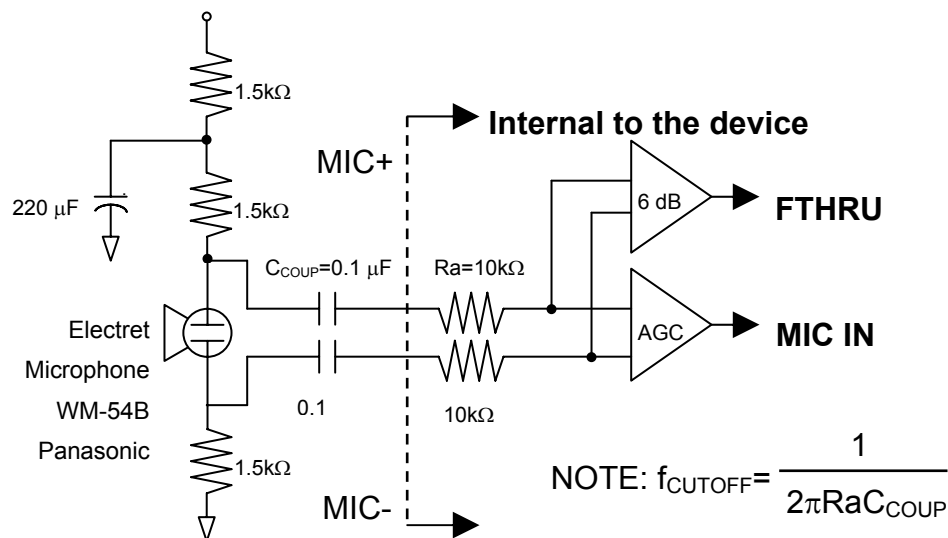
A0, A1 (Address Pins)

These two pins are normally strapped for the desired address that the ISD5100 Series will have on the I²C serial interface. If there are four of these devices on the bus, then each must be strapped differently in order to allow the Master device to address them individually. The possible addresses range from 80h to 87h, depending upon whether the device is being written to, or read from, by the host. The ISD5100 Series have a 7-bit slave address of which only A0 and A1 are pin programmable. The eighth bit (LSB) is the R/W bit. Thus, the address will be 1000 0xy0 or 1000 0xy1. (See the table in [section 7.3.1](#) on page 13.)

6.6.2 Analog I/O Pins

MIC+, MIC- (Microphone Input +/-)

The microphone input transfers the voice signal to the on-chip AGC preamplifier or directly to the ANA OUT MUX, depending on the selected path. The direct path to the ANA OUT MUX has a gain of 6 dB so a 208 mV p-p signal across the differential microphone inputs would give 416 mV p-p across the ANA OUT pins. The AGC circuit has a range of 45 dB in order to deliver a nominal 694 mV p-p into the storage array from a typical electret microphone output of 2 to 20 mV p-p. The input impedance is typically 10k Ω .



ANA OUT+, ANA OUT- (Analog Output +/-)

This differential output is designed to go to the microphone input of the telephone chip set. It is designed to drive a minimum of 5 k Ω between the “+” and “-” pins to a nominal voltage level of 694 mV p-p. Both pins have DC bias of approximately 1.2 VDC. The AC signal is superimposed upon this analog ground voltage. These pins can be used single-ended, getting only half the voltage. Do **NOT** ground the unused pin.

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ACAP (AGC Capacitor)

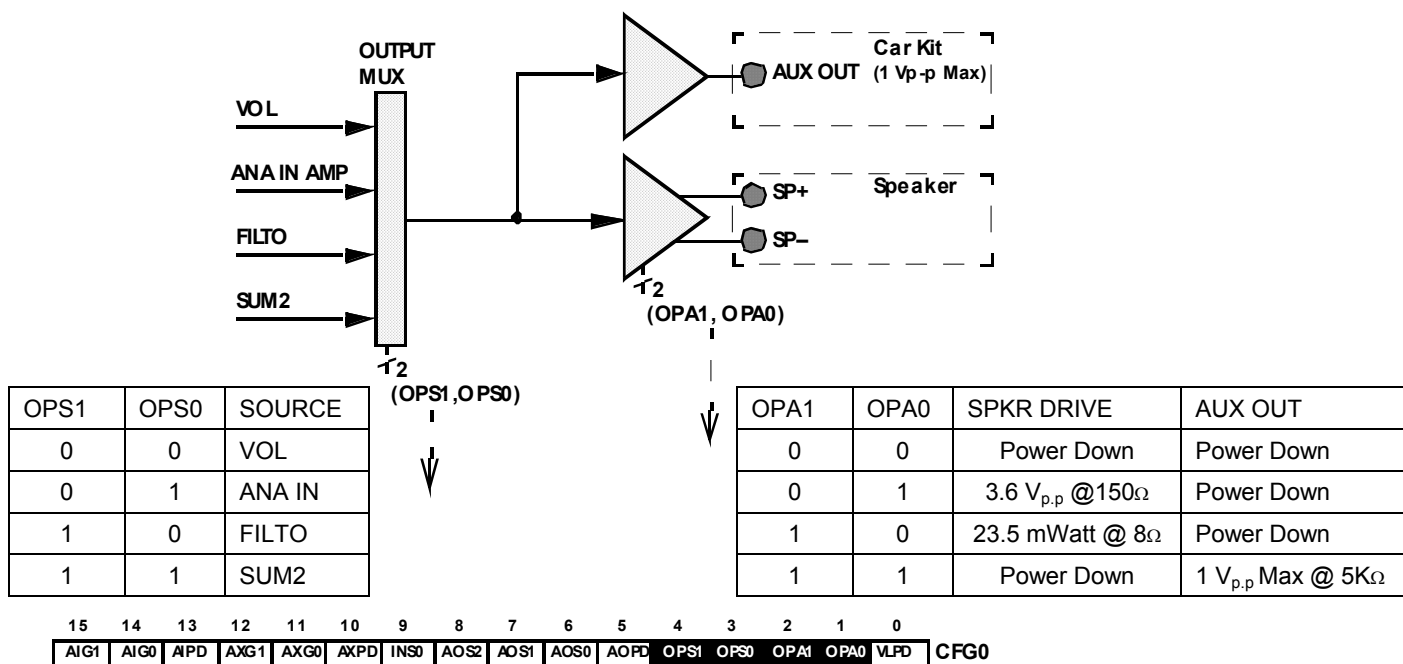
This pin provides the capacitor connection for setting the parameters of the microphone AGC circuit. It should have a 4.7 μF capacitor connected to ground. It cannot be left floating. This is because the capacitor is also used in the playback mode for the AutoMute circuit. This circuit reduces the amount of noise present in the output during quiet pauses. Tying this pin to ground gives maximum gain; tying it to V_{CCA} gives minimum gain for the AGC amplifier but cancels the AutoMute function.

SP +, SP- (Speaker +/-)

This is the speaker differential output circuit. It is designed to drive an 8 Ω speaker connected across the speaker pins up to a maximum of 23.5 mW RMS power. This stage has two selectable gains, 1.32 and 1.6, which can be chosen through the configuration registers. These pins are biased to approximately 1.2 VDC and, if used single-ended, must be capacitively coupled to their load. Do **NOT** ground the unused pin.

AUX OUT (Auxiliary Output)

The AUX OUT is an additional audio output pin to be used, for example, to drive the speaker circuit in a "car kit." It drives a minimum load of 5k Ω and up to a maximum of 1V p-p. The AC signal is superimposed on approximately 1.2 VDC bias and must be capacitively coupled to the load.



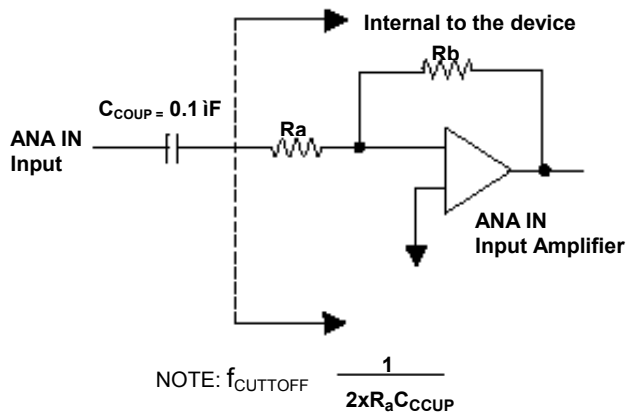
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ANA IN (Analog Input)

The ANA IN pin is the analog input from the telephone chip set. It can be switched (by the I²C interface) to the speaker output, the array input or to various other paths. This pin is designed to accept a nominal 1.11 V p-p when at its minimum gain (6 dB) setting. There is additional gain available, if required, in 3 dB steps, up to 15 dB. The gain settings are controlled from the I²C interface.

ANA IN Input Modes



Gain Setting	Resistor Ration (Rb/Ra)	Gain	Gain ² (dB)
00	63.9 / 102	0.625	-4.1
01	77.9 / 88.1	0.88	-1.1
10	92.3 / 73.8	1.25	1.9
11	106 / 60	1.77	4.9

Note: Ra & Rb are in kΩ

ANA IN Amplifier Gain Settings

Setting ⁽¹⁾	0TLP Input V _{P-P} ⁽³⁾	CFG0		Gain ⁽²⁾	Array In/Out V _{P-P}	Speaker Out V _{P-P} ⁽⁴⁾
		AIG1	AIG0			
6 dB	1.110	0	0	0.625	0.694	2.22
9 dB	0.785	0	1	0.883	0.694	2.22
12 dB	0.555	1	0	1.250	0.694	2.22
15 dB	0.393	1	1	1.767	0.694	2.22

1. Gain from ANA IN to SP+/-
2. Gain from ANA IN to ARRAY IN
3. 0TLP Input is the reference Transmission Level Point that is used for testing. This level is typically 3 dB below clipping
4. Speaker Out gain set to 1.6 (High). (Differential)

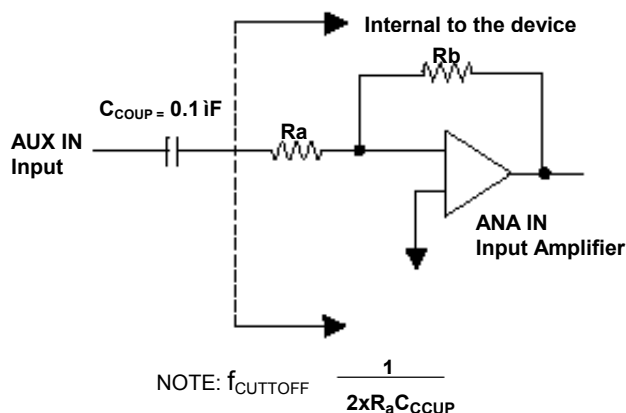
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AUX IN (Auxiliary Input)

The AUX IN is an additional audio input to the ISD5100-Series, such as from the microphone circuit in a mobile phone “car kit.” This input has a nominal 694 mV p-p level at its minimum gain setting (0 dB). See the [AUX IN Amplifier Gain Settings table](#) on page 56. Additional gain is available in 3 dB steps (controlled by the I²C interface) up to 9 dB.

AUX IN Input Modes



Gain Setting	Resistor Ratio (Rb/Ra)	Gain	Gain ⁽²⁾ (dB)
00	40.1 / 40.1	1.0	0
01	47.0 / 33.2	1.414	3
10	53.5 / 26.7	2.0	6
11	59.2 / 21	2.82	9

Note: Ra & Rb are in kΩ

AUX IN Amplifier Gain Settings

Setting ⁽¹⁾	0TLP Input V _{P-P} ⁽³⁾	CFG0		Gain ⁽²⁾	Array In/Out V _{P-P}	Speaker Out V _{P-P} ⁽⁴⁾
		AXG1	AXG0			
0 dB	0.694	0	0	1.00	0.694	0.694
3 dB	0.491	0	1	1.41	0.694	0.694
6 dB	0.347	1	0	2.00	0.694	0.694
9 dB	0.245	1	1	2.82	0.694	0.694

1. Gain from AUX IN to ANA OUT
2. Gain from AUX IN to ARRAY IN
3. 0TLP Input is the reference Transmission Level Point that is used for testing. This level is typically 3 dB below clipping
4. Differential

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6.6.3 Power and Ground Pins

V_{CCA} , V_{CCD} (Voltage Inputs)

To minimize noise, the analog and digital circuits in the ISD5100 Series devices use separate power busses. These +3 V busses lead to separate pins. Tie the V_{CCD} pins together as close as possible and decouple both supplies as near to the package as possible.

V_{SSA} , V_{SSD} (Ground Inputs)

The ISD5100 Series utilizes separate analog and digital ground busses. The analog ground (V_{SSA}) pins should be tied together as close to the package as possible and connected through a low-impedance path to power supply ground. The digital ground (V_{SSD}) pin should be connected through a separate low impedance path to power supply ground. These ground paths should be large enough to ensure that the impedance between the V_{SSA} pins and the V_{SSD} pin is less than 3Ω . The backside of the die is connected to V_{SSD} through the substrate resistance. In a chip-on-board design, the die attach area must be connected to V_{SSD} .

NC (Not Connect)

These pins should not be connected to the board at any time. Connection of these pins to any signal, ground or V_{CC} , may result in incorrect device behavior or cause damage to the device.

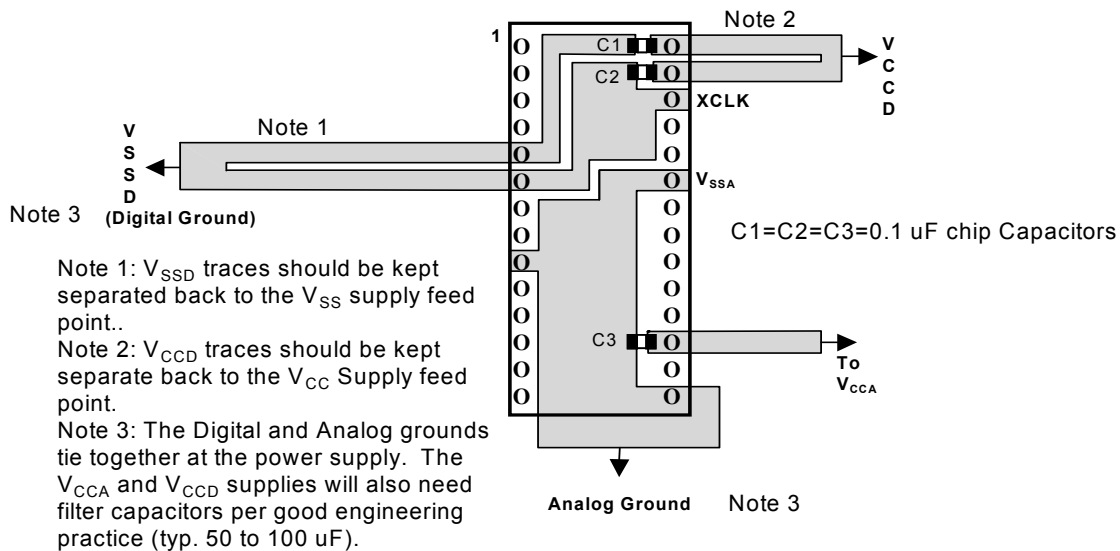
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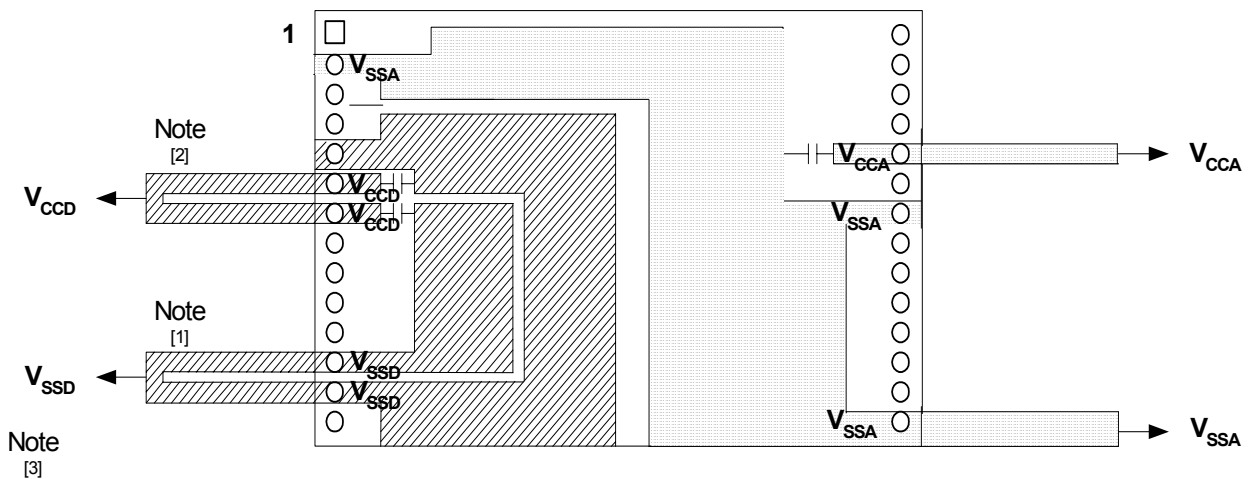
6.6.4 PCB Layout Examples

For SOIC package :

PC board traces and the three chip capacitors are on the bottom side of the board.



For TSOP package :



Notes:

- [1] V_{SSD} traces should be kept separated back to the V_{SS} supply feedpoint.
- [2] V_{CCD} traces should be kept separate back to the V_{CC} supply feedpoint.
- [3] Digital and Analog grounds tie together at power supply. The V_{CCA} and V_{CCD} supplies will also need filter capacitors per good engineering practice (typ. 50 to 100 μ F).

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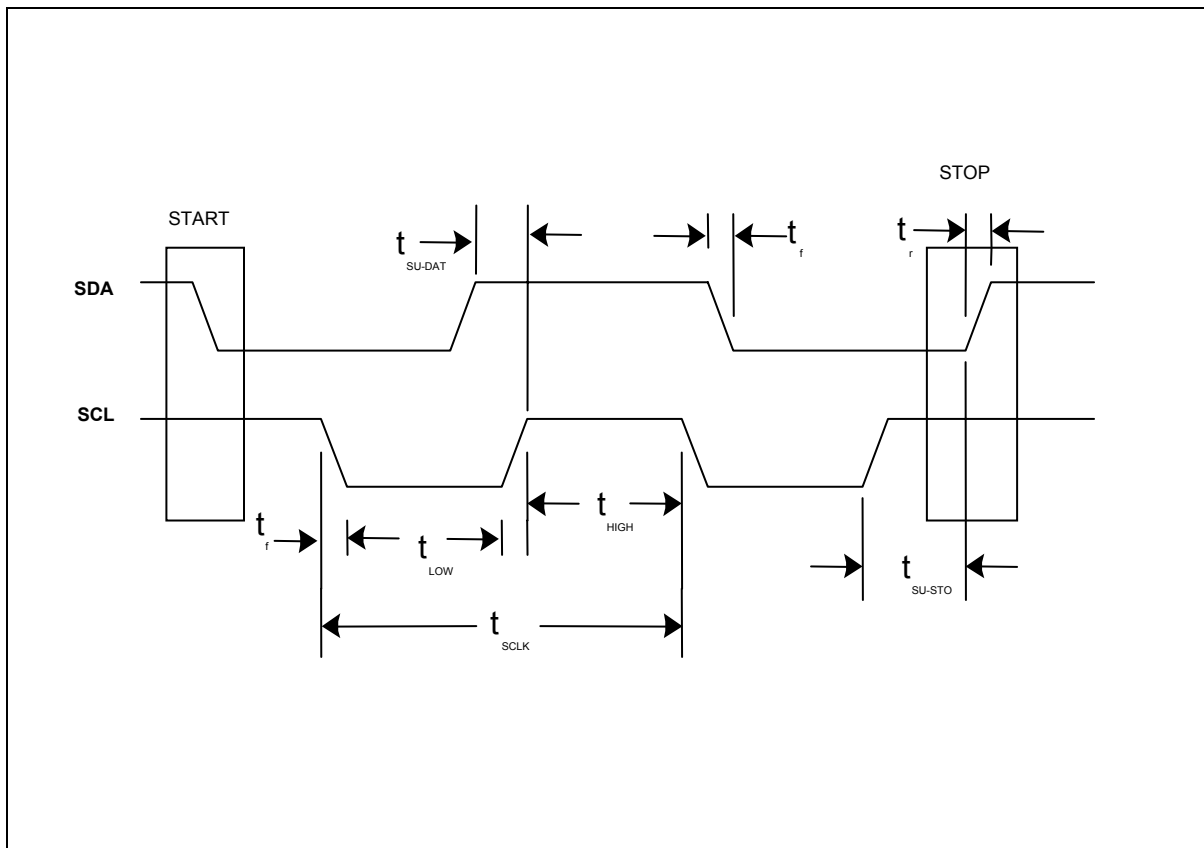


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7. TIMING DIAGRAMS

7.1 I²C TIMING DIAGRAM



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I²C INTERFACE TIMING

PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		UNIT
		MIN.	MAX.	MIN.	MAX.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	t_{HD-STA}	4.0	-	0.6	-	μ s
LOW period of the SCL clock	t_{LOW}	4.7	-	1.3	-	μ s
HIGH period of the SCL clock	t_{HIGH}	4.0	-	0.6	-	μ s
Set-up time for a repeated START condition	t_{SU-STA}	4.7	-	0.6	-	μ s
Data set-up time	t_{SU-DAT}	250	-	100 ⁽¹⁾	-	ns
Rise time of both SDA and SCL signals	t_r	-	1000	$20 + 0.1C_b^{(2)}$	300	ns
Fall time of both SDA and SCL signals	t_f	-	300	$20 + 0.1C_b^{(2)}$	300	ns
Set-up time for STOP condition	t_{SU-STO}	4.0	-	0.6	-	μ s
Bus-free time between a STOP and START condition	t_{BUF}	4.7	-	1.3	-	μ s
Capacitive load for each bus line	C_b	-	400	-	400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	$0.1 V_{DD}$	-	$0.1 V_{DD}$	-	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nH}	$0.2 V_{DD}$	-	$0.2 V_{DD}$	-	V

1. A Fast-mode I²C-interface device can be used in a Standard-mode I²C-interface system, but the requirement $t_{SU,DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal.

If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line; $t_{r\ max} + t_{SU,DAT} = 1000 + 250 = 1250$ ns (according to the Standard-mode I²C -interface specification) before the SCL line is released.

2. C_b = total capacitance of one bus line in pF. If mixed with HS mode devices, faster fall-times are allowed.

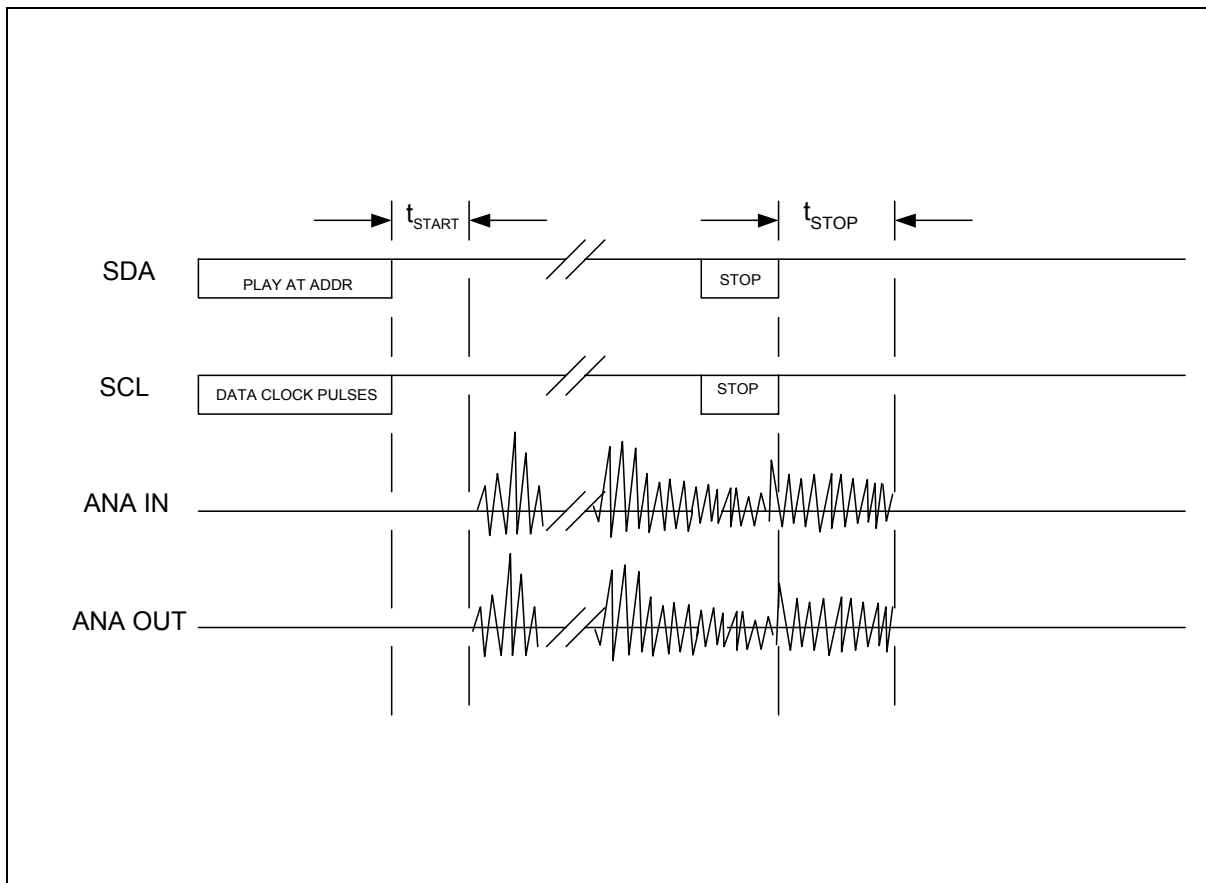
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7.2 PLAYBACK AND STOP CYCLE

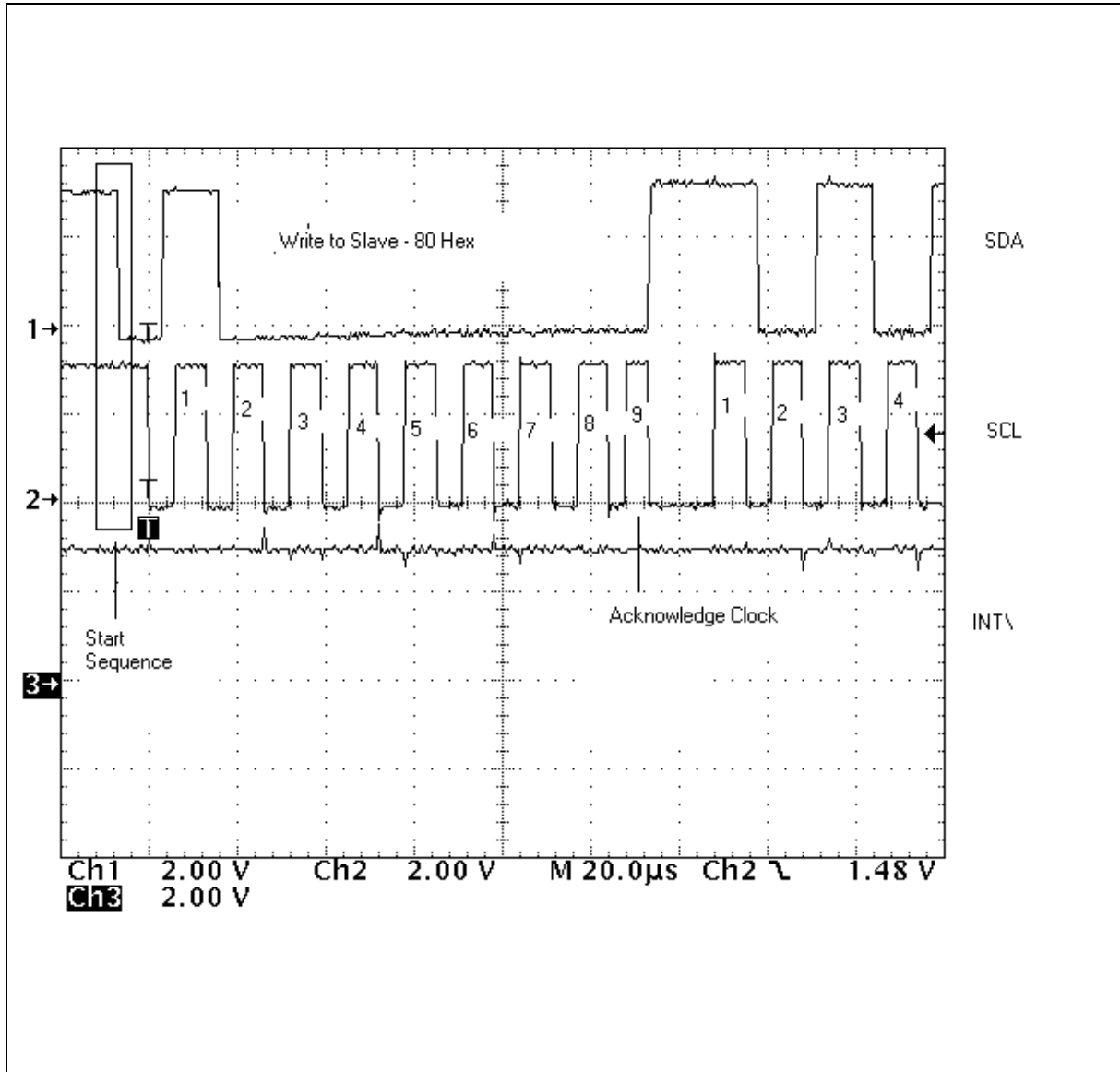


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7.3 EXAMPLE OF POWER UP COMMAND (FIRST 12 BITS)



ISD5100 SERIES**nuvoTon****8. ABSOLUTE MAXIMUM RATINGS****ABSOLUTE MAXIMUM RATINGS (PACKAGED PARTS)⁽¹⁾**

Condition	Value
Junction temperature	150 ⁰ C
Storage temperature range	-65 ⁰ C to +150 ⁰ C
Voltage Applied to any pins	(V _{SS} - 0.3V) to (V _{CC} + 0.3V)
Voltage applied to any pin (Input current limited to +/-20 mA)	(V _{SS} - 1.0V) to (V _{CC} + 1.0V)
Lead temperature (soldering - 10 seconds)	300 ⁰ C
V _{CC} - V _{SS}	-0.3V to +5.5V

^{1.} Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.

ABSOLUTE MAXIMUM RATINGS (DIE)⁽¹⁾

Condition	Value
Junction temperature	150 ⁰ C
Storage temperature range	-65 ⁰ C to +150 ⁰ C
Voltage Applied to any pads	(V _{SS} - 0.3V) to (V _{CC} + 0.3V)
V _{CC} - V _{SS}	-0.3V to +5.5V

^{1.} Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.

ISD5100 SERIES**nuvoTon****OPERATING CONDITIONS (PACKAGED PARTS)**

Conditions	Values
Commercial operating temperature ^[1]	0°C to +70°C
Supply voltage (V_{CC}) ^[2]	+2.7V to +3.3V
Ground voltage (V_{SS}) ^[3]	0V
Voltage Applied to any pins	($V_{SS} - 0.3V$) to ($V_{CC} + 0.3V$)

Conditions	Values	
Industrial operating temperature ^[1]	-40°C to +85°C	
Supply voltage (V_{CC}) ^[2]	ISD5102, ISD5104, ISD5116	+2.7V to +3.3V
	ISD5108	+2.7V to +3.6V
Ground voltage (V_{SS}) ^[3]	0V	
Voltage Applied to any pins	($V_{SS} - 0.3V$) to ($V_{CC} + 0.3V$)	

OPERATING CONDITIONS (DIE)

Conditions	Values
Die operating temperature range ^[1]	0°C to +50°C
Supply voltage (V_{CC}) ^[2]	+2.7V to +3.3V
Ground voltage (V_{SS}) ^[3]	0V
Voltage Applied to any pads	($V_{SS} - 0.3V$) to ($V_{CC} + 0.3V$)

^[1] Case temperature^[2] $V_{CC} = V_{CCA} = V_{CCD}$ ^[3] $V_{SS} = V_{SSA} = V_{SSD}$

ISD5100 SERIES**9. ELECTRICAL CHARACTERISTICS****9.1. GENERAL PARAMETERS**

Symbol	Parameters	Min ⁽²⁾	Typ ⁽¹⁾	Max ⁽²⁾	Units	Conditions
V _{IL}	Input Low Voltage			V _{CC} × 0.2	V	
V _{IH}	Input High Voltage	V _{CC} × 0.8			V	
V _{OL}	SCL, SDA Output Low Voltage			0.4	V	I _{OL} = 3 μA
V _{IL2V}	Input low voltage for 2V interface			0.4	V	Apply only to SCL, SDA
V _{IH2V}	Input high voltage for 2V interface	1.6			V	Apply only to SCL, SDA
V _{OL1}	RAC, INT Output Low Voltage			0.4	V	I _{OL} = 1 mA
V _{OH}	Output High Voltage	V _{CC} - 0.4			V	I _{OL} = -10 μA
I _{CC}	V _{CC} Current (Operating) - Playback - Record - Feedthrough		15 30 12	25 40 15	mA	No Load ⁽³⁾ No Load ⁽³⁾ No Load ⁽³⁾
I _{SB}	V _{CC} Current (Standby)		1	10	μA	[3]
I _{IL}	Input Leakage Current			±1	μA	

^[1] Typical values: T_A = 25°C and V_{CC} = 3.0 V.

^[2] All min/max limits are guaranteed by Nuvoton via electrical testing or characterization. Not all specifications are 100 percent tested.

^[3] All V_{CC} and V_{SS} are connected appropriately and others are floated.

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9.2. TIMING PARAMETERS

Symbol	Parameters	Min ⁽²⁾	Typ ⁽¹⁾				Max ⁽²⁾	Units	Conditions
F _S	Sampling Frequency		8.0					kHz	(5)
			6.4					kHz	(5)
			5.3					kHz	(5)
			4.0					kHz	(5)
F _{CF}	Filter Knee								
	8.0 kHz (sample rate)		3.4					kHz	Knee Point ⁽³⁾⁽⁷⁾
	6.4 kHz (sample rate)		2.7					kHz	Knee Point ⁽³⁾⁽⁷⁾
	5.3 kHz (sample rate)		2.3					kHz	Knee Point ⁽³⁾⁽⁷⁾
T _{REC}	Record Duration		ISD5116	ISD5108	ISD5104	ISD5102			
	8.0 kHz (sample rate)		8.73	4.36	2.18	1.08		min	(6)
	6.4 kHz (sample rate)		10.9	5.45	2.72	1.35		min	(6)
	5.3 kHz (sample rate)		13.1	6.55	3.27	1.63		min	(6)
T _{PLAY}	Playback Duration		ISD5116	ISD5108	ISD5104	ISD5102			
	8.0 kHz (sample rate)		8.73	4.36	2.18	1.08		min	(6)
	6.4 kHz (sample rate)		10.9	5.45	2.72	1.35		min	(6)
	5.3 kHz (sample rate)		13.1	6.55	3.27	1.63		min	(6)
T _{PUD}	Power-Up Delay								
	8.0 kHz (sample rate)		1					msec	
	6.4 kHz (sample rate)		1					msec	
	5.3 kHz (sample rate)		1					msec	
T _{STOP/ PAUSE}	Stop or Pause								
	Record or Play								
	8.0 kHz (sample rate)		32					msec	
	6.4 kHz (sample rate)		40					msec	
T _{RAC}	5.3 kHz (sample rate)		48					msec	
	4.0 kHz (sample rate)		64					msec	
	RAC Clock Period								
T _{RAC}	8.0 kHz (sample rate)		256					msec	(9)
	6.4 kHz (sample rate)		320					msec	(9)
	5.3 kHz (sample rate)		384					msec	(9)

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	4.0 kHz (sample rate)		512		msec	(9)
T _{RACL}	RAC Clock Low Time					
	8.0 kHz (sample rate)		8		msec	
	6.4 kHz (sample rate)		10		msec	
	5.3 kHz (sample rate)		12.1		msec	
	4.0 kHz (sample rate)		16		msec	
T _{RACM}	RAC Clock Period in Message Cueing Mode					
	8.0 kHz (sample rate)		500		μsec	
	6.4 kHz (sample rate)		625		μsec	
	5.3 kHz (sample rate)		750		μsec	
	4.0 kHz (sample rate)		1000		μsec	
T _{RACML}	RAC Clock Low Time in Message Cueing Mode					
	8.0 kHz (sample rate)		15.6		μsec	
	6.4 kHz (sample rate)		19.5		μsec	
	5.3 kHz (sample rate)		23.4		μsec	
	4.0 kHz (sample rate)		31.2		μsec	
T _{RACE}	RAC Clock Period in Digital Erase Mode					
	8.0 kHz (sample rate)		1.25		msec	
	6.4 kHz (sample rate)		1.56		msec	
	5.3 kHz (sample rate)		1.87		msec	
	4.0 kHz (sample rate)		2.50		msec	
T _{RACEL}	RAC Clock Low Time in Digital Erase mode					
	8.0 kHz (sample rate)		0.25		msec	
	6.4 kHz (sample rate)		0.31		msec	
	5.3 kHz (sample rate)		0.37		msec	
	4.0 kHz (sample rate)		0.50		msec	
THD	Total Harmonic Distortion					
	ANA IN to ARRAY, ARRAY to SPKR		1 1	2 2	% %	@1 kHz at 0TLP, sample rate = 5.3 kHz

ISD5100 SERIES**nuvoTon****9.3. ANALOG PARAMETERS****MICROPHONE INPUT⁽¹⁴⁾**

Symbol	Parameters	Min ⁽²⁾	Typ ⁽¹⁾⁽¹⁴⁾	Max ⁽²⁾	Units	Conditions
V _{MIC+/-}	MIC +/- Input Voltage			300	mV	Peak-to-Peak ⁽⁴⁾⁽⁸⁾
V _{MIC (OTLP)}	MIC +/- input reference transmission level point (OTLP)		208		mV	Peak-to-Peak ⁽⁴⁾⁽¹⁰⁾
A _{MIC}	Gain from MIC +/- input to ANA OUT	5.5	6.0	6.5	dB	1 kHz at V _{MIC (OTLP)} ⁽⁴⁾
A _{MIC (GT)}	MIC +/- Gain Tracking		+/-0.1		dB	1 kHz, +3 to -40 dB OTLP Input
R _{MIC}	Microphone input resistance		10		kΩ	MIC- and MIC+ pins
A _{AGC}	Microphone AGC Amplifier Range	6		40	dB	Over 3-300 mV Range

ANA IN⁽¹⁴⁾

Symbol	Parameters	Min ⁽²⁾	Typ ⁽¹⁾⁽¹⁴⁾	Max ⁽²⁾	Units	Conditions
V _{ANA IN}	ANA IN Input Voltage			1.6	V	Peak-to-Peak (6 dB gain setting)
V _{ANA IN (OTLP)}	ANA IN (OTLP) Input Voltage		1.1		V	Peak-to-Peak (6 dB gain setting) ⁽¹⁰⁾
A _{ANA IN (sp)}	Gain from ANA IN to SP+/-		+6 to +15		dB	4 Steps of 3 dB
A _{ANA IN (AUX OUT)}	Gain from ANA IN to AUX OUT		-4 to +5		dB	4 Steps of 3 dB
A _{ANA IN (GA)}	ANA IN Gain Accuracy	-0.5		+0.5	dB	(11)
A _{ANA IN (GT)}	ANA IN Gain Tracking		+/-0.1		dB	1000 Hz, +3 to -45 dB OTLP Input, 6 dB setting
R _{ANA IN}	ANA IN Input Resistance (6 dB to +15 dB)		10 to 100		kΩ	Depending on ANA IN Gain

ISD5100 SERIES**nuvoTon****AUX IN⁽¹⁴⁾**

Symbol	Parameters	Min ⁽²⁾	Typ ⁽¹⁾⁽¹⁴⁾	Max ⁽²⁾	Units	Conditions
V _{AUX IN}	AUX IN Input Voltage			1.0	V	Peak-to-Peak (0 dB gain setting)
V _{AUX IN (0TLP)}	AUX IN (0TLP) Input Voltage		694.2		mV	Peak-to-Peak (0 dB gain setting)
A _{AUX IN (ANA OUT)}	Gain from AUX IN to ANA OUT		0 to +9		dB	4 Steps of 3 dB
A _{AUX IN (GA)}	AUX IN Gain Accuracy	-0.5		+0.5	dB	(11)
A _{AUX IN (GT)}	AUX IN Gain Tracking		+/-0.1		dB	1000 Hz, +3 to -45 dB 0TLP Input, 0 dB setting
R _{AUX IN}	AUX IN Input Resistance		10 to 100		kΩ	Depending on AUX IN Gain

SPEAKER OUTPUTS⁽¹⁴⁾

Symbol	Parameters	Min ⁽²⁾	Typ ⁽¹⁾⁽¹⁴⁾	Max ⁽²⁾	Units	Conditions
V _{SPHG}	SP+/- Output Voltage (High Gain Setting)			3.6	V	Peak-to-Peak, differential load = 150Ω, OPA1, OPA0 = 01
R _{SPLG}	SP+/- Output Load Imp. (Low Gain)	8			Ω	OPA1, OPA0 = 10
R _{SPHG}	SP+/- Output Load Imp. (High Gain)	70	150		Ω	OPA1, OPA0 = 01
C _{SP}	SP+/- Output Load Cap.			100	pF	
V _{SPAG}	SP+/- Output Bias Voltage (Analog Ground)		1.2		VDC	
V _{SPDCO}	Speaker Output DC Offset			+/-100	mV DC	With ANA IN to Speaker, ANA IN AC coupled to V _{SSA}
IC _{N ANA IN(SP+/-)}	ANA IN to SP+/- Idle Channel Noise			-65	dB	Speaker Load = 150Ω ⁽¹²⁾⁽¹³⁾
C _{RT(SP+/-)/ANA OUT}	SP+/- to ANA OUT Cross Talk			-65	dB	1 kHz 0TLP input to ANA IN, with MIC+/- and AUX IN AC coupled to V _{SS} , and measured at ANA OUT feed through mode ⁽¹²⁾
PSRR	Power Supply Rejection Ratio		-55		dB	Measured with a 1 kHz, 100 mV p-p

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						sine wave input at V_{CC} and V_{CC} pins
F_R	Frequency Response (300-3400 Hz)		± 0.5		dB	With 0TLP input to ANA IN, 6 dB setting ⁽¹²⁾ Guaranteed by design
P_{OUTLG}	Power Output (Low Gain Setting)	23.5			mW RMS	Differential load at 8Ω
SINAD	SINAD ANA IN to SP+/-	62.5			dB	0TLP ANA In input minimum gain, 150Ω load ⁽¹²⁾⁽¹³⁾

ANA OUT⁽¹⁴⁾

Symbol	Parameters	Min ⁽²⁾	Type ⁽¹⁾⁽¹⁴⁾	Max ⁽²⁾	Units	Conditions
SINAD	SINAD, MIC IN to ANA OUT	62.5			dB	Load = $5k\Omega$ ⁽¹²⁾⁽¹³⁾
SINAD	SINAD, AUX IN to ANA OUT (0 to 9 dB)	62.5			dB	Load = $5k\Omega$ ⁽¹²⁾⁽¹³⁾
$ICO_{NIC/ANA OUT}$	Idle Channel Noise – Microphone			-65	dB	Load = $5k\Omega$ ⁽¹²⁾⁽¹³⁾
$ICN_{AUX IN/ANA OUT}$	Idle Channel Noise – AUX IN (0 to 9 dB)			-65	dB	Load = $5k\Omega$ ⁽¹²⁾⁽¹³⁾
$PSRR_{(ANA OUT)}$	Power Supply Rejection Ratio		-40		dB	Measured with a 1 kHz, 100 mV _{P-P} sine wave to V_{CCA} , V_{CCD} pins
V_{BIAS}	ANA OUT+ and ANA OUT-		1.2		VDC	Inputs AC coupled to V_{SSA}
V_{OFFSET}	ANA OUT+ to ANA OUT-			+/- 100	mV DC	Inputs AC coupled to V_{SSA}
R_L	Minimum Load Impedance	5			$k\Omega$	Differential Load
F_R	Frequency Response (300-3400 Hz)		± 0.5		dB	0TLP input to MIC+/- in feedthrough mode. 0TLP input to AUX IN in feedthrough mode ⁽¹²⁾
$C_{RTANA OUT/(SP+/-)}$	ANA OUT to SP+/- Cross Talk			-65	dB	1 kHz 0TLP output from ANA OUT, with ANA IN AC coupled to V_{SSA} , and measured at SP+/- ⁽¹²⁾

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$C_{RTANA\ OUT/AUX\ OUT}$	ANA OUT to AUX OUT Cross Talk				-65	dB	1 kHz 0TLP output from ANA OUT, with ANA IN AC coupled to V_{SSA} , and measured at AUX OUT ⁽¹²⁾
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AUX OUT⁽¹⁴⁾

Symbol	Parameters	Min ⁽²⁾	Typ ⁽¹⁾⁽¹⁴⁾	Max ⁽²⁾	Units	Conditions	
$V_{AUX\ OUT}$	AUX OUT – Maximum Output Swing			1.0	V	5k Ω Load	
R_L	Minimum Load Impedance	5			K Ω		
C_L	Maximum Load Capacitance			100	pF		
V_{BIAS}	AUX OUT		1.2		VDC		
SINAD	SINAD – ANA IN to AUX OUT	62.5			dB	0TLP ANA IN input, minimum gain, 5k load ⁽¹²⁾⁽¹³⁾	
$ICN_{(AUX\ OUT)}$	Idle Channel Noise – ANA IN to AUX OUT			-65	dB	Load=5k Ω ⁽¹²⁾⁽¹³⁾	
$C_{RTAUX\ OUT/ANA\ OUT}$	AUX OUT to ANA OUT Cross Talk				-65	dB	1 kHz 0TLP input to ANA IN, with MIC +/- and AUX IN AC coupled to V_{SSA} , measured at SP+/-, load = 5k Ω . Referenced to nominal 0TLP @ output

VOLUME CONTROL⁽¹⁴⁾

Symbol	Parameters	Min ⁽²⁾	Typ ⁽¹⁾⁽¹⁴⁾	Max ⁽²⁾	Units	Conditions
A_{OUT}	Output Gain		-28 to 0		dB	8 steps of 4 dB, referenced to output
	Tolerance for each step	-1.0		+1.0	dB	ANA IN 1.0 kHz 0TLP, 6 dB gain setting measured differentially at SP+/-

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Conditions

1. Typical values: $T_A = 25^\circ\text{C}$ and $V_{CC} = 3.0\text{V}$.
2. All min/max limits are guaranteed by Nuvoton via electrical testing or characterization. Not all specifications are 100 percent tested.
3. Low-frequency cut off depends upon the value of external capacitors (see Pin Descriptions).
4. Differential input mode. Nominal differential input is 208 mV p-p. (OTLP)
5. Sampling frequency can vary as much as $-6/+4$ percent over the industrial temperature and voltage ranges. For greater stability, an external clock can be utilized (see Pin Descriptions).
6. Playback and Record Duration can vary as much as $-6/+4$ percent over the industrial temperature and voltage ranges. For greater stability, an external clock can be utilized (See Pin Descriptions).
7. Filter specification applies to the low pass filter.
8. For optimal signal quality, this maximum limit is recommended.
9. When a record command is sent, $T_{RAC} = T_{RAC} + T_{RACL}$ on the first page addressed.
10. The maximum signal level at any input is defined as 3.17 dB higher than the reference transmission level point. (OTLP) This is the point where signal clipping may begin.
11. Measured at OTLP point for each gain setting. See the [ANA IN table](#) and [AUX IN table](#) on pages 54 and 55 respectively.
12. OTLP is the reference test level through inputs and outputs. See the [ANA IN table](#) and [AUX IN table](#) on pages 54 and 55 respectively.
13. Referenced to OTLP input at 1 kHz, measured over 300 to 3,400 Hz bandwidth.
14. For die, only typical values are applicable.

9.4. CHARACTERISTICS OF THE I²C SERIAL INTERFACE

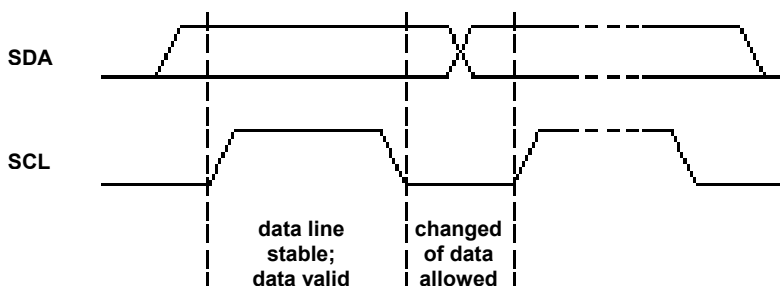
The I²C interface is for bi-directional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the interface bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse, as changes in the data line at this time will be interpreted as a control signal.

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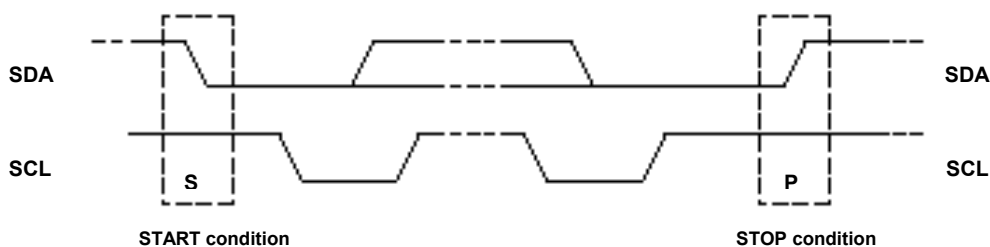
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Bit transfer on the I²C-Bus

Start and stop conditions

Both data and clock lines remain HIGH when the interface bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).



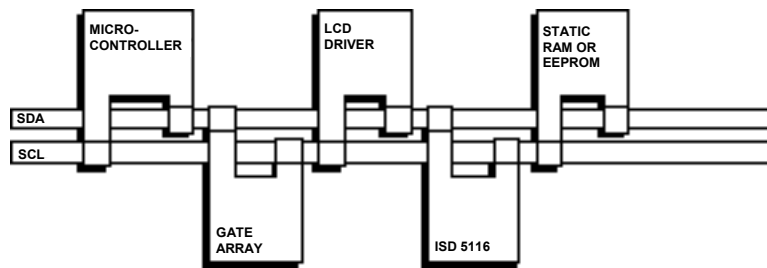
Definition of START and STOP conditions

System Configuration

A device generating a message is a 'transmitter'; a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices that are controlled by the master are the 'slaves'.

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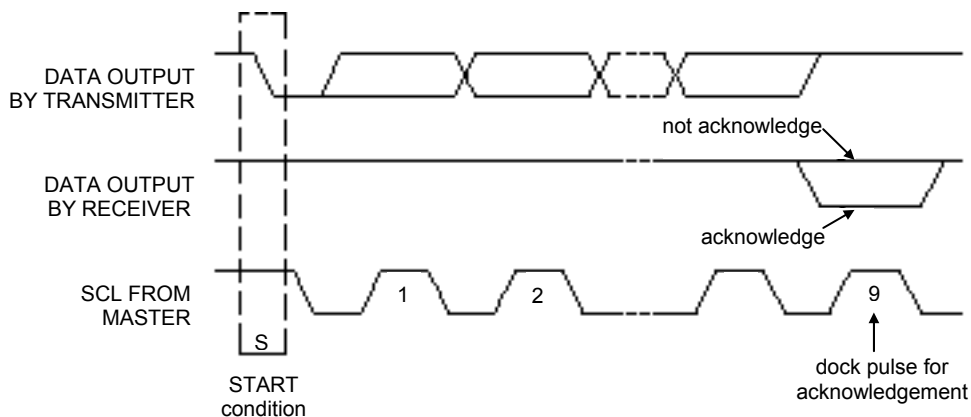


Example of an I²C-bus configuration using two microcontrollers

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the interface bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. In addition, a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a stop condition.



Acknowledge on the I²C-bus

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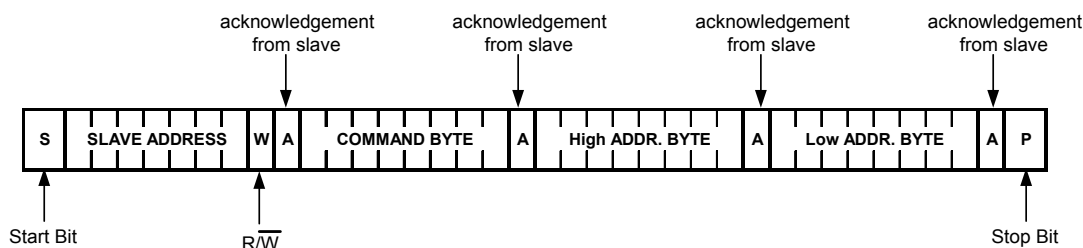
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9.5. I²C PROTOCOL

Since the I²C protocol allows multiple devices on the bus, each device must have an address. This address is known as a "Slave Address". A Slave Address consists of 7 bits, followed by a single bit that indicates the direction of data flow. This single bit is 1 for a Write cycle, which indicates the data is being sent from the current bus master to the device being addressed. This single bit is a 0 for a Read cycle, which indicates that the data is being sent from the device being addressed to the current bus master. For example, the valid Slave Addresses for the ISD5100 Series device, for both Write and Read cycles, are shown in [section 7.3.1](#) on page 13 of this datasheet.

Before any data is transmitted on the I²C interface, the current bus master must address the slave it wishes to transfer data to or from. The Slave Address is always sent out as the 1st byte following the Start Condition sequence. An example of a Master transmitting an address to a ISD5100 Series slave is shown below. In this case, the Master is writing data to the slave and the R/W bit is "0", i.e. a Write cycle. All the bits transferred are from the Master to the Slave, except for the indicated Acknowledge bits. The following example details the transfer explained in [section 7.3.1-2-3](#) on pages 13-20 of this datasheet.

Master Transmits to Slave Receiver (Write) Mode

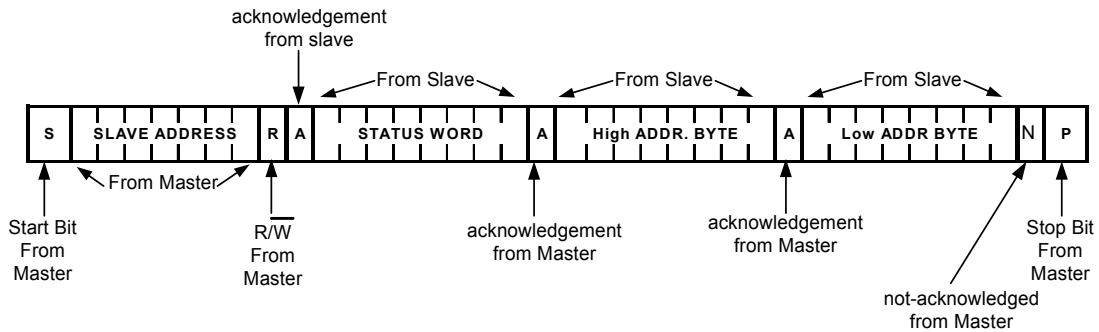


A common procedure in the ISD5100 Series is the reading of the Status Bytes. The Read Status condition in the ISD5100 Series is triggered when the Master addresses the chip with its proper Slave Address, immediately followed by the R/W bit set to a "1" and without the Command Byte being sent. This is an example of the Master sending to the Slave, immediately followed by the Slave sending data back to the Master. The "N" not-acknowledge cycle from the Master ends the transfer of data from the Slave. The following example details the transfer explained in [section 7.3.1](#) on page 13 of this datasheet.

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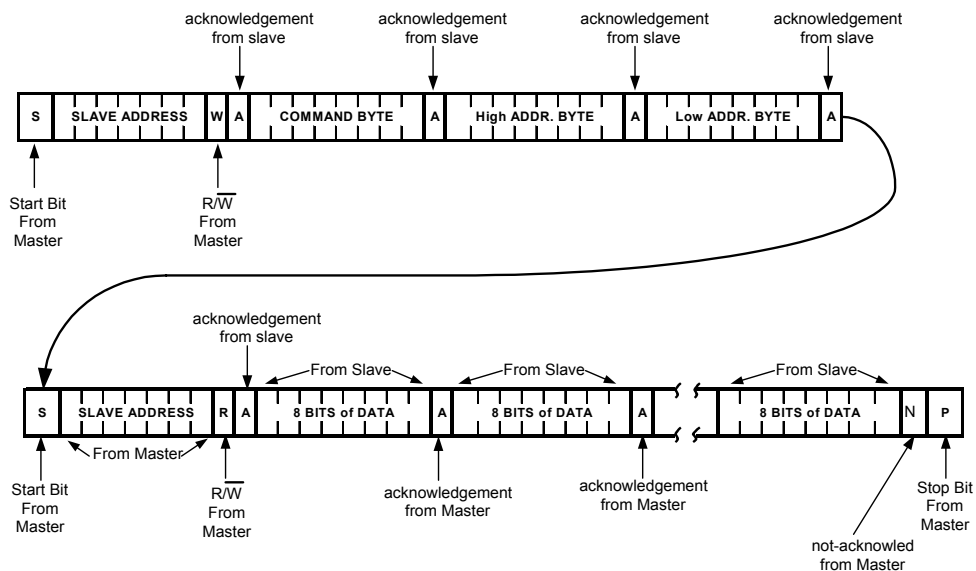


Master Reads from Slave immediately after first byte (Read Mode)



Another common operation in the ISD5100 Series is the reading of digital data from the chip's memory array at a specific address. This requires the I²C interface Master to first send an address to the ISD5100 Series Slave device, and then receive data from the Slave in a single I²C operation. To accomplish this, the data direction R/W bit must be changed in the middle of the command. The following example shows the Master sending the Slave address, then sending a Command Byte and 2 bytes of address data to the ISD5100-Series, and then immediately changing the data direction and reading some number of bytes from the chip's digital array. An unlimited number of bytes can be read in this operation. The "N" not-acknowledge cycle from the Master forces the end of the data transfer from the Slave. The following example details the transfer explained in [section 7.5.4](#) on page 47 of this datasheet.

Master Reads from the Slave after setting data address in Slave (Write data address, READ Data)



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10. TYPICAL APPLICATION CIRCUIT

The following typical application example on ISD5100 series is for references only. They make no representation or warranty that such applications shall be suitable for the use specified. It's customer's obligation to verify the design in its own system for the functionalities, voice quality, current consumption, and etc.

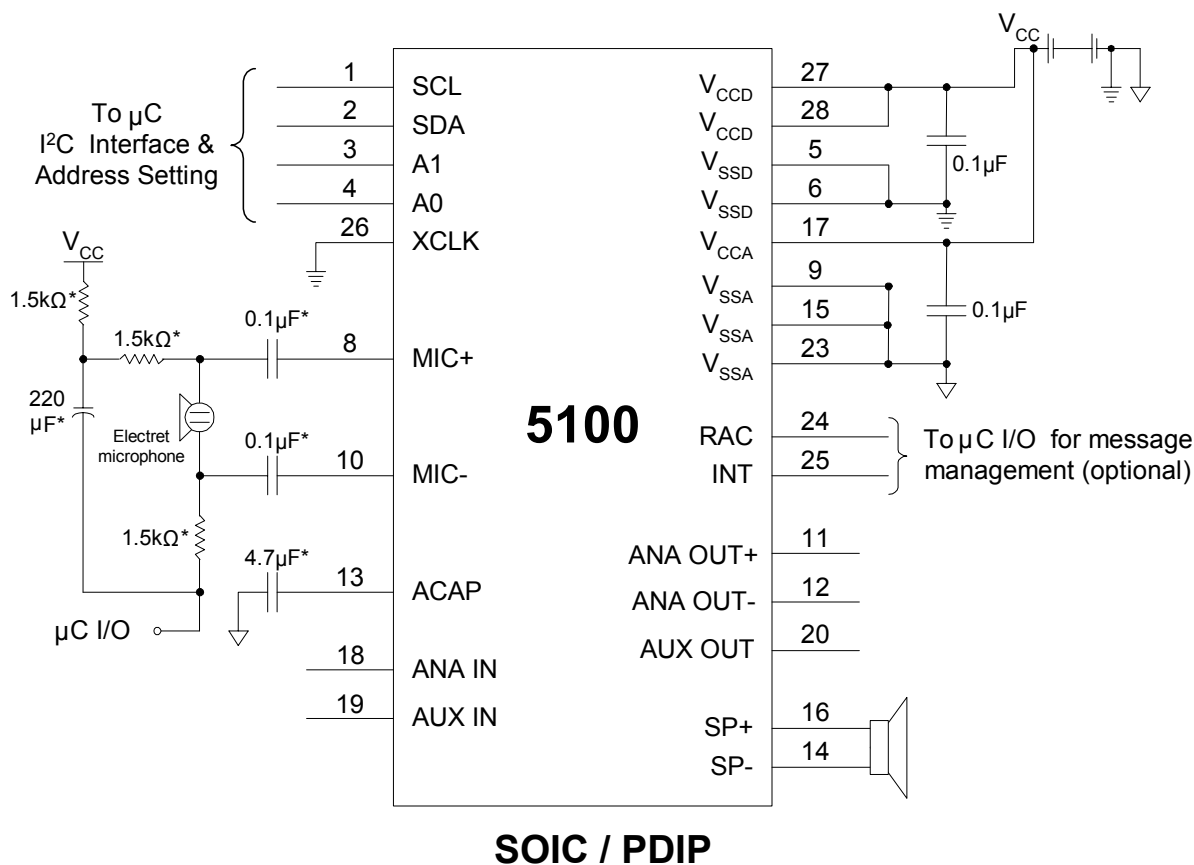
In addition, the below notes apply to the following application examples:

- * The suggested values are for references only. Depending on system requirements, they can be adjusted for functionalities and better performance.

It is important to have a separate path for each ground and power back to the related terminals to minimize the noise. Besides, the power supplies should be decoupled as close to the device as possible.

Also, it is crucial to follow good audio design practices in layout and power supply decoupling. See recommendations in Application Notes from our websites.

Example #1: Recording via microphone

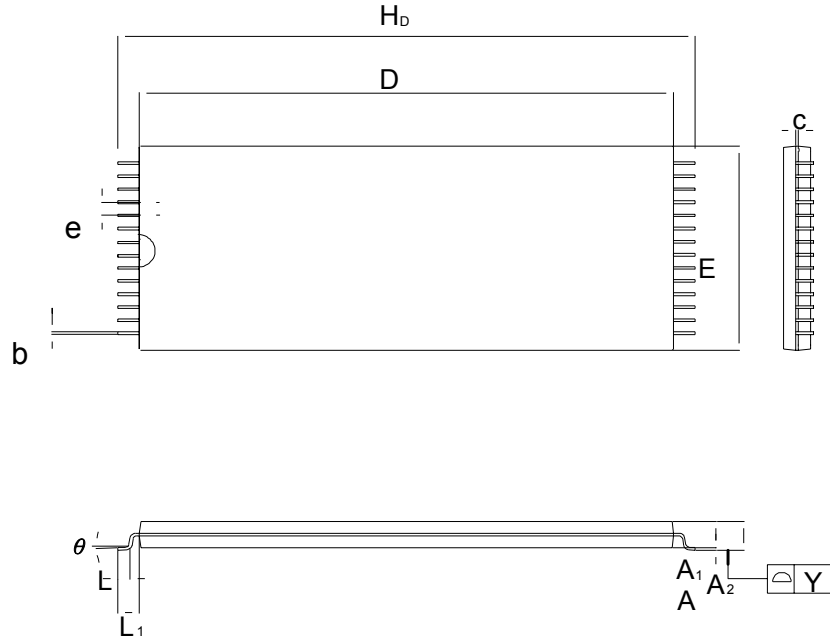


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11. PACKAGE SPECIFICATION

11.1. 28-LEAD 8X13.4MM PLASTIC THIN SMALL OUTLINE PACKAGE (TSOP) TYPE 1 - IQC

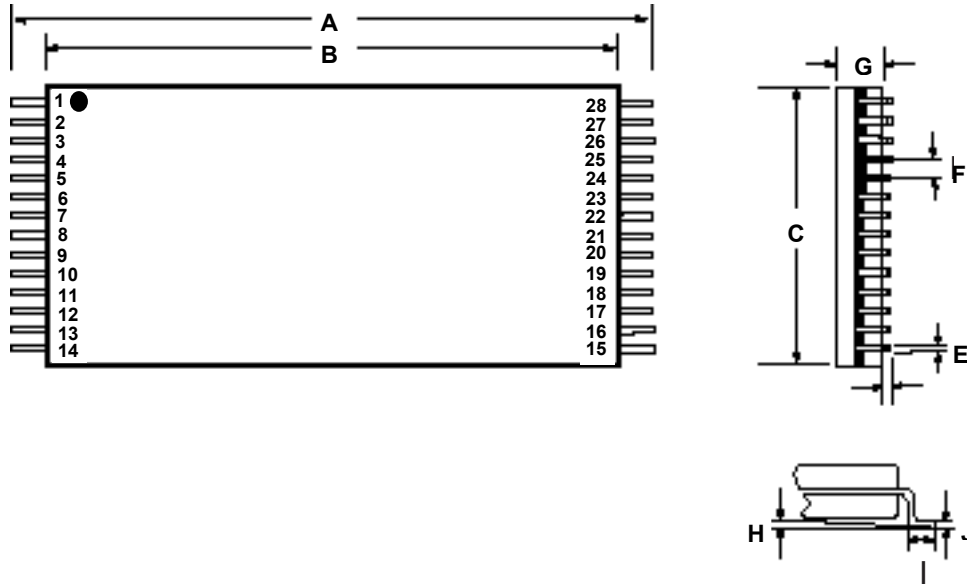


Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.047	—	—	1.20
A1	0.002	—	0.006	0.05	—	0.15
A2	0.035	0.040	0.041	0.95	1.00	1.05
b	0.007	0.008	0.011	0.17	0.20	0.27
c	0.004	0.006	0.008	0.10	0.15	0.21
D	0.461	0.465	0.469	11.70	11.80	11.90
E	0.311	0.315	0.319	7.90	8.00	8.10
H _D	0.520	0.528	0.536	13.20	13.40	13.60
e	—	0.022	—	—	0.55	—
L	0.020	0.024	0.028	0.50	0.60	0.70
L ₁	—	0.031	—	—	0.80	—
Y	0.000	—	0.004	0.00	—	0.10
θ	0	3	5	0	3	5

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11.2. 28-LEAD 8X13.4MM PLASTIC THIN SMALL OUTLINE PACKAGE (TSOP) TYPE 1



Plastic Thin Small Outline Package (TSOP) Type 1 Dimensions

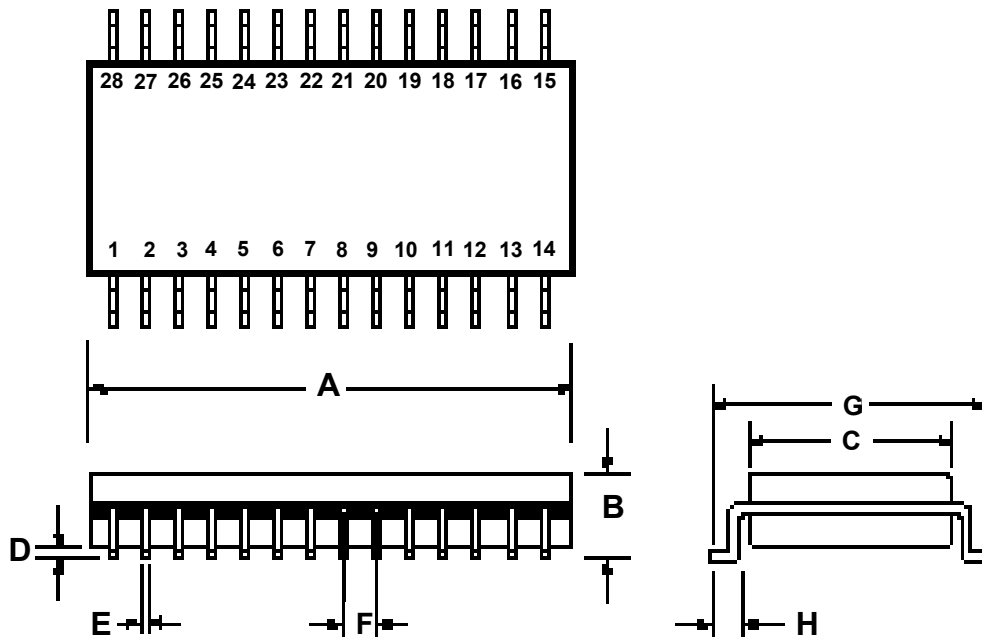
	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	0.520	0.528	0.535	13.20	13.40	13.60
B	0.461	0.465	0.469	11.70	11.80	11.90
C	0.311	0.315	0.319	7.90	8.00	8.10
D	0.002		0.006	0.05		0.15
E	0.007	0.009	0.011	0.17	0.22	0.27
F		0.0217			0.55	
G	0.037	0.039	0.041	0.95	1.00	1.05
H	0°	3°	6°	0°	3°	6°
I	0.020	0.022	0.028	0.50	0.55	0.70
J	0.004		0.008	0.10		0.21

Note: Lead coplanarity to be within 0.004 inches.

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11.3. 28-LEAD 300-MIL PLASTIC SMALL OUTLINE INTEGRATED CIRCUIT (SOIC)



Plastic Small Outline Integrated Circuit (SOIC) Dimensions

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	0.701	0.706	0.711	17.81	17.93	18.06
B	0.097	0.101	0.104	2.46	2.56	2.64
C	0.292	0.296	0.299	7.42	7.52	7.59
D	0.005	0.009	0.0115	0.127	0.22	0.29
E	0.014	0.016	0.019	0.35	0.41	0.48
F		0.050			1.27	
G	0.400	0.406	0.410	10.16	10.31	10.41
H	0.024	0.032	0.040	0.61	0.81	1.02

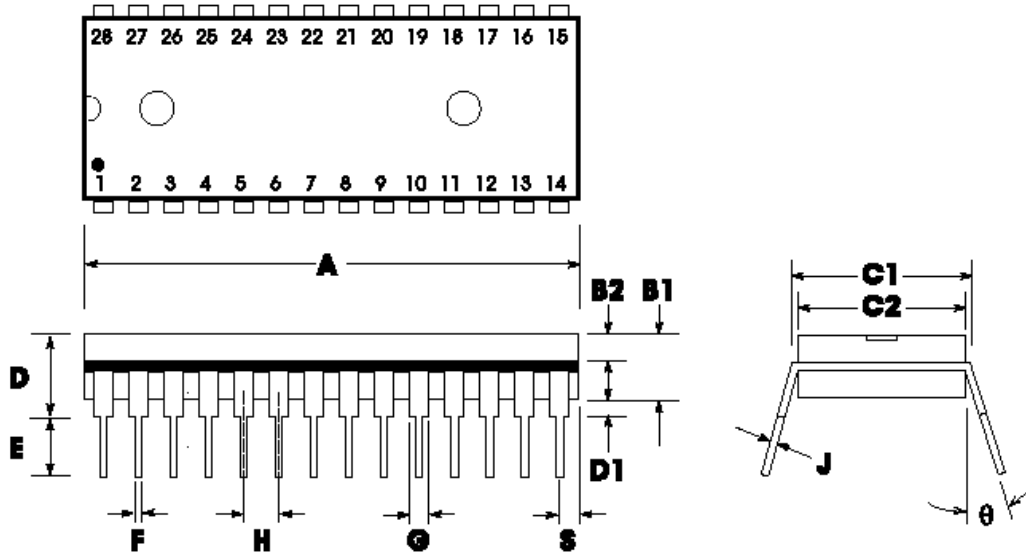
Note: Lead coplanarity to be within 0.004 inches.

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11.4. 28-LEAD 600-MIL PLASTIC DUAL INLINE PACKAGE (PDIP)



Plastic Dual Inline Package (PDIP) (P) Dimensions

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	1.445	1.450	1.455	36.70	36.83	36.96
B1		0.150			3.81	
B2	0.065	0.070	0.075	1.65	1.78	1.91
C1	0.600		0.625	15.24		15.88
C2	0.530	0.540	0.550	13.46	13.72	13.97
D			0.19			4.83
D1	0.015			0.38		
E	0.125		0.135	3.18		3.43
F	0.015	0.018	0.022	0.38	0.46	0.56
G	0.055	0.060	0.065	1.40	1.52	1.65
H		0.100			2.54	
J	0.008	0.010	0.012	0.20	0.25	0.30
S	0.070	0.075	0.080	1.78	1.91	2.03
theta	0°		15°	0°		15°

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11.5. ISD5116 DIE INFORMATION

ISD5116 Device

Die Dimensions

X: 4125 μm

Y: 8030 μm

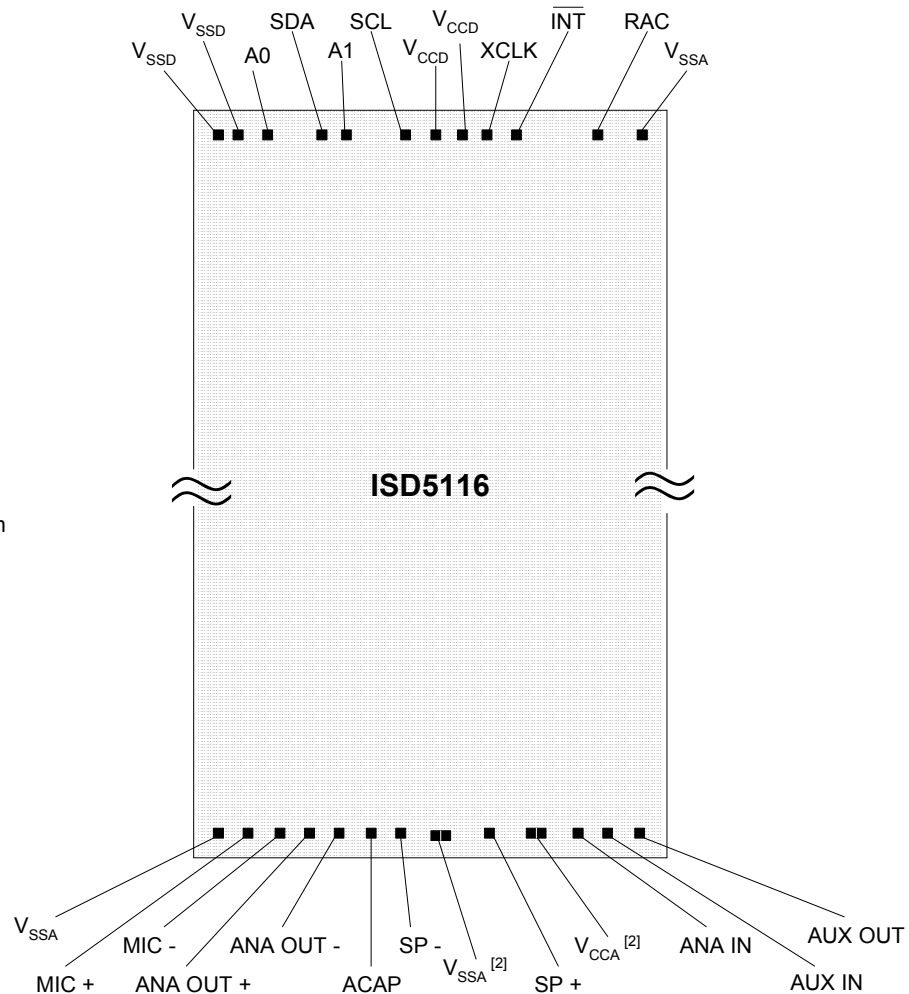
Die Thickness ^[3]

292.1 $\mu\text{m} \pm 12.7 \mu\text{m}$

Pad Opening

Single pad: 90 x 90 μm

Double pad: 180 x 90 μm



Notes

1. The backside of die is internally connected to V_{SS}. It MUST NOT be connected to any other potential or damage may occur.
2. Double bond recommended, if treated as single doubled-pad.
3. This figure reflects the current die thickness. Please contact Nuvoton as this thickness may change in the future.

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ISD5100 SERIES**nuvoTon****ISD5116 Pad Coordinates**(with respect to die center in μm)

Pad	Pad Name	X Axis	Y Axis
V _{SSA}	Analog Ground	1879.45	3848.65
RAC	Row Address Clock	1536.20	3848.65
$\overline{\text{INT}}$	Interrupt	787.40	3848.65
XCLK	External Clock Input	475.60	3848.65
V _{CCD}	Digital Supply Voltage	288.60	3848.65
V _{CCD}	Digital Supply Voltage	73.20	3848.65
SCL	Serial Clock Line	-201.40	3848.65
A1	Address 1	-560.90	3848.65
SDA	Serial Data Address	-818.20	3848.65
A0	Address 0	-1369.40	3848.65
V _{SSD}	Digital Ground	-1671.30	3848.65
V _{SSD}	Digital Ground	-1842.90	3848.65
V _{SSA}	Analog Ground	-1948.00	-3841.60
MIC+	Non-inverting Microphone Input	-1742.20	-3841.60
MIC-	Inverting Microphone Input	-1509.70	-3841.60
ANA OUT+	Non-inverting Analog Output	-1248.00	-3841.60
ANA OUT-	Inverting Analog Output	-913.80	-3841.60
ACAP	AGC/AutoMute Cap	-626.50	-3841.60
SP-	Speaker Negative	-130.70	-3841.60
V _{SSA}	Analog Ground	202.90	-3841.60
V _{SSA}	Analog Ground	292.90	-3841.60
SP+	Speaker Positive	626.50	-3841.60
V _{CCA}	Analog Supply Voltage	960.10	-3841.60
V _{CCA}	Analog Supply Voltage	1050.10	-3841.60
ANA IN	Analog Input	1257.40	-3841.60
AUX IN	Auxiliary Input	1523.00	-3841.60
AUX OUT	Auxiliary Output	1767.20	-3841.60

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11.6. ISD5108 DIE INFORMATION

ISD5108 Device

Die Dimensions (include scribe line)

X: 4230 μm

Y: 6090 μm

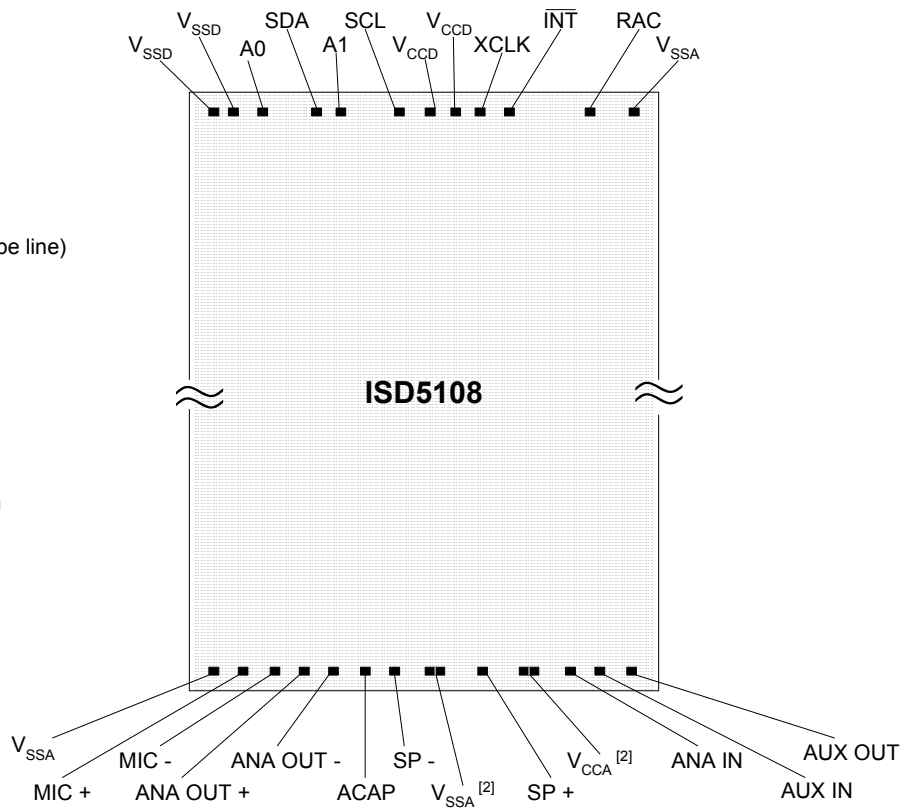
Die Thickness ^[3]

292.1 $\mu\text{m} \pm 12.7 \mu\text{m}$

Pad Opening

Single pad: 90 x 90 μm

Double pad: 180 x 90 μm



Notes

1. The backside of die is internally connected to Vss. It MUST NOT be connected to any other potential or damage may occur.
2. Double bond recommended, if treated as single doubled-pad.
3. This figure reflects the current die thickness. Please contact Nuvoton as this thickness may change in the future.

ISD5100 SERIES**nuvoTon****ISD5108 Pad Coordinates**(with respect to die center in μm)

Pad	Pad Name	X Axis	Y Axis
V _{SSA}	Analog Ground	1882.40	2820.65
RAC	Row Address Clock	1539.15	2820.65
$\overline{\text{INT}}$	Interrupt	790.35	2820.65
XCLK	External Clock Input	478.55	2820.65
V _{CCD}	Digital Supply Voltage	291.55	2820.65
V _{CCD}	Digital Supply Voltage	76.15	2820.65
SCL	Serial Clock Line	-198.45	2820.65
A1	Address 1	-557.95	2820.65
SDA	Serial Data Address	-815.25	2820.65
A0	Address 0	-1366.45	2820.65
V _{SSD}	Digital Ground	-1668.35	2820.65
V _{SSD}	Digital Ground	-1839.95	2820.65
V _{SSA}	Analog Ground	-1945.05	-2821.60
MIC+	Non-inverting Microphone Input	-1739.25	-2821.60
MIC-	Inverting Microphone Input	-1506.75	-2821.60
ANA OUT+	Non-inverting Analog Output	-1245.05	-2821.60
ANA OUT-	Inverting Analog Output	-910.85	-2821.60
ACAP	AGC/AutoMute Cap	-623.55	-2821.60
SP-	Speaker Negative	-127.75	-2821.60
V _{SSA}	Analog Ground	205.85	-2821.60
V _{SSA}	Analog Ground	295.85	-2821.60
SP+	Speaker Positive	629.45	-2821.60
V _{CCA}	Analog Supply Voltage	963.05	-2821.60
V _{CCA}	Analog Supply Voltage	1053.05	-2821.60
ANA IN	Analog Input	1260.35	-2821.60
AUX IN	Auxiliary Input	1525.95	-2821.60
AUX OUT	Auxiliary Output	1770.15	-2821.60

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11.7. ISD5104 DIE INFORMATION

ISD5104 Device

Die Dimensions (include scribe line)

X: 4230 μm

Y: 5046 μm

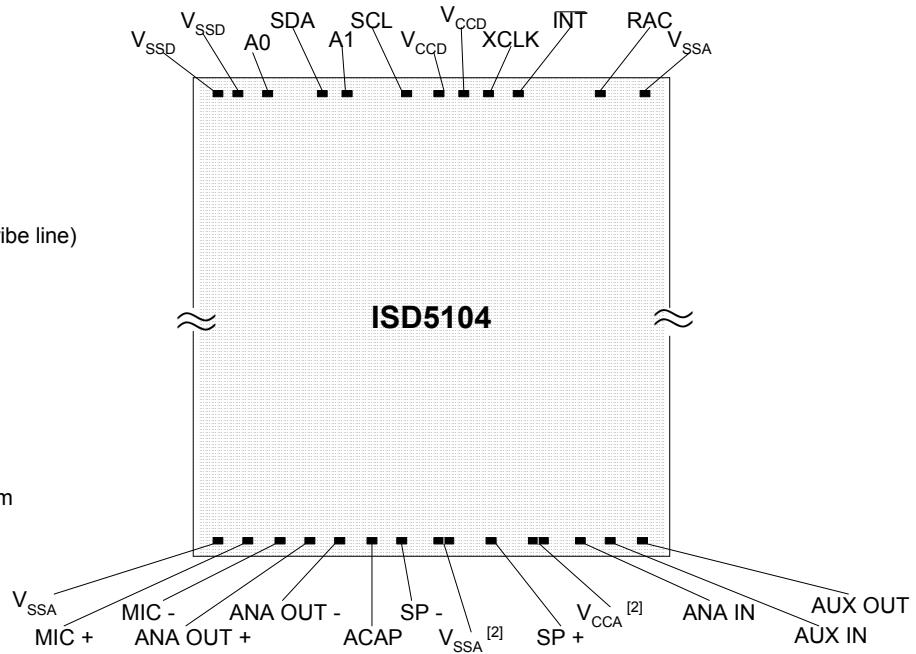
Die Thickness ^[3]

292.1 $\mu\text{m} \pm 12.7 \mu\text{m}$

Pad Opening

Single pad: 90 x 90 μm

Double pad: 180 x 90 μm



Notes

1. The backside of die is internally connected to Vss. It MUST NOT be connected to any other potential or damage may occur.
2. Double bond recommended, if treated as single doubled-pad.
3. This figure reflects the current die thickness. Please contact Nuvoton as this thickness may change in the future.

ISD5100 SERIES**nuvoTon****ISD5104 Pad Coordinates**(with respect to die center in μm)

Pad	Pad Name	X Axis	Y Axis
V _{SSA}	Analog Ground	1882.4	2306.65
RAC	Row Address Clock	1539.15	2306.65
$\overline{\text{INT}}$	Interrupt	790.35	2306.65
XCLK	External Clock Input	478.55	2306.65
V _{CCD}	Digital Supply Voltage	291.55	2306.65
V _{CCD}	Digital Supply Voltage	76.15	2306.65
SCL	Serial Clock Line	-198.45	2306.65
A1	Address 1	-557.95	2306.65
SDA	Serial Data Address	-815.25	2306.65
A0	Address 0	-1366.45	2306.65
V _{SSD}	Digital Ground	-1839.95	2306.65
V _{SSD}	Digital Ground	-1668.35	2306.65
V _{SSA}	Analog Ground	-1945.05	-2311.60
MIC+	Non-inverting Microphone Input	-1739.25	-2311.60
MIC-	Inverting Microphone Input	-1506.75	-2311.60
ANA OUT+	Non-inverting Analog Output	-1245.05	-2311.60
ANA OUT-	Inverting Analog Output	-910.85	-2311.60
ACAP	AGC/AutoMute Cap	-623.55	-2311.60
SP-	Speaker Negative	-127.75	-2311.60
V _{SSA}	Analog Ground	205.85	-2311.60
V _{SSA}	Analog Ground	295.85	-2311.60
SP+	Speaker Positive	629.45	-2311.60
V _{CCA}	Analog Supply Voltage	963.05	-2311.60
V _{CCA}	Analog Supply Voltage	1053.05	-2311.60
ANA IN	Analog Input	1260.35	-2311.60
AUX IN	Auxiliary Input	1525.95	-2311.60
AUX OUT	Auxiliary Output	1770.15	-2311.60

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11.8. ISD5102 DIE INFORMATION

ISD5102 Device

Die Dimensions (include scribe line)

X: 4230 μm

Y: 5046 μm

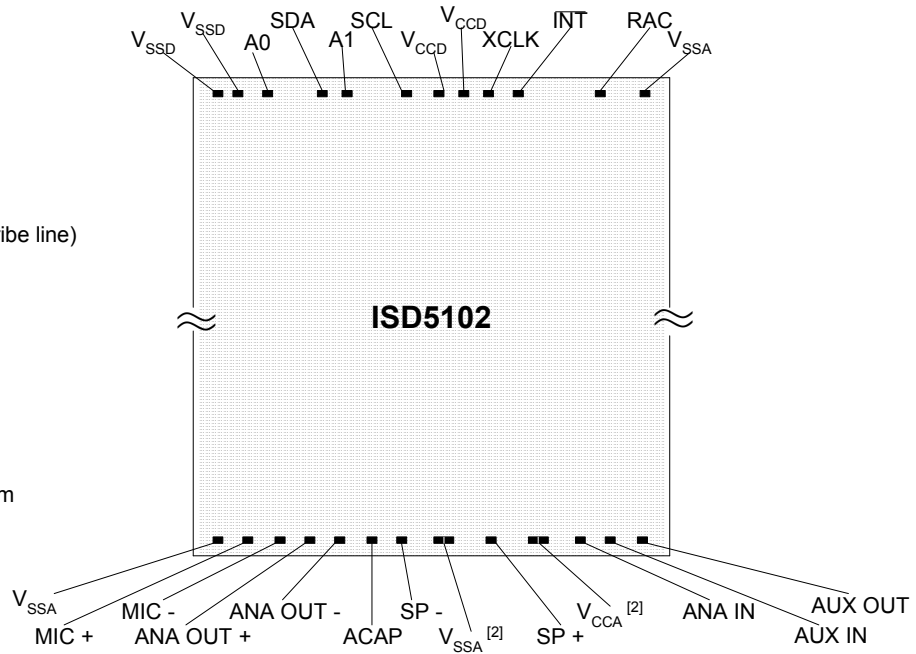
Die Thickness ^[3]

292.1 $\mu\text{m} \pm 12.7 \mu\text{m}$

Pad Opening

Single pad: 90 x 90 μm

Double pad: 180 x 90 μm



Notes

1. The backside of die is internally connected to Vss. It MUST NOT be connected to any other potential or damage may occur.
2. Double bond recommended, if treated as single doubled-pad.
3. This figure reflects the current die thickness. Please contact Nuvoton as this thickness may change in the future.

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ISD5100 SERIES**nuvoTon****ISD5102 Pad Coordinates**(with respect to die center in μm)

Pad	Pad Name	X Axis	Y Axis
V _{SSA}	Analog Ground	1882.4	2306.65
RAC	Row Address Clock	1539.15	2306.65
$\overline{\text{INT}}$	Interrupt	790.35	2306.65
XCLK	External Clock Input	478.55	2306.65
V _{CCD}	Digital Supply Voltage	291.55	2306.65
V _{CCD}	Digital Supply Voltage	76.15	2306.65
SCL	Serial Clock Line	-198.45	2306.65
A1	Address 1	-557.95	2306.65
SDA	Serial Data Address	-815.25	2306.65
A0	Address 0	-1366.45	2306.65
V _{SSD}	Digital Ground	-1839.95	2306.65
V _{SSD}	Digital Ground	-1668.35	2306.65
V _{SSA}	Analog Ground	-1945.05	-2311.60
MIC+	Non-inverting Microphone Input	-1739.25	-2311.60
MIC-	Inverting Microphone Input	-1506.75	-2311.60
ANA OUT+	Non-inverting Analog Output	-1245.05	-2311.60
ANA OUT-	Inverting Analog Output	-910.85	-2311.60
ACAP	AGC/AutoMute Cap	-623.55	-2311.60
SP-	Speaker Negative	-127.75	-2311.60
V _{SSA}	Analog Ground	205.85	-2311.60
V _{SSA}	Analog Ground	295.85	-2311.60
SP+	Speaker Positive	629.45	-2311.60
V _{CCA}	Analog Supply Voltage	963.05	-2311.60
V _{CCA}	Analog Supply Voltage	1053.05	-2311.60
ANA IN	Analog Input	1260.35	-2311.60
AUX IN	Auxiliary Input	1525.95	-2311.60
AUX OUT	Auxiliary Output	1770.15	-2311.60

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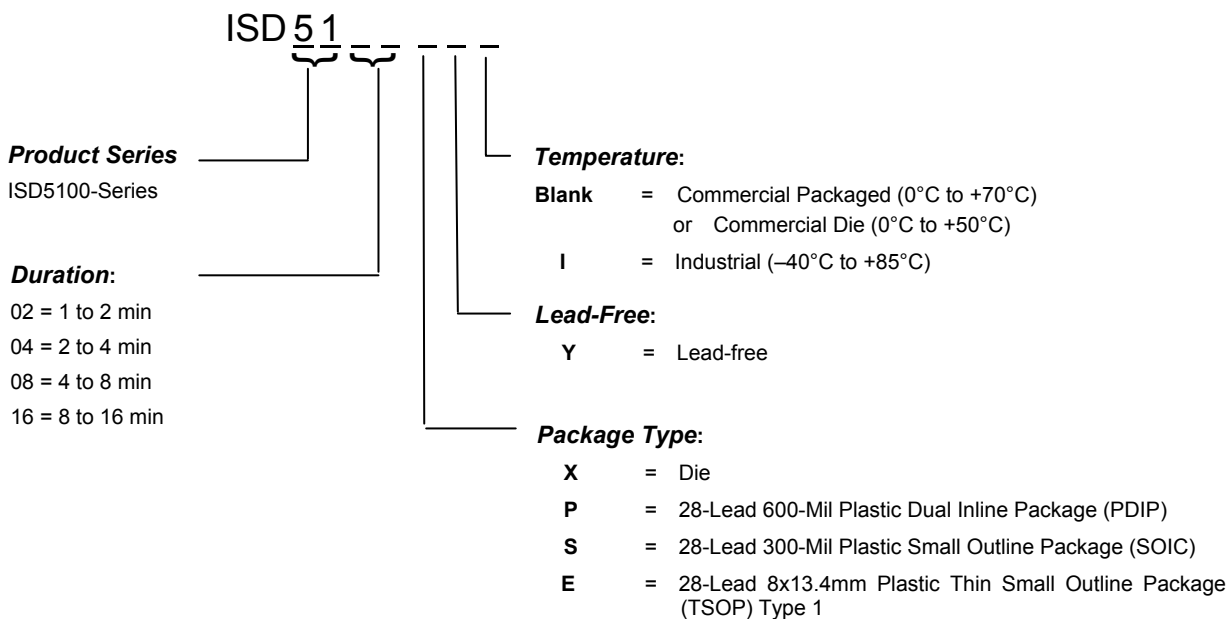
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12. ORDERING INFORMATION

Nuvoton Part Number Description



When ordering the devices, please refer to the following valid ordering numbers. For the shaded part numbers, please contact the local Nuvoton Sales Representatives for availability.

Type	Duration Package	ISD5102		ISD5104		ISD5108		ISD5116	
		Part #	Order #	Part #	Order #	Part #	Order #	Part #	Order #
	Die	ISD5102X	I5102X	ISD5104X	I5104X	ISD5108X	I5108X	ISD5116X	I5116X
Lead-Free	PDIP	N/A	N/A	N/A	N/A	N/A	N/A	ISD5116PY	I5116PY
	SOIC	ISD5102SY	I5102SY	ISD5104SY	I5104SY	ISD5108SY	I5108SY	ISD5116SY	I5116SY
		ISD5102SYI	I5102SY I	ISD5104SYI	I5104SY I	ISD5108SY I	I5108SY I	ISD5116SYI	I5116SY I
	TSOP	ISD5102EY	I5102EY	ISD5104EY	I5104EY	ISD5108EY	I5108EY	ISD5116EY	I5116EY
		ISD5102EYI	I5102EY I	ISD5104EYI	I5104EY I	ISD5108EY I	I5108EY I	ISD5116EYI	I5116EY I

For the latest product information, access Nuvoton's worldwide website at <http://www.Nuvoton-usa.com>

ISD5100 SERIES**13. VERSION HISTORY**

VERSION	DATE	DESCRIPTION
0.1	Mar 2003	New data sheet for the ISD5100-Series
0.2	Oct 2003	Add I5102 and I5104 products Utilize TAD application in Functional Details Reserve Load Address feature for factory uses Simplify Playback mode AnalIn: add k Ω for Ra & Rb AuxIn: add k Ω for Ra & Rb, remove duplicate diagram, correct parameter names in gain setting table & fix typos Add application diagram Add PCB layout example for TSOP package I ² C protocol: revise R/W bit =1 for reading status Packaging: revise unit to mil instead of inch for SOIC & PDIP Fix other typos
1.0	Jul 2004	Vcc: Industrial temp: 2.7 – 3.3V (5108: 2.7- 3.6V) Section 7.3.10 CFG0: Select 8 Ω speaker output Section 7.6.2 AuxOut: Correct parameter name to OPA1 Application diagram: Revise pin # on SDA & A1
1.1	Nov 2004	Revise Operating conditions sections Add Pb-free option to Ordering Info
1.2	Apr 2005	Revise Ordering Info section Update disclaim section
1.3	Oct. 2005	Revise Packaging information.
1.4	May. 2007	Remove leaded package offer Update XCLK description Revise application diagram
1.42	Oct 31, 2008	Change logo.

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