

Freescale Semiconductor

MPX12
Rev 11, 07/2009

10 kPa Uncompensated Silicon Pressure Sensors

The MPX12 series silicon piezoresistive pressure sensors provide a very accurate and linear voltage output, directly proportional to the applied pressure. This standard, low cost, uncompensated sensor permits manufacturers to design and add their own external temperature compensating and signal conditioning networks. Compensation techniques are simplified because of the predictability of Freescale's single element strain gauge design.

Features

- Low Cost
- Patented Silicon Shear Stress Strain Gauge Design
- Ratiometric to Supply Voltage
- Easy to Use Chip Carrier Package Options
- Gauge Options
- Durable Epoxy Package

MPX12 Series

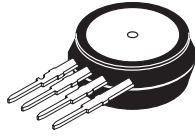
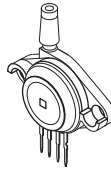
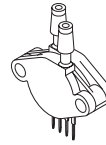
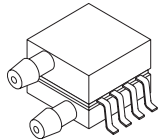
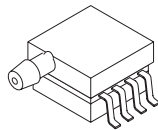
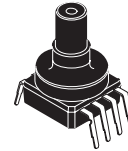
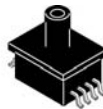
0 to 10 kPa (0 to 1.45 psi)
55 mV Full Scale Span
(Typical)

Application Examples

- Air Movement Control
- Environmental Control Systems
- Level Indicators
- Leak Detection
- Medical Instrumentation
- Industrial Controls
- Pneumatic Control Systems
- Robotics

ORDERING INFORMATION

Device Name	Package Options	Case No.	# of Ports			Pressure Type			Device Marking
			None	Single	Dual	Gauge	Differential	Absolute	
Unibody Package (MPX12 Series)									
MPX12D	Tray	344	•				•		MPX12D
MPX12DP	Tray	344C			•		•		MPX12DP
MPX12GP	Tray	344B		•		•			MPX12GP
Small Outline Package (MPXV12 Series)									
MPXV12DP	Tray	1351			•		•		MPXV12DP
MPXV12GP	Tray	1369		•		•			MPXV12GP
MPXV12GW6U	Rail	1735		•		•			MPXV12GW
MPXV12GW7U	Rail	1560		•		•			MPXV12GW
MPAK Package (MPXM12 Series)									
MPXM12GS	Rail	1320A		•		•			MPXM12GS
MPXM12GST1	Tape & Reel	1320A		•		•			MPXM12GS

UNIBODY PACKAGES**MPX12D
CASE 344-15****MPX12GP
CASE 344B-01****MPX12DP
CASE 344C-01****SMALL OUTLINE PACKAGES****MPXV12DP
CASE 1351-01****MPXV12GP
CASE 1369-01****MPXV12GW6U
CASE 1735-02****MPXV12GW7U
CASE 1560-02****MPAK PACKAGE****MPXM12GS/GST1
CASE 1320A-02**

Operating Characteristics

Table 1. Operating Characteristics ($V_S = 3.0$ Vdc, $T_A = 25^\circ\text{C}$ unless otherwise noted, $P_1 > P_2$)

Characteristic	Symbol	Min	Typ	Max	Unit
Differential Pressure Range ⁽¹⁾	P_{OP}	0	—	10	kPa
Supply Voltage ⁽²⁾	V_S	—	3.0	6.0	Vdc
Supply Current	I_o	—	6.0	—	mAdc
Full Scale Span ⁽³⁾	V_{FSS}	45	55	70	mV
Offset ⁽⁴⁾	V_{off}	0	20	35	mV
Sensitivity	$\Delta V/\Delta P$	—	5.5	—	mV/kPa
Linearity	—	-0.5	—	5.0	% V_{FSS}
Pressure Hysteresis ⁽⁶⁾ (0 to 10 kPa)	—	—	± 0.1	—	% V_{FSS}
Temperature Hysteresis (-40°C to $+125^\circ\text{C}$)	—	—	± 0.5	—	% V_{FSS}
Temperature Coefficient of Full Scale Span	TCV_{FSS}	-0.22	—	-0.16	% $V_{FSS}/^\circ\text{C}$
Temperature Coefficient of Offset	TCV_{off}	—	± 15	—	$\mu\text{V}/^\circ\text{C}$
Temperature Coefficient of Resistance	TCR	0.21	—	0.27	% $Z_{in}/^\circ\text{C}$
Input Impedance	Z_{in}	400	—	550	Ω
Output Impedance	Z_{out}	750	—	1250	Ω
Response Time ⁽⁵⁾ (10% to 90%)	t_R	—	1.0	—	ms
Warm-Up Time ⁽⁶⁾	—	—	20	—	ms
Offset Stability ⁽⁷⁾	—	—	± 0.5	—	% V_{FSS}

1. 1.0 kPa (kiloPascal) equals 0.145 psi.
2. Device is ratiometric within this specified excitation range. Operating the device above the specified excitation range may induce additional error due to device self-heating.
3. Full Scale Span (V_{FSS}) is defined as the algebraic difference between the output voltage at full rated pressure and the output voltage at the minimum related pressure.
4. Offset (V_{OFF}) is defined as the output voltage at the minimum rated pressure.
5. Response Time is defined as the time from the incremental change in the output to go from 10% to 90% of its final value when subjected to a specified step change in pressure.
6. Warm-up Time is defined as the time required for the product to meet the specified output voltage after the pressure is stabilized.
7. Offset stability is the product's output deviation when subjected to 1000 hours of Pulsed Pressure, Temperature Cycling with Bias Test.

Maximum Ratings

Table 2. Maximum Ratings⁽¹⁾

Rating	Symbol	Value	Unit
Maximum Pressure ($P_1 > P_2$)	P_{MAX}	75	kPa
Burst Pressure ($P_1 > P_2$)	P_{BURST}	100	kPa
Storage Temperature	T_{STG}	-40 to +125	°C
Operating Temperature	T_A	-40 to +125	°C

1. Exposure beyond the specified limits may cause permanent damage or degradation to the device.

Figure 1 shows a block diagram of the internal circuitry integrated on a pressure sensor chip.

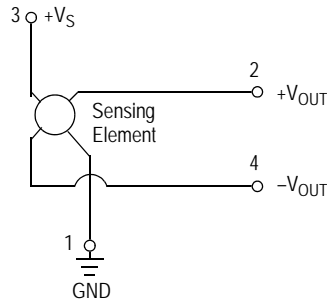


Figure 1. Uncompensated Pressure Sensor Schematic

Voltage Output versus Applied Differential Pressure

The output voltage of the differential or gauge sensor increases with increasing pressure applied to the pressure side (P_1) relative to the vacuum side (P_2). Similarly, output

voltage increases as increasing vacuum is applied to the vacuum side (P_2) relative to the pressure side (P_1).

Temperature Compensation

Figure 2 shows the typical output characteristics of the MPX12 series over temperature.

Because this strain gauge is an integral part of the silicon diaphragm, there are no temperature effects due to differences in the thermal expansion of the strain gauge and the diaphragm, as are often encountered in bonded strain gauge pressure sensors. However, the properties of the strain gauge itself are temperature dependent, requiring that the device be temperature compensated if it is to be used over an extensive temperature range.

Temperature compensation and offset calibration can be achieved rather simply with additional resistive components, or by designing your system using the MPX2010D series sensor.

Several approaches to external temperature compensation over both -40 to $+125^{\circ}\text{C}$ and 0 to $+80^{\circ}\text{C}$ ranges are presented in Applications Note AN840.

LINEARITY

Linearity refers to how well a transducer's output follows the equation: $V_{\text{OUT}} = V_{\text{OFF}} + \text{sensitivity} \times P$ over the operating pressure range (Figure 3). There are two basic methods for calculating nonlinearity: (1) end point straight line fit or (2) a least squares best line fit. While a least squares fit gives the "best case" linearity error (lower numerical value), the calculations required are burdensome.

Conversely, an end point fit will give the "worst case" error (often more desirable in error budget calculations) and the calculations are more straightforward for the user.

Freescale's specified pressure sensor linearities are based on the end point straight line method measured at the midrange pressure.

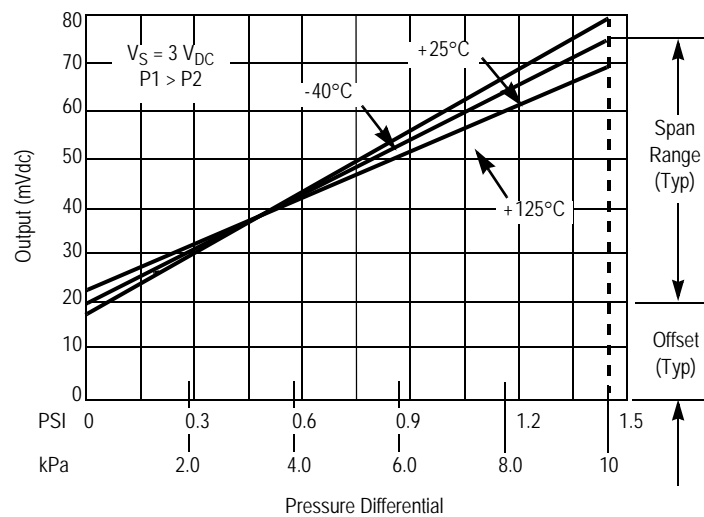


Figure 2. Output vs. Pressure Differential

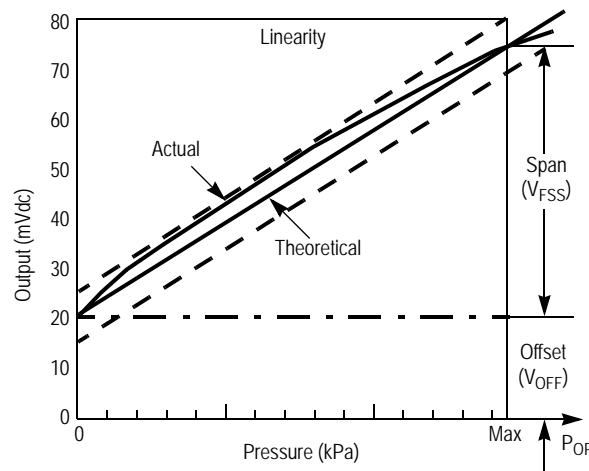


Figure 3. Linearity Specification Comparison

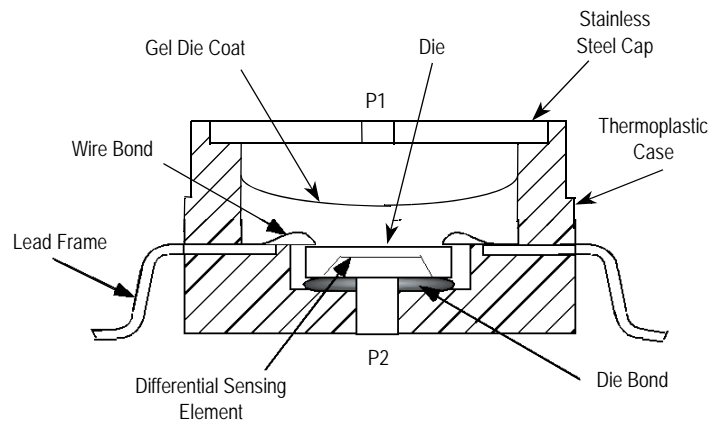


Figure 4. Cross-Sectional Diagram (not to scale)

Figure 4 illustrates the differential/gauge die. A gel isolates the die surface and wire bonds from the environment, while allowing the pressure signal to be transmitted to the silicon diaphragm.

Operating characteristics, internal reliability and qualification tests are based on use of dry clean air as the

pressure media. Media other than dry clean air may have adverse effects on sensor performance and long term reliability. Contact the factory for information regarding media compatibility in your application.

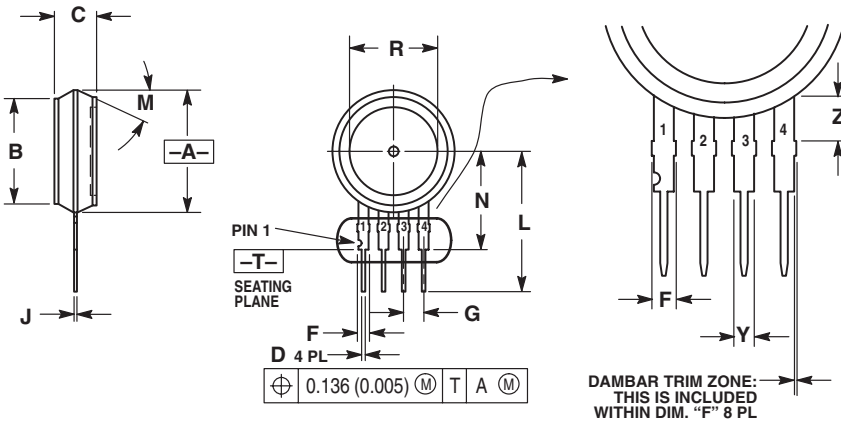
PRESSURE (P1)/VACUUM (P2) SIDE IDENTIFICATION TABLE

Freescle designates the two sides of the pressure sensor as the Pressure (P1) side and the Vacuum (P2) side. The Pressure (P1) side is the side containing gel which isolates the die from the environment. Freescle's MPx12 series is designed to operate with positive differential pressure applied, $P1 > P2$.

The Pressure (P1) side may be identified by using the following table

Part Number	Case Type	Pressure (P1) Side Identifier
MPX12D	344	Stainless Steel Cap
MPX12DP	344C	Side with Part Marking
MPX12GP	344B	Side with Port Attached
MPXV12DP	1351	Side with Part Marking
MPXV12GP	1369	Side with Port
MPXV12GW6U	1735	Side with Port
MPXV12GW7U	1560	Side with Port
MPXM12GS/GST1	1320A	Side with Port Attached

PACKAGE DIMENSIONS



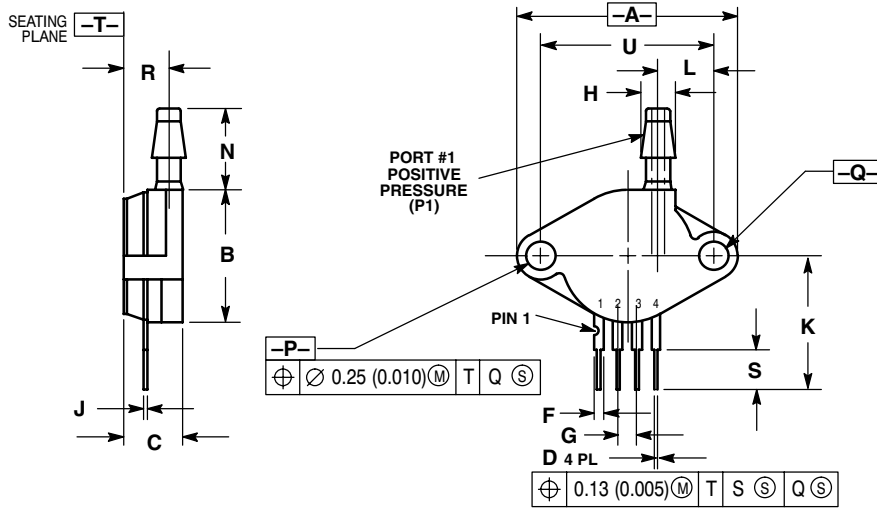
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION -A- IS INCLUSIVE OF THE MOLD STOP RING. MOLD STOP RING NOT TO EXCEED 16.00 (0.630).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.595	0.630	15.11	16.00
B	0.514	0.534	13.06	13.56
C	0.200	0.220	5.08	5.59
D	0.016	0.020	0.41	0.51
F	0.048	0.064	1.22	1.63
G	0.100 BSC		2.54 BSC	
J	0.014	0.016	0.36	0.40
L	0.695	0.725	17.65	18.42
M	30° NOM		30° NOM	
N	0.475	0.495	12.07	12.57
R	0.430	0.450	10.92	11.43
Y	0.048	0.052	1.22	1.32
Z	0.106	0.118	2.68	3.00

- STYLE 1:
 PIN 1. GROUND
 2. + OUTPUT
 3. + SUPPLY
 4. - OUTPUT
- STYLE 2:
 PIN 1. V_{CC}
 2. - SUPPLY
 3. + SUPPLY
 4. GROUND
- STYLE 3:
 PIN 1. GND
 2. -VOUT
 3. VS
 4. +VOUT

**CASE 344-15
 ISSUE AA
 UNIBODY PACKAGE**



NOTES:

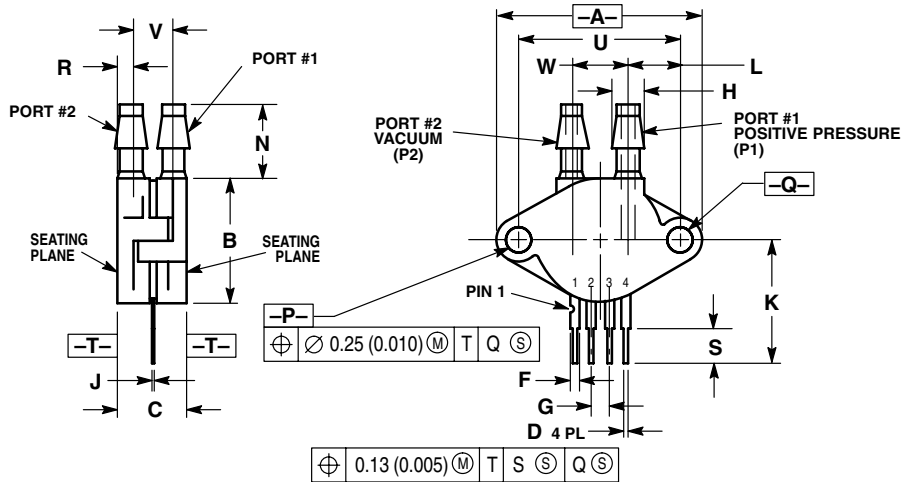
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.145	1.175	29.08	29.85
B	0.685	0.715	17.40	18.16
C	0.305	0.325	7.75	8.26
D	0.016	0.020	0.41	0.51
F	0.048	0.064	1.22	1.63
G	0.100 BSC		2.54 BSC	
H	0.182	0.194	4.62	4.93
J	0.014	0.016	0.36	0.41
K	0.695	0.725	17.65	18.42
L	0.290	0.300	7.37	7.62
N	0.420	0.440	10.67	11.18
P	0.153	0.159	3.89	4.04
Q	0.153	0.159	3.89	4.04
R	0.230	0.250	5.84	6.35
S	0.220	0.240	5.59	6.10
U	0.910 BSC		23.11 BSC	

- STYLE 1:
 PIN 1. GROUND
 2. + OUTPUT
 3. + SUPPLY
 4. - OUTPUT

**CASE 344B-01
 ISSUE B
 UNIBODY PACKAGE**

PACKAGE DIMENSIONS



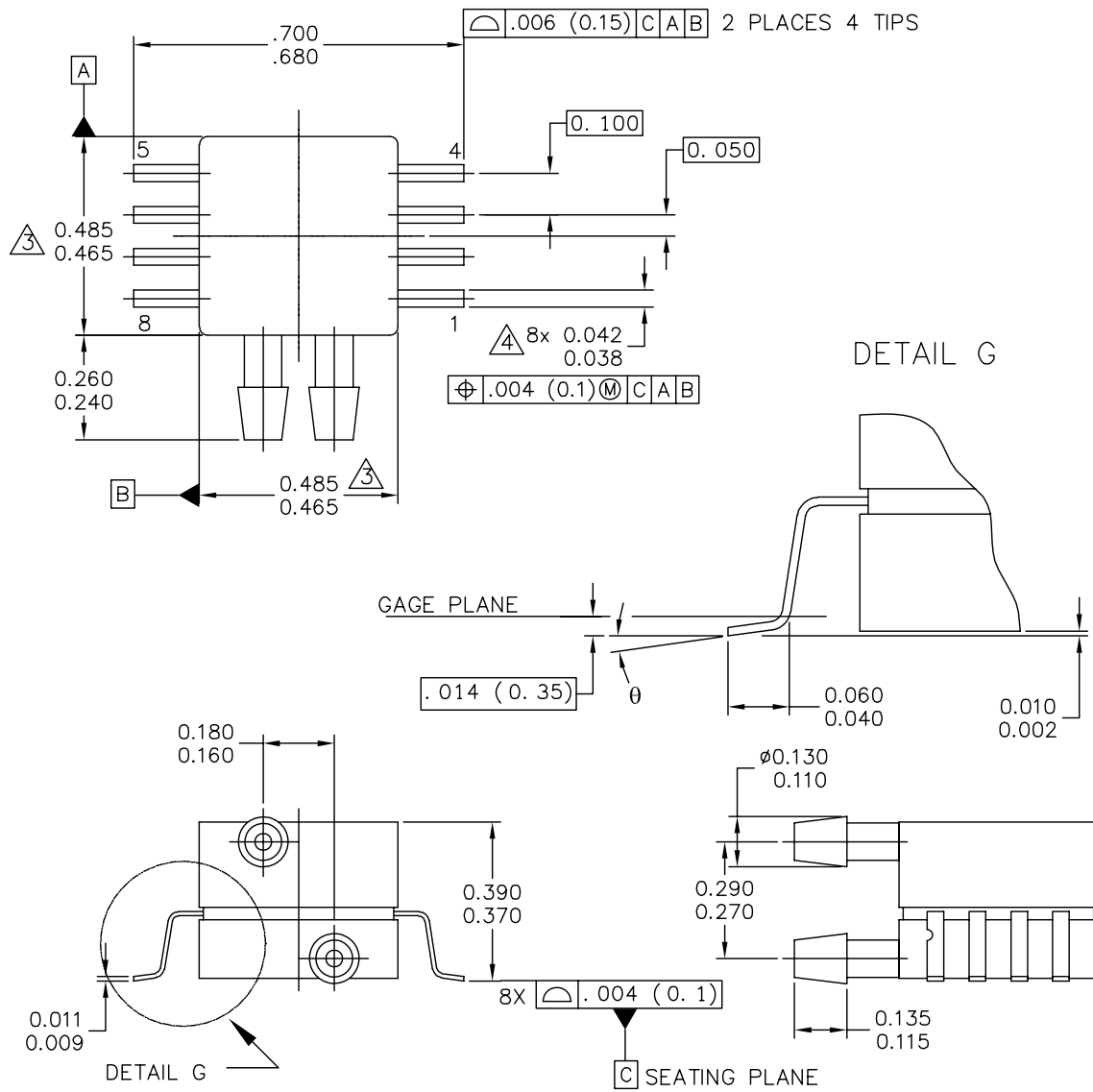
NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.145	1.175	29.08	29.85
B	0.685	0.715	17.40	18.16
C	0.405	0.435	10.29	11.05
D	0.016	0.020	0.41	0.51
F	0.048	0.064	1.22	1.63
G	0.100 BSC		2.54 BSC	
H	0.182	0.194	4.62	4.93
J	0.014	0.016	0.36	0.41
K	0.695	0.725	17.65	18.42
L	0.290	0.300	7.37	7.62
N	0.420	0.440	10.67	11.18
P	0.153	0.159	3.89	4.04
Q	0.153	0.159	3.89	4.04
R	0.063	0.083	1.60	2.11
S	0.220	0.240	5.59	6.10
U	0.910 BSC		23.11 BSC	
V	0.248	0.278	6.30	7.06
W	0.310	0.330	7.87	8.38

STYLE 1:
 PIN 1. GROUND
 2. + OUTPUT
 3. + SUPPLY
 4. - OUTPUT

**CASE 344C-01
 ISSUE B
 UNIBODY PACKAGE**

PACKAGE DIMENSIONS



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: 8 LD SNSR, DUAL PORT	DOCUMENT NO: 98ASA99255D	REV: A	
	CASE NUMBER: 1351-01	27 JUL 2005	
	STANDARD: NON-JEDEC		

**CASE 1351-01
ISSUE A
SMALL OUTLINE PACKAGE**

PACKAGE DIMENSIONS

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

3. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH AND PROTRUSIONS SHALL NOT EXCEED .006 PER SIDE.

4. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR
PROTRUSION SHALL BE .008 MAXIMUM.

STYLE 1:

PIN 1: GND
PIN 2: +Vout
PIN 3: Vs
PIN 4: -Vout
PIN 5: N/C
PIN 6: N/C
PIN 7: N/C
PIN 8: N/C

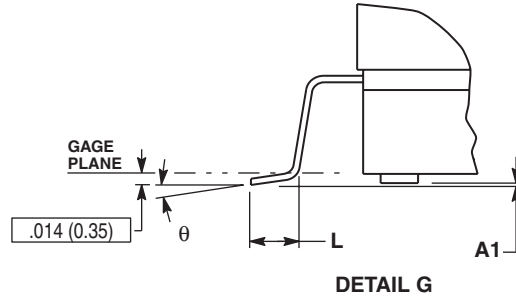
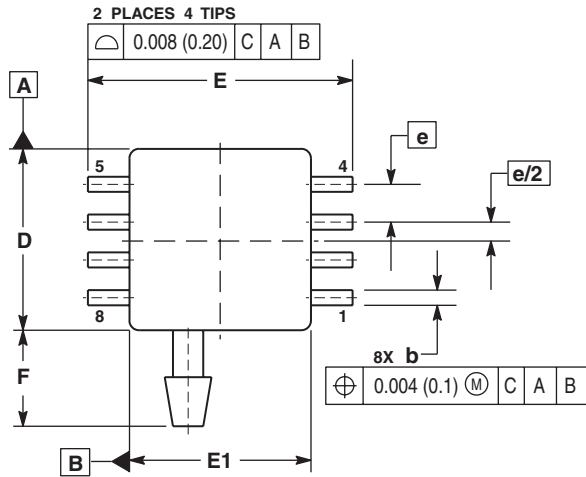
STYLE 2:

PIN 1: N/C
PIN 2: Vs
PIN 3: GND
PIN 4: Vout
PIN 5: N/C
PIN 6: N/C
PIN 7: N/C
PIN 8: N/C

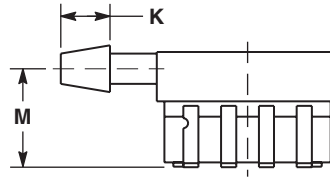
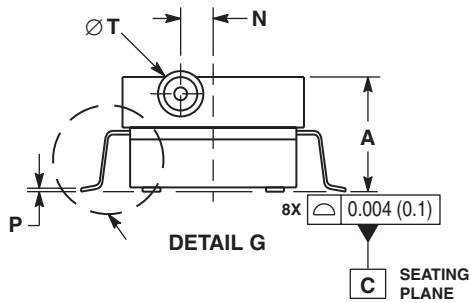
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: 8 LD SNSR, DUAL PORT	DOCUMENT NO: 98ASA99255D	REV: A	
	CASE NUMBER: 1351-01	27 JUL 2005	
	STANDARD: NON-JEDEC		

**CASE 1351-01
ISSUE A
SMALL OUTLINE PACKAGE**

PACKAGE DIMENSIONS



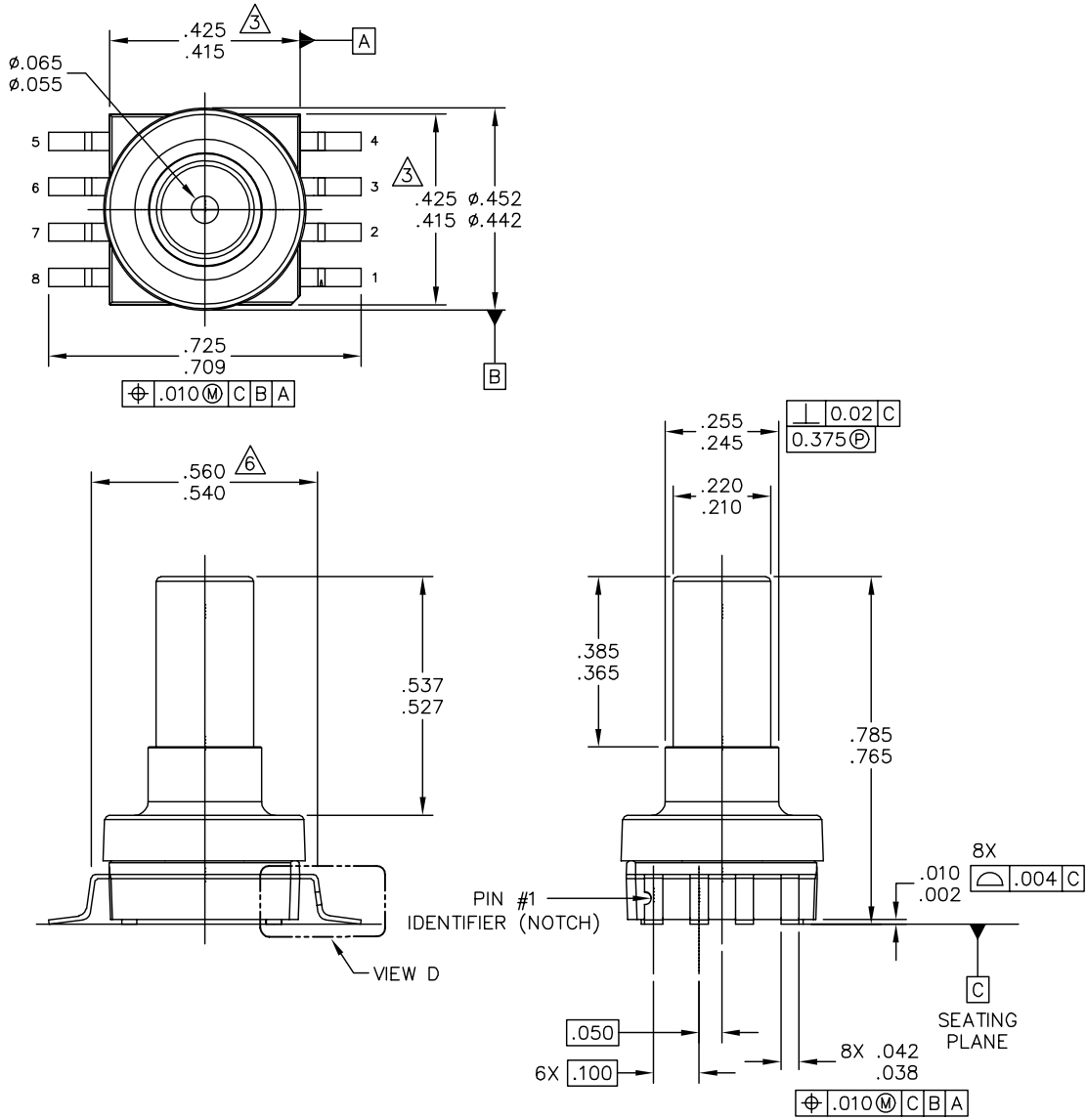
- NOTES:
1. CONTROLLING DIMENSION: INCH.
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
 3. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 (0.152) PER SIDE.
 4. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.008 (0.203) MAXIMUM.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.300	0.330	7.11	7.62
A1	0.002	0.010	0.05	0.25
b	0.038	0.042	0.96	1.07
D	0.465	0.485	11.81	12.32
E	0.717 BSC		18.21 BSC	
E1	0.465	0.485	11.81	12.32
e	0.100 BSC		2.54 BSC	
F	0.245	0.255	6.22	6.47
K	0.120	0.130	3.05	3.30
L	0.061	0.071	1.55	1.80
M	0.270	0.290	6.86	7.36
N	0.080	0.090	2.03	2.28
P	0.009	0.011	0.23	0.28
T	0.115	0.125	2.92	3.17
θ	0°	7°	0°	7°

CASE 1369-01
 ISSUE O
 SMALL OUTLINE PACKAGE

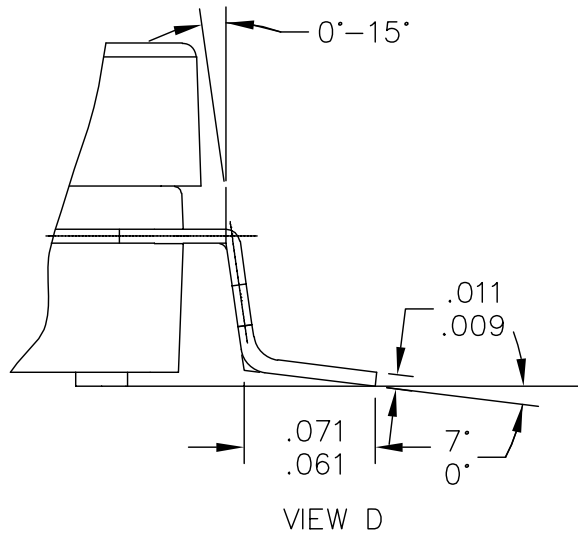
PACKAGE DIMENSIONS



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: SO, 8 I/O, .420 X .420 PKG, .100 IN PITCH	DOCUMENT NO: 98ASA10686D	REV: B	
	CASE NUMBER: 1735-02	19 FEB 2009	
	STANDARD: NON-JEDEC		

**CASE 1735-02
ISSUE B
SMALL OUTLINE PACKAGE**

PACKAGE DIMENSIONS



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: SO, 8 I/O, .420 X .420 PKG, .100 IN PITCH	DOCUMENT NO: 98ASA10686D	REV: B	
	CASE NUMBER: 1735-02	19 FEB 2009	
	STANDARD: NON-JEDEC		

**CASE 1735-02
ISSUE B
SMALL OUTLINE PACKAGE**

PACKAGE DIMENSIONS

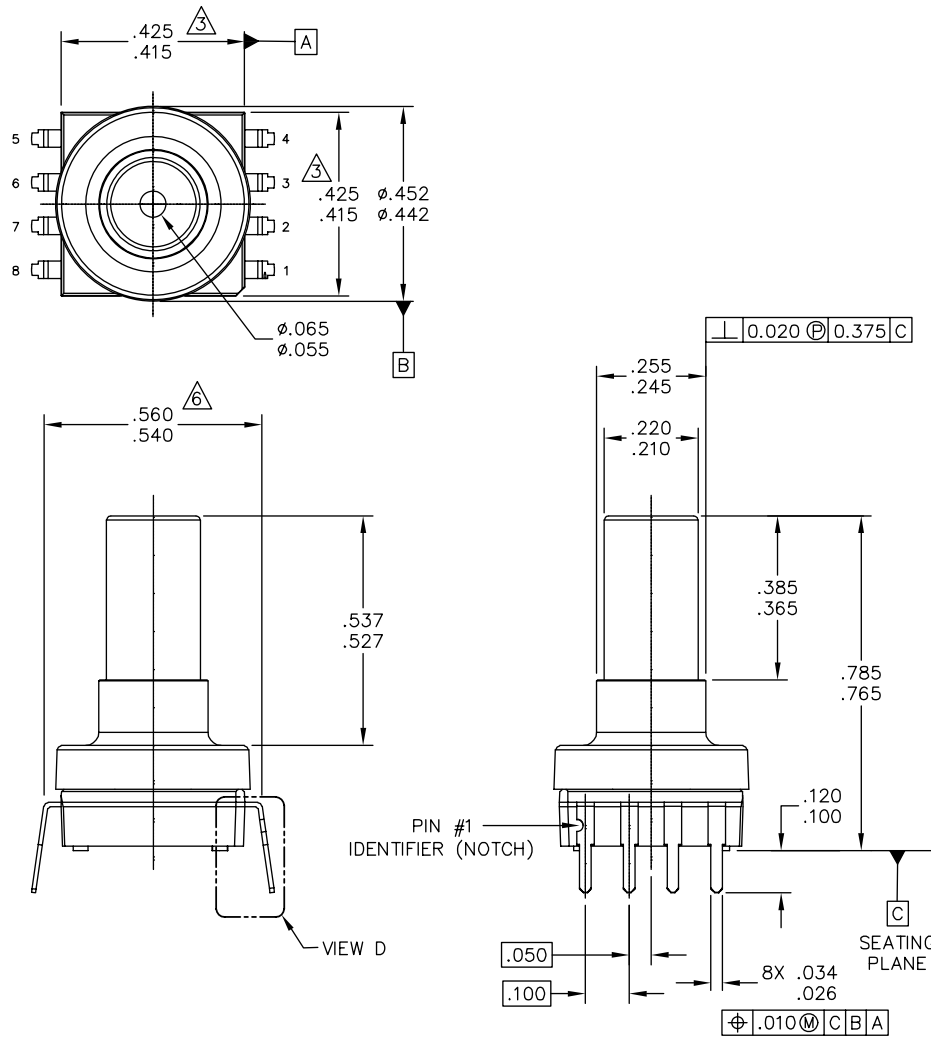
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M – 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION IS .006.
5. ALL VERTICAL SURFACES 5° TYPICAL DRAFT.
6. DIMENSION TO CENTER OF LEAD WHEN FORMED PARALLEL.

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: SO, 8 I/O, .420 X .420 PKG, .100 IN PITCH	DOCUMENT NO: 98ASA10686D	REV: B	
	CASE NUMBER: 1735-02	19 FEB 2009	
	STANDARD: NON-JEDEC		

**CASE 1735-02
ISSUE B
SMALL OUTLINE PACKAGE**

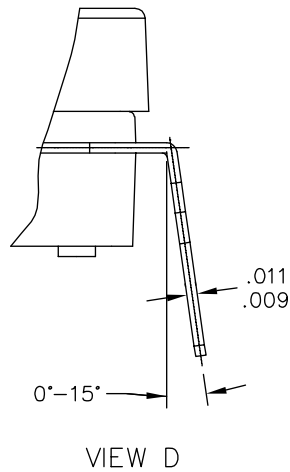
PACKAGE DIMENSIONS



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: SO, 8 I/O, .420 X .420 PKG, .100 IN PITCH	DOCUMENT NO: 98ASA10611D	REV: D	
	CASE NUMBER: 1560-03	25 FEB 2009	
	STANDARD: NON-JEDEC		

**CASE 1560-03
ISSUE D
SMALL OUTLINE PACKAGE**

PACKAGE DIMENSIONS



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: SO, 8 I/O, .420 X .420 PKG, .100 IN PITCH	DOCUMENT NO: 98ASA10611D	REV: D	
	CASE NUMBER: 1560-03	25 FEB 2009	
	STANDARD: NON-JEDEC		

**CASE 1560-03
ISSUE D
SMALL OUTLINE PACKAGE**

PACKAGE DIMENSIONS

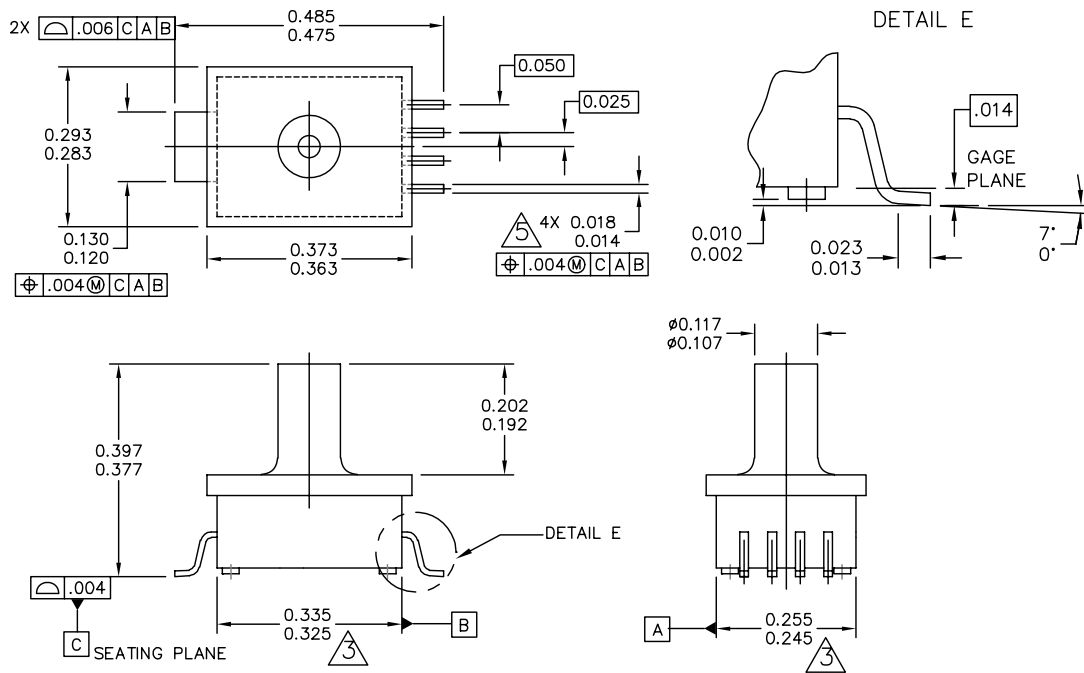
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M – 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION IS .006.
5. ALL VERTICAL SURFACES 5° TYPICAL DRAFT.
6. DIMENSION TO CENTER OF LEAD WHEN FORMED PARALLEL.

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: SO, 8 I/O, .420 X .420 PKG, .100 IN PITCH	DOCUMENT NO: 98ASA10611D	REV: D	
	CASE NUMBER: 1560-03	25 FEB 2009	
	STANDARD: NON-JEDEC		

**CASE 1560-03
ISSUE D
SMALL OUTLINE PACKAGE**

PACKAGE DIMENSIONS



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 5 LD M-PAC, PORTED	DOCUMENT NO: 98ARH99087A	REV: A
	CASE NUMBER: 1320A-02	22 JUL 2005
	STANDARD: NON-JEDEC	

**CASE 1320A-02
ISSUE A
MPAK PACKAGE**

PACKAGE DIMENSIONS

NOTES:

1. DIMENSIONS ARE IN INCHES.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

3. DIMENSIONS DOES NOT INCLUDE MOLD FLASH OR PROTRUSION. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED .006" PER SIDE.

4. ALL VERTICAL SURFACES TO BE 5" MAXIMUM.

5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .008 MAXIMUM.

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: 5 LD M-PAC, PORTED	DOCUMENT NO: 98ARH99087A	REV: A	
	CASE NUMBER: 1320A-02	22 JUL 2005	
	STANDARD: NON-JEDEC		

**CASE 1320A-02
ISSUE A
MPAK PACKAGE**

How to Reach Us:

Home Page:

www.freescale.com

Web Support:

<http://www.freescale.com/support>

USA/Europe or Locations Not Listed:

Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 010 5879 8000
support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center
1-800-441-2447 or +1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc. 2009. All rights reserved.

