HPS128-LT-S – Hybrid pyroelectric linear array with 128 responsive elements and integrated CMOS multiplexer

Description

The pyroelectric linear array 128-LT is a hybrid detector with 128 responsive elements and an integrated CMOS multiplexer.

The pyroelectric chip consists of lithium tantalate ($LiTaO_3$). The size of the responsive elements is (90 x 500) µm^2 with a pitch of 100 µm (90 x 1000 µm² available on request).

The multiplexer includes low-noise preamplifiers for each pixel, analogue switches and an output amplifier. The preamplifiers transform the signal charges of each pixel in a signal voltage, realize a band limiting and give the amplified signal to the sample&hold for the read-out process. The digital inputs are CMOS compatible.

For the measurement of the detector temperature a sensor (type AD 590) is integrated. It provides a temperature proportional current.

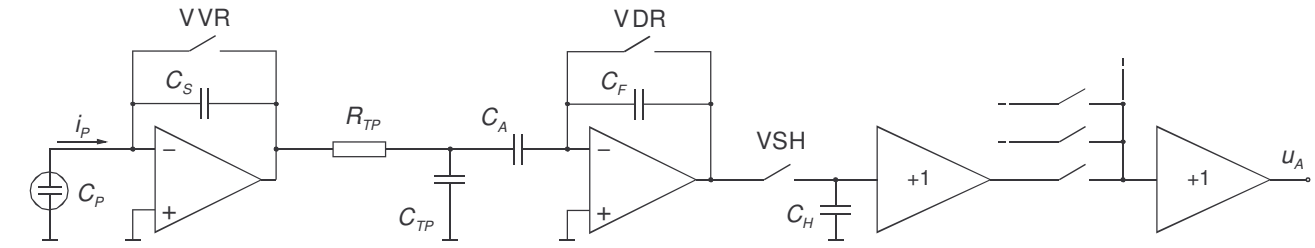
The pyroelectric chip and the read-out circuit are arranged in a metal hermetic package with an infrared window. It determines the spectral responsivity.

For the measurement of the infrared radiation it is necessary to chop the radiation flux.

Features

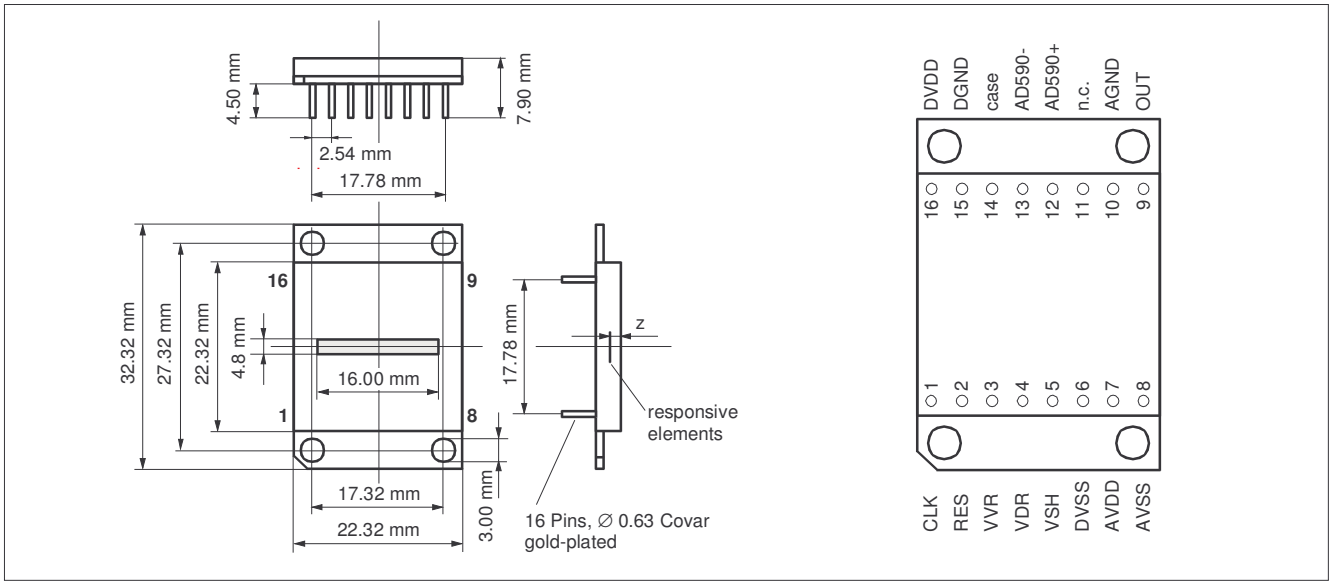
- 128 responsive elements arranged in a line
- Coated germanium or silicon as infrared window
- Broad band windows or special filters are possible on request
- NEP (128 Hz) = 7 nW (typical)
- Dynamic range > 75 dB
- Integrated CMOS multiplexed
- Good long-term stability
- Simple mode of operation
- Operation at ambient temperatures
- Small package

Readout-circuit



Detector geometry and optical specification

Package and pins



Pins

Pin number	Pin name	Remark
1	CLK	Input clock CLK
2	RES	Input clock RES
3	VVR	Input clock VVR
4	VDR	Input clock VDR
5	VSH	Input clock VSH
6	DVSS	Digital operating voltage DVSS (–5 V)
7	AVDD	Analog operating voltage AVDD (+5 V)
8	AVSS	Analog operating voltage AVSS (–5 V)
9	OUT	Analog signal output
10	AGND	Analog ground
11	n.c.	not connected
12	AD590+	Temperature sensor
13	AD590–	Temperature sensor
14	case	Case
15	DGND	Digital ground
16	DVDD	Digital operating voltage DVDD (+5 V)

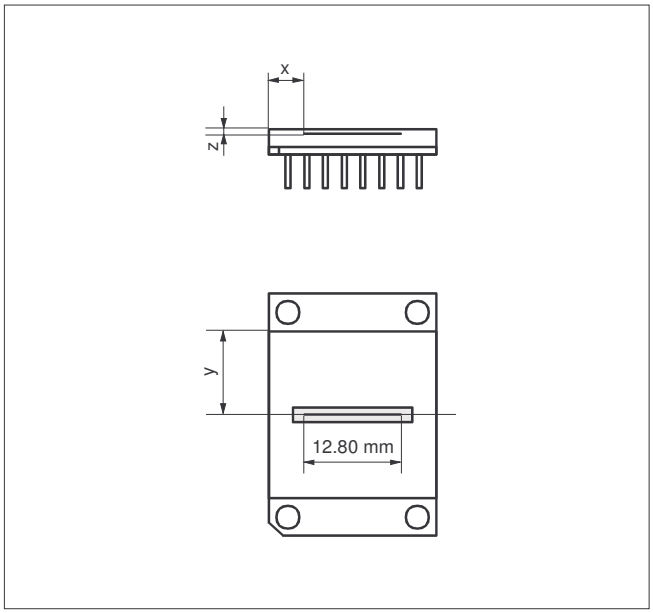
Optical Specification

Geometry

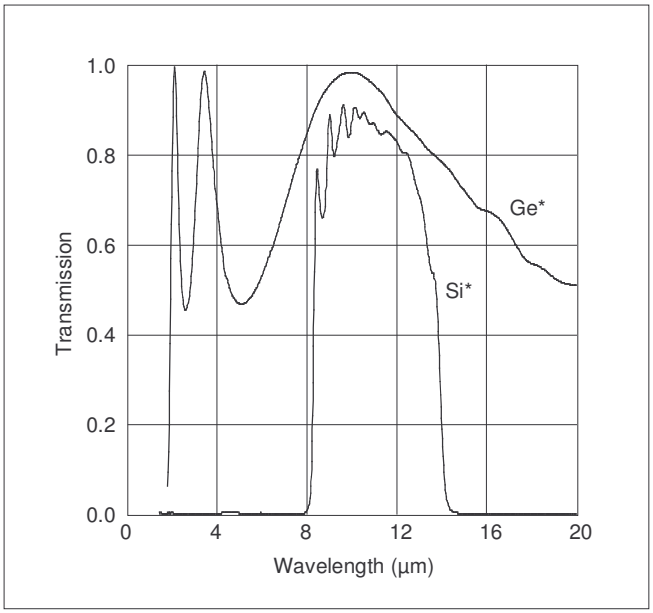
Parameter	Minimum value	Typical value	Maximum value	Unit
Field of view of each pixel[1]	90			°
Pixel width		90		µm
Pitch		100		µm
Pixel length		500		µm
Distance x	4.71	4.76	4.81	mm
Distance y	11.06	11.16	11.26	mm
Distance z	1.00	1.05	1.10	mm

[1] Perpendicular to the array

Position of the Pixels



Transmission of the germanium window



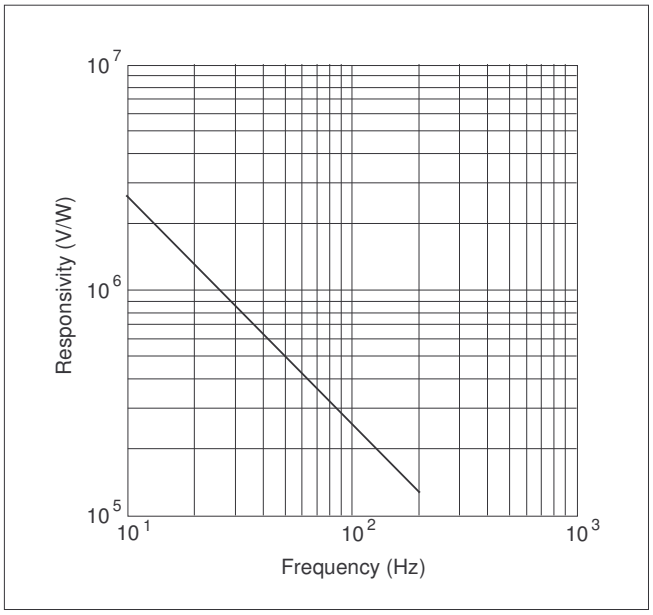
Electro-optical specification

Rectangular chopping with 128 Hz, array temperature 25 °C

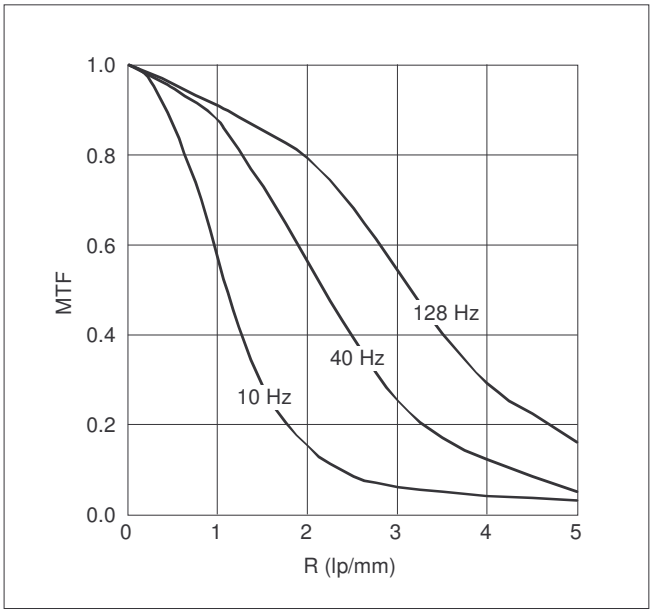
Parameter	Minimum value	Typical value	Maximum value	Unit
Responsivity S_V	140000	200000		V/W
Noise U_N		1.5	3	mV
NEP		7	15	nW
MTF (R = 3 lp/mm)	0.4	0.6		
Uniformity[1] S_V		1	3	%
Operating temperature	–15		70	°C

[1] No defective elements

Typical responsivity



Typical MTF



Electrical parameters

All values for DVDD = AVDD = 5 V, AVSS = DVSS = –5 V

Parameter	Minimum value	Typical value	Maximum value	Unit
AVDD, DVDD[1]	4.75	5.0	5.25	V
AVSS, DVSS[1]	–5.25	–5.0	–4.75	V
Digital inputs				
Low voltage	0		0.3 DVDD	V
High voltage	0.7 DVDD		DVDD	V
Switching threshold		0.5 DVDD		V
Leakage current			±1	µA
Current consumption I_{analog}		8		mA
Current consumption $I_{digital}$		30		µA
AD590 Operating voltage[2]	+4		+30	V

[1] AVDD and DVDD; AVSS and DVSS must be connect together direct at the detector, [2] See data sheet of Analog Devices

Maxiumum/minimum conditions

All voltages refer to ground (pin 15)

Parameter	Maximum/minimum value	Unit
DVDD, AVDD	–0.3 to +7	V
AVSS, DVSS	+0.3 to –7	V
Digital inputs CLK, RES, VVR, VDR, VSH	–0.3 to DVDD +0.3	V
Chopping frequency f_{Ch}	10 to 300	Hz
AD590+ to AD590– [1]	–20 to +44	V
Analog output [2]	±5	mA
Maximum irradiance	50	mW/mm^2
Soldering temperature (10 s)	300	°C
Storage temperature	–20 to 80	°C

[1] Potential free to ground (Pin 15), [2] Not short resistent

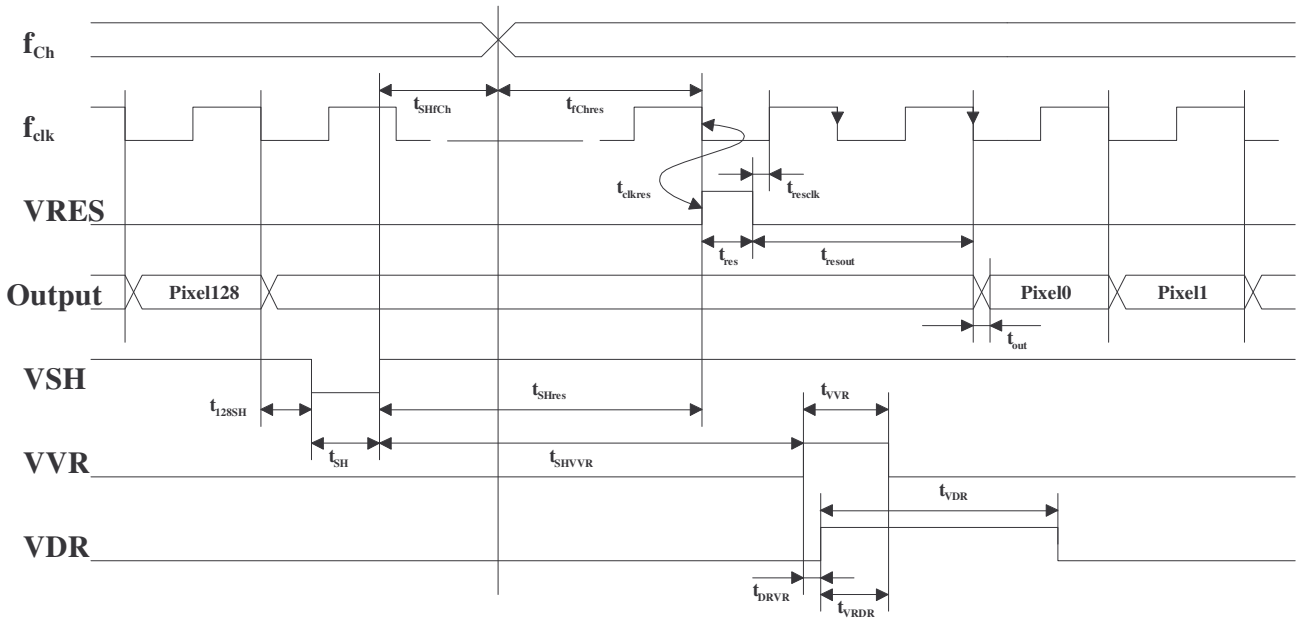
Clock parameters

All values for DVDD = AVDD = 5 V, AVSS = DVSS = –5 V

Parameter	Minimum value	Typical value	Maximum value	Unit
Chopping frequency[1] f_{Ch}	10	128	200	Hz
Ground clock[1] CLK f_{clk}	0	34.3	100	kHz
Reset clock high-impulse duration t_{res}	2.5	4		µs
Clock VVR high-impulse duration t_{VVR}	10	15		µs
Clock VDR high-impulse duration t_{VDR}	200	300		µs
Clock VSH low-impulse duration t_{SH}	10	15		µs
Settling time at the output t_{out}	3	5		µs
Setup time before clock t_{128SH}	10			µs
Time distance t_{SHres}	10			µs
Time distance t_{SHVVR}	10			µs
Time distance t_{SHfCh}	0			µs
Time distance t_{fChres}	0			µs
Time distance t_{clkres}	0			µs
Time distance t_{resclk}	1			µs
Time distance t_{resout}	1.5 t_{clk} + t_{resclk}			µs
Time distance t_{DRVR}	0			µs
Time distance t_{VRDR}	0			µs

[1] $t_{Ch\ low} = t_{Ch\ high}$

Clock diagram



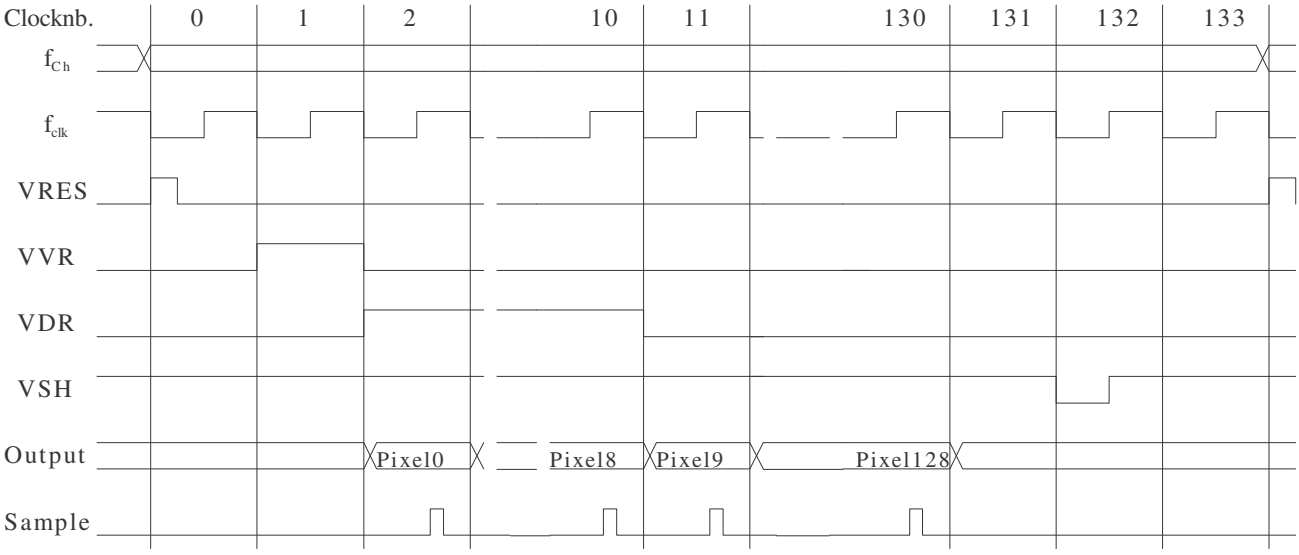
Remark: pixel 0 is an input without responsive element (dark signal)

Application remarks

Typical clock regime

Parameter	Relative value	Typical value	Unit
Chopping frequency f_{Ch}		128	Hz
Ground clock f_{clk}	$1/t_{clk}$	34 304	Hz
Reset clock high-impulse duration t_{res}	¼ t_{clk}	7.3	µs
Clock VVR high-impulse duration t_{VVR}	3 t_{clk}	29.2	µs
Clock VDR high-impulse duration t_{VDR}	10 t_{clk}	292	µs
Clock VSH low- impulse duration t_{SH}	½ t_{clk}	14.6	µs

Clock diagram



Remark: Clock 133 is for the compensation of jitter of the chopping frequency during the mechanical chopping