



Low-g Micromachined Accelerometer

The MMA series of silicon capacitive, micromachined accelerometers feature signal conditioning, a 2-pole low pass filter and temperature compensation. Zero-g offset full scale span and filter cut-off are factory set and require no external devices. A full system self-test capability verifies system functionality.

Features

- Integral Signal Conditioning
- Linear Output
- 2nd Order Bessel Filter
- Calibrated Self-test
- EPROM Parity Check Status
- Transducer Hermetically Sealed at Wafer Level for Superior Reliability
- Robust Design, High Shock Survivability
- Qualified AECQ100, Rev. F Grade 2 (-40°C/ +105°C)

Typical Applications

- Vibration Monitoring and Recording
- Appliance Control
- Mechanical Bearing Monitoring
- Computer Hard Drive Protection
- Computer Mouse and Joysticks
- Virtual Reality Input Devices
- Sports Diagnostic Devices and Systems

MMA1254

**MMA1254: Z-AXIS SENSITIVITY
 MICROMACHINED
 ACCELEROMETER
 ±5g**



ORDERING INFORMATION			
Device Name	Temperature Range	Case No.	Package
MMA1254EG	-40° to 105°C	475-01	SOIC-16
MMA1254EGR2	-40° to 105°C	475-01	SOIC-16, Tape & Reel
MMA1254KEG*	-40° to 105°C	475-01	SOIC-16
MMA1254KEGR2*	-40° to 105°C	475-01	SOIC-16, Tape & Reel

*Part number sourced from a different facility.

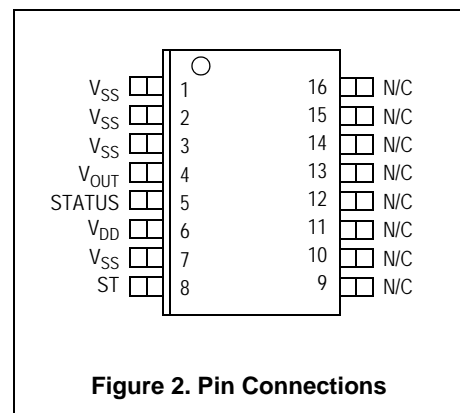
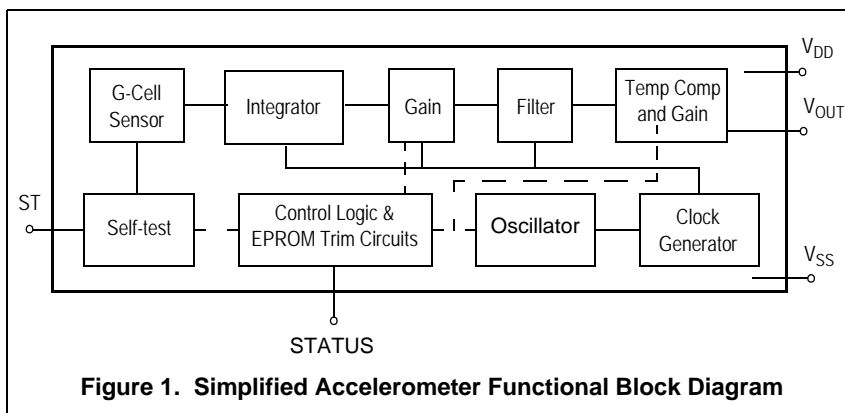


Table 1. Maximum Ratings

(Maximum ratings are the limits to which the device can be exposed without causing permanent damage.)

Rating	Symbol	Value	Unit
Powered Acceleration (all axes)	G_{pd}	1500	g
Unpowered Acceleration (all axes)	G_{upd}	2000	g
Supply Voltage	V_{DD}	-0.3 to +7.0	V
Drop Test ⁽¹⁾	D_{drop}	1.2	m
Storage Temperature Range	T_{stg}	-40 to +125	°C

1. Dropped onto concrete surface from any axis.

ELECTRO STATIC DISCHARGE (ESD)**WARNING: This device is sensitive to electrostatic discharge.**

Although the Freescale accelerometers contain internal 2 kV ESD protection circuitry, extra precaution must be taken by the user to protect the chip from ESD. A charge of over 2000 volts can accumulate on the human body or associated test equipment. A charge of this magnitude can alter the

performance or cause failure of the chip. When handling the accelerometer, proper ESD precautions should be followed to avoid exposing the device to discharges which may be detrimental to its performance.

Table 2. Operating Characteristics(Unless otherwise noted: $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$, $4.75 \leq V_{DD} \leq 5.25$, Acceleration = 0g, Loaded output.⁽¹⁾)

Characteristic	Symbol	Min	Typ	Max	Unit
Operating Range ⁽²⁾					
Supply Voltage ⁽³⁾	V_{DD}	4.75	5.00	5.25	V
Supply Current	I_{DD}	1.1	2.1	3.0	mA
Operating Temperature Range	T_A	-40	—	+105	$^{\circ}\text{C}$
Acceleration Range	g_{FS}	—	5	—	g
Output Signal					
+1g ($T_A = 25^{\circ}\text{C}$, $V_{DD} = 5.0\text{ V}$) ⁽⁴⁾	V_{OFF}	2.25	2.5	2.75	V
+1g ($V_{DD} = 5.0\text{ V}$)	V_{OFF}	2.2	2.5	2.8	V
Sensitivity ($T_A = 25^{\circ}\text{C}$, $V_{DD} = 5.0\text{ V}$) ⁽⁵⁾	S	380	400	420	mV/g
Sensitivity	S	74	80	86	mV/g/V
Bandwidth Response	f_{-3dB}	42.5	50	57.5	Hz
Nonlinearity	NL_{OUT}	-1.0	—	+1.0	% FSO
Noise					
RMS (0.1 Hz – 1.0 kHz)	n_{RMS}	—	2.0	4.0	mVrms
Spectral Density (RMS, 0.1 Hz – 1.0 kHz) ⁽⁶⁾	n_{SD}	—	700	—	$\mu\text{g}/\sqrt{\text{Hz}}$
Self-Test					
Output Response ($V_{DD} = 5.0\text{ V}$)	ΔV_{ST}	0.2	0.25	0.3	V/V
Input Low	V_{IL}	V_{SS}	—	$0.3 V_{DD}$	V
Input High	V_{IH}	$0.7 V_{DD}$	—	V_{DD}	V
Input Loading ⁽⁷⁾	I_{IN}	-300	-125	-50	μA
Response Time ⁽⁸⁾	t_{ST}	—	2.0	25	ms
Status ^{(9), (10)}					
Output Low ($I_{load} = 100\ \mu\text{A}$)	V_{OL}	—	—	0.4	V
Output High ($I_{load} = 100\ \mu\text{A}$)	V_{OH}	$V_{DD} - 0.8$	—	—	V
Output Stage Performance					
Electrical Saturation Recovery Time ⁽¹¹⁾	t_{DELAY}	—	—	2.0	ms
Full Scale Output Range ($I_{OUT} = 200\ \mu\text{A}$)	V_{FSO}	$V_{SS} + 0.25$	—	$V_{DD} - 0.25$	V
Capacitive Load Drive ⁽¹²⁾	C_L	—	—	100	pF
Output Impedance	Z_O	—	50	—	Ω
Mechanical Characteristics					
Transverse Sensitivity ⁽¹³⁾	$V_{XZ,YZ}$	—	—	5.0	% FSO

- For a loaded output the measurements are observed after an RC filter consisting of a 1 k Ω resistor and a 0.1 μF capacitor to ground.
- These limits define the range of operation for which the part will meet specification.
- Within the supply range of 4.75 and 5.25 volts, the device operates as a fully calibrated linear accelerometer. Beyond these supply limits the device may operate as a linear device but is not guaranteed to be in calibration.
- The device can measure both + and - acceleration. With +1g acceleration the output is at midsupply. For positive acceleration the output will increase above $V_{DD}/2$ and for negative acceleration the output will decrease below $V_{DD}/2$.
- The device is calibrated at 3g. Sensitivity limits apply to 0Hz acceleration.
- At clock frequency ≥ 70 kHz.
- The digital input pin has an internal pull-down current source to prevent inadvertent self test initiation due to external board level leakages.
- Time for the output to reach 90% of its final value after a self-test is initiated.
- The Status pin output is not valid following power-up until at least one rising edge has been applied to the self-test pin. The Status pin is high whenever the self-test input is high, as a means to check the connectivity of the self-test and Status pins in the application.
- The Status pin output latches high if a Low Voltage Detection or Clock Frequency failure occurs, or the EPROM parity changes to odd. The Status pin can be reset low if the self-test pin is pulsed with a high input for at least 100 μs , unless a fault condition continues to exist.
- Time for amplifiers to recover after an acceleration signal causes them to saturate.
- Preserves phase margin (60 $^{\circ}$) to guarantee output amplifier stability.
- A measure of the device's ability to reject an acceleration applied 90 $^{\circ}$ from the true axis of sensitivity.

PRINCIPLE OF OPERATION

The Freescale accelerometer is a surface-micromachined integrated-circuit accelerometer.

The device consists of a surface micromachined capacitive sensing cell (g-cell) and a CMOS signal conditioning ASIC contained in a single integrated circuit package. The sensing element is sealed hermetically at the wafer level using a bulk micromachined "cap" wafer.

The g-cell is a mechanical structure formed from semiconductor materials (polysilicon) using semiconductor processes (masking and etching). It can be modeled as two stationary plates with a moveable plate in-between. The center plate can be deflected from its rest position by subjecting the system to an acceleration (Figure 3).

When the center plate deflects, the distance from it to one fixed plate will increase by the same amount that the distance to the other plate decreases. The change in distance is a measure of acceleration.

The g-cell plates form two back-to-back capacitors (Figure 4). As the center plate moves with acceleration, the distance between the plates changes and each capacitor's value will change, ($C = A\epsilon/D$). Where A is the area of the plate, ϵ is the dielectric constant, and D is the distance between the plates.

The CMOS ASIC uses switched capacitor techniques to measure the g-cell capacitors and extract the acceleration data from the difference between the two capacitors. The ASIC also signal conditions and filters (switched capacitor) the signal, providing a high level output voltage that is ratiometric and proportional to acceleration.

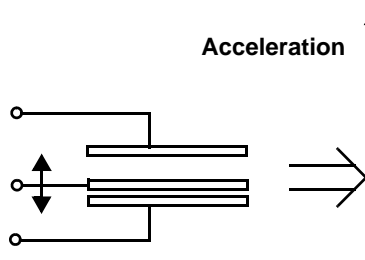


Figure 3. Transducer Physical Model

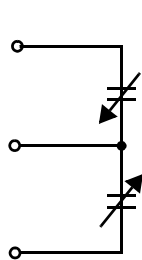


Figure 4. Equivalent Circuit Model

SPECIAL FEATURES

Filtering

The Freescale accelerometers contain an onboard 2-pole switched capacitor filter. A Bessel implementation is used because it provides a maximally flat delay response (linear phase) thus preserving pulse shape integrity. Because the filter is realized using switched capacitor techniques, there is no requirement for external passive components (resistors and capacitors) to set the cut-off frequency.

Self-Test

The sensor provides a self-test feature that allows the verification of the mechanical and electrical integrity of the accelerometer at any time before or after installation. This feature is critical in applications such as automotive airbag systems where system integrity must be ensured over the life of the vehicle. A fourth "plate" is used in the g-cell as a self-test plate. When the user applies a logic high input to the self-test pin, a calibrated potential is applied across the self-test plate and the moveable plate. The resulting electrostatic force ($F_e = \frac{1}{2} AV^2/d^2$) causes the center plate to deflect. The resultant deflection is measured by the accelerometer's control ASIC and a proportional output voltage results. This procedure assures that both the mechanical (g-cell) and electronic sections of the accelerometer are functioning.

Status

Freescale accelerometers include fault detection circuitry and a fault latch. The Status pin is an output from the fault latch, OR'd with self-test, and is set high whenever the following event occurs:

- Parity of the EPROM bits becomes odd in number.

The fault latch can be reset by a rising edge on the self-test input pin, unless one (or more) of the fault conditions continues to exist.

BASIC CONNECTIONS

Pinout Description

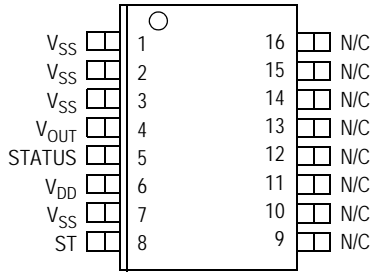


Table 3. Pin Descriptions

Pin No.	Pin Name	Description
1 thru 3	V _{SS}	Redundant connections to the internal V _{SS} and may be left unconnected.
4	V _{OUT}	Output voltage of the accelerometer.
5	STATUS	Logic output pin to indicate fault.
6	V _{DD}	The power supply input.
7	V _{SS}	The power supply ground.
8	ST	Logic input pin used to initiate self-test.
9 thru 13	Trim pins	Used for factory trim. Leave unconnected.
14 thru 16	—	No internal connection. Leave unconnected.

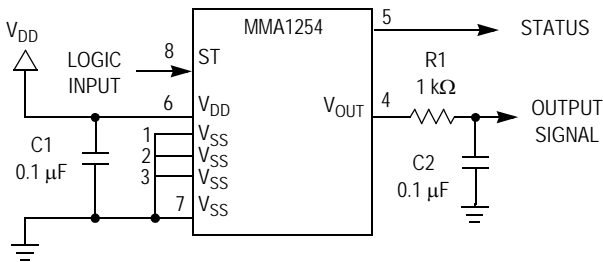


Figure 5. SOIC Accelerometer with Recommended Connection Diagram

PCB Layout

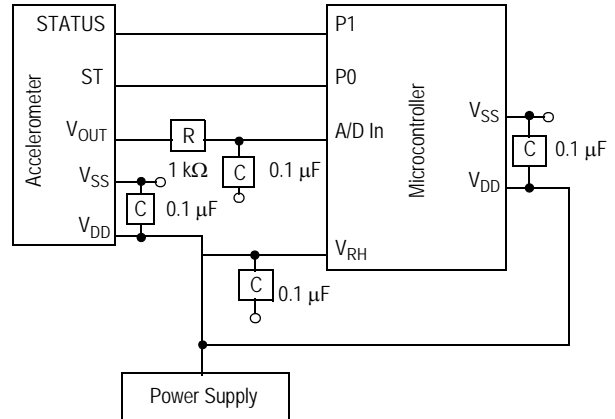


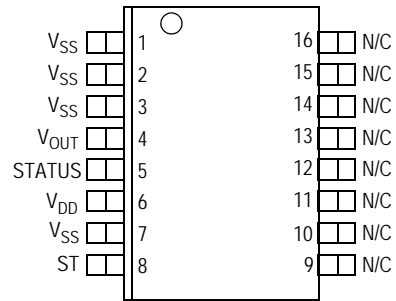
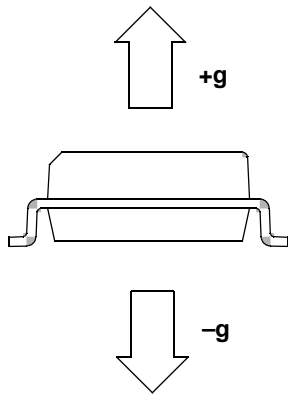
Figure 6. Recommended PCB Layout for Interfacing Accelerometer to Microcontroller

NOTES:

1. Use a 0.1 μF capacitor on V_{DD} to decouple the power source.
2. Physical coupling distance of the accelerometer to the microcontroller should be minimal.
3. Place a ground plane beneath the accelerometer to reduce noise, the ground plane should be attached to all of the open ended terminals shown in Figure 6.
4. Use an RC filter of 1 kΩ and 0.1 μF on the output of the accelerometer to minimize clock noise (from the switched capacitor filter circuit).
5. PCB layout of power and ground should not couple power supply noise.
6. Accelerometer and microcontroller should not be a high current path.
7. A/D sampling rate and any external power supply switching frequency should be selected such that they do not interfere with the internal accelerometer sampling frequency. This will prevent aliasing errors.

ACCELERATION SENSING DIRECTIONS

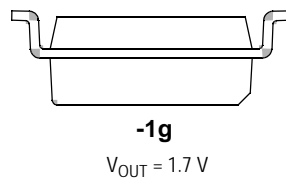
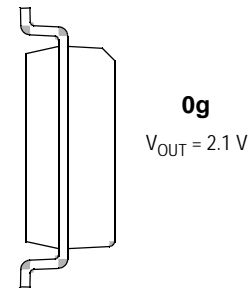
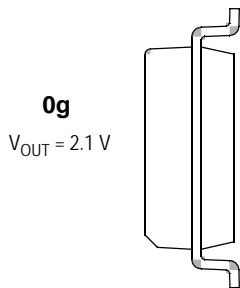
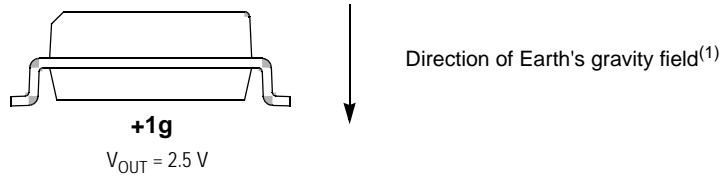
DYNAMIC ACCELERATION



16-Pin SOIC Package

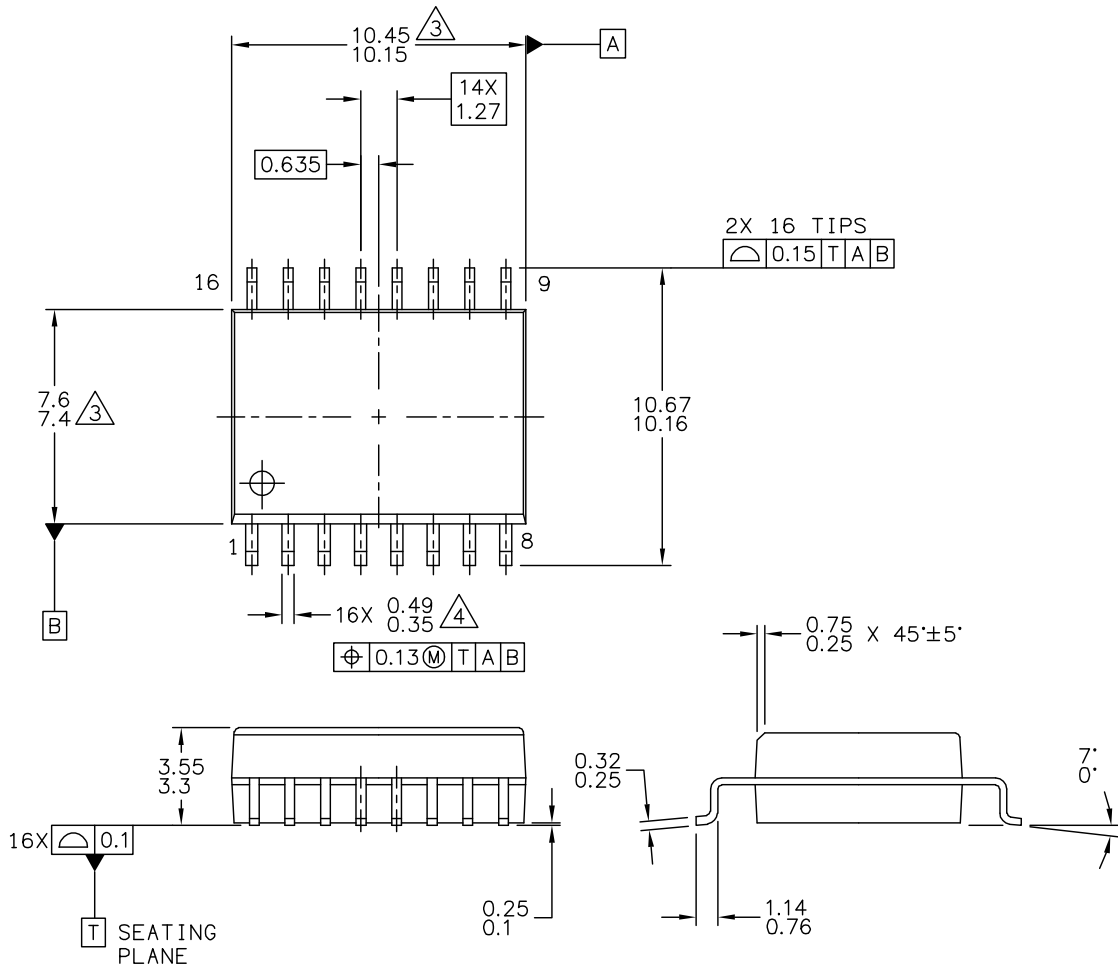
N/C pins are recommended to be left FLOATING

STATIC ACCELERATION



1. When positioned as shown, the Earth's gravity will result in a positive 1g output

PACKAGE DIMENSIONS



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	TITLE: 16 LEAD SOIC ACCELEROMETER		DOCUMENT NO: 98ASB16926C REV: C
		CASE NUMBER: 475-01	17 MAR 2005
		STANDARD: NON-JEDEC	

**CASE 475-01
ISSUE C
16 LEAD SOIC**

PACKAGE DIMENSIONS

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 PER SIDE.

4. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. PROTRUSIONS SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.75

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TITLE: 16 LEAD SOIC ACCELEROMETER	DOCUMENT NO: 98ASB16926C	REV: C	
	CASE NUMBER: 475-01	17 MAR 2005	
	STANDARD: NON-JEDEC		

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**CASE 475-01
ISSUE C
16 LEAD SOIC**

MMA1254

Revision History

Revision number	Revision date	Description of changes
0	01/2012	<ul style="list-style-type: none">Initial Release
1	06/2012	<ul style="list-style-type: none">Removed KEG suffix from Device Number, in Table 2. Operating Characteristics changed Output Signal +1g VOF: VDD = 0.40, 0.50 and 0.60 to +1g (VDD =5.0 V)(4) VOFF VDD = 2.2, 2.5 and 2.8.

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