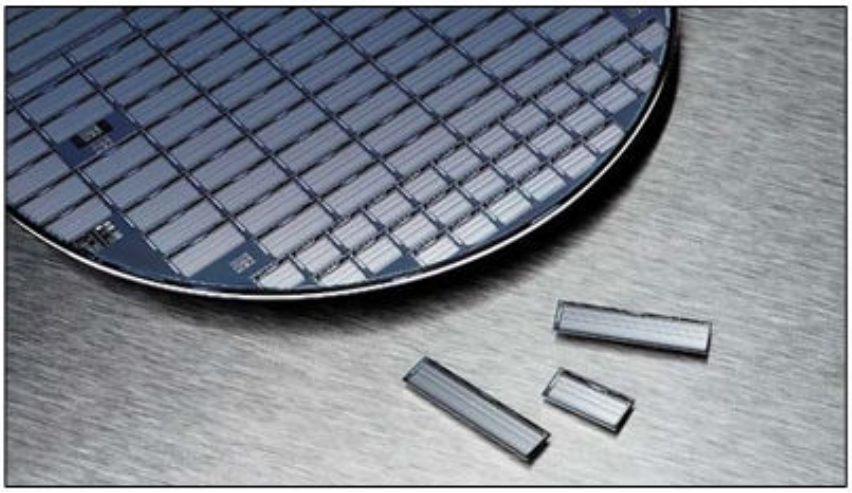
DATASHEET

XL-1 Series

64, 128, and 256 Channel Variable-Gain CMOS Buffered Multiplexers



Overview

The XL-1 series buffered multiplexers offer a versatile solution to the increasing demand for low noise amplification and multiplexing. They are designed to interface with linear photosensitive arrays, such as those made of indium gallium arsenide, germanium, amorphous silicon, or any of several special-purpose infrared-sensitive materials. Each channel of the multiplexer channel consists of a charge amplifier in series with two separate buffered sample-and-hold paths for correlated double sampling (CDS). A broad range of electrically-selectable integrating capacitors provide accommodation for charge packets from a wide range of sensor materials, pixel sizes, and exposure levels.

Features

- 64, 128, or 256 active channels
- 100 µm channel pitch
- Selectable integrating capacitor
- Dynamic range greater than 90 dB
- Charge conversion 10 to 160 nV/e-
- Video output frequency 1.0 MHz
- Low input noise leakage current
- Single clock output operation
- Built-in correlated double sampling
- Bi-directional readout capability

Caution: While the XL-1 Multiplexers have been designed to resist electrostatic discharge (ESD), they can be damaged from such discharges. Always observe proper ESD precautions when handling and storing these devices.

Buffered Multiplexers

Functional Description

Each XL-1 series multiplexer consists of the 64, 128, or 256 channels. In addition, the 256-channel model includes a dummy channel placed on either end of the array to prevent edge non-uniformity effects common in long multiplexers. An on-chip decoder supports readout of the device at any speed up to 1MHz. Data into the decoder and at output pads is buffered for direct readings with low signal degradation. The dual sample-and-hold video outputs support correlated double sampling (CDS). An on-chip counter operates the readout with one master clock signal. *Figure 1* shows a block diagram for the 256-channel type. *Figure 2* displays a schematic for an individual channel.

Each channel of the multiplexer consists of a charge amplifier in series with two separate buffered paths for CDS. The charge amplifier converts incoming electrons into a voltage that can be stored in either the Reset or Sample path. External clocks, $Ø_{SHR}$ and $Ø_{SHS}$ respectively, control access to the reset and sample paths of the CDS. Since these paths are identical, the timing is accurately matched. Inside each path of the CDS is an amplifier set up in a unity gain buffer configuration. This will record the voltage value seen at the output of the charge amplifier an store it until the corresponding decoder path reads it out. The decoders are controlled simultaneously by a start pulse ($Ø_{ST}$) and a master clock signal ($Ø_{CLK}$) supplied externally to the multiplexer. Once the decoder is activated, the stored values are read sequentially in one direction until all channels have been accessed.

Figure 1. Block Diagram for the 256-Channel Model

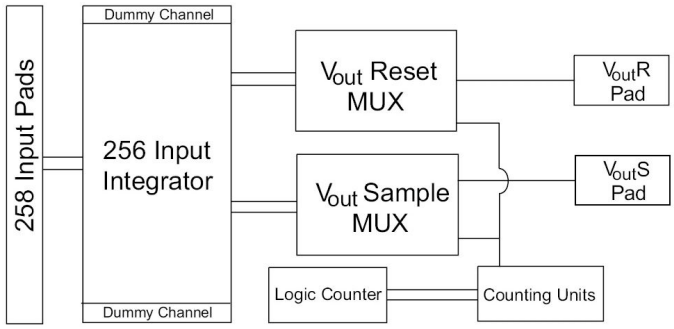


Figure 2. Schematic of an Individual Channel

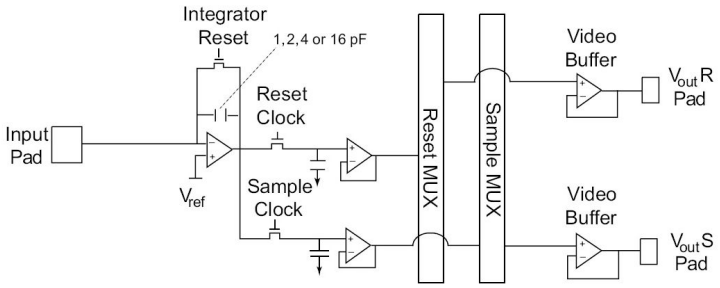


Table 1a. Integration Capacitance Selection and Value

Control 0	Control 1	C_i(pF)	Conversion (nV/e -)
0	0	1	160
1	0	2	80
0	1	4	40
1	1	16	10

Upon completion of the readout, the device will generate a digital end-of-scan signal, EOS. This signal can be used as the start pulse for a second multiplexer to facilitate sequential readout of several multiplexer devices placed end-to-end on a long imager.

Charge Amplifier

The charge amplifier in each channel converts incoming electrons into a corresponding voltage value based on the sensitivity of the amplifier and its corresponding capacitance value. For this device, the sensitivity is determined by the integration capacitance value (C_i) selected (1, 2, 4, or 16 pf), as shown in *Table 1A*.

The general equation that governs this effect is:

[charge x sensitivity = voltage]

Therefore, the output will be:

V_{out} = [V_{ref} - (# of electrons x sensitivity per electron)]

This equation is only valid if V_{ref} (corresponding reference value) allows the amplifier to operate within its linear region. A generalized schematic for this amplifier configuration is shown in *Figure 3a*. *Figure 3b* and *Figure 3c* show the V_{out} versus integration time at different gains as the charge amplifier receives incoming holes and electrons, respectively.

The sensitivity of the charge amplifier may be selected from one of four values through two binary control inputs. Integrating capacitors of the 1, 2, 4, and 16 pf provide sensitivities of 0.16, 0.08, 0.04, and 0.01 µV/e- respectively.

Figure 3a. Charge Amplifier

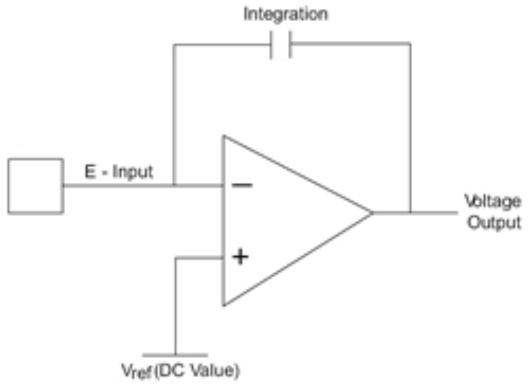


Figure 3b. Holes

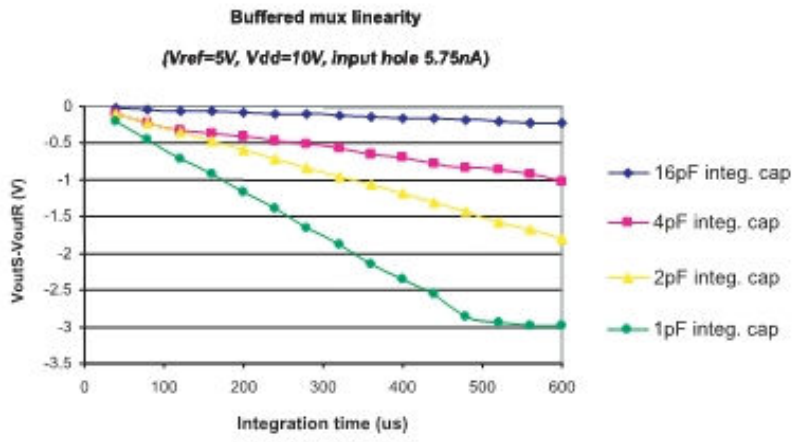
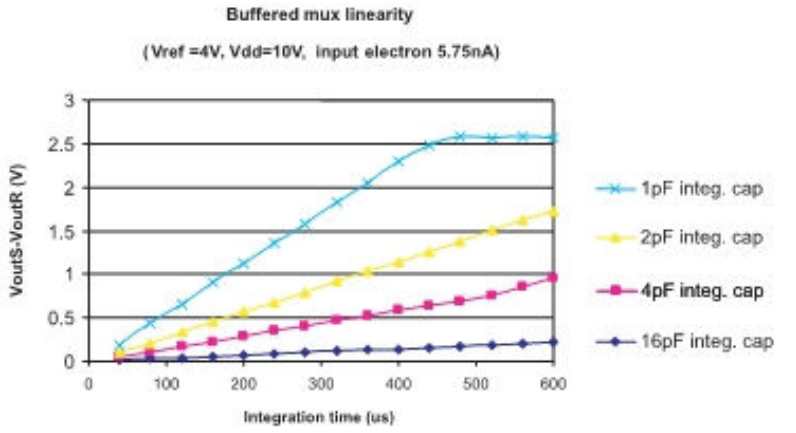


Figure 3c. Electrons



Sample and Hold

After the charge has been integrated into a voltage value, the output can then be stored in one of the two sample-and-hold paths for each channel. There are two sample-and-hold paths present to perform off-chip CDS operations on the output signal and to improve the dynamic range of the device.

Dual Decoders

To place all of these separate voltage values on two different output pads, two decoders are positioned after all of the sample-and-hold paths. The decoder control is done on the chip. The decoder is controlled by two clocks, $Ø_{ST}$ and $Ø_{CLK}$. Triggering $Ø_{ST}$ from low to high will signal the control logic to begin monitoring the $Ø_{CLK}$. Signal. At each rising edge of the $Ø_{CLK}$ signal, the control logic will pass the sample-and-hold voltage value to the corresponding output pad.

Video Buffer

A video buffer follows the decoder and reads out all channels sequentially at a high speed. For this purpose, the video buffer has a high slew rate and low output impedance.

Timing

There are eight different control clocks that must be synchronized with one another to operate the XL-1 series multiplexers. At power-up and in-between data samples, the multiplexer timing must be reset. To accomplish this, the first signal, $Ø_{RST}$, is brought from high to low for at least one clock cycle. This transition resets the counter inside the device so the decoders will always begin clocking at the beginning of the multiplexer.

Data Sampling

Three signals, $Ø_{SHR}$, $Ø_{SHS}$, and $Ø_{IRST}$ work together to take valid data samples. $Ø_{IRST}$ controls the integration mode. When $Ø_{IRST}$ is high, the amplifier will begin to integrate charge. $Ø_{SHR}$ activates one of the two sample-and-hold paths to pass the output voltage on the charge amplifier. Similarly, $Ø_{SHS}$ activates the second path. *Figure 4* and *Table 1b* show the above clocks on a common time base.

If t1 is too small, there will be insufficient time for integration. If t1 is too large, the integrator will integrate part of the offset as well. Intervals t2 and t5 correspond to the difference in time between $Ø_{IRST}$ high and $Ø_{SHR}$ or $Ø_{SHS}$ low, respectively. Intervals t3 and t4 correspond to the time required for sample-and-hold to settle onto a voltage. For a one-bit output value, one clock cycle is adequate. However, for high-resolution DACs, sufficient time must be allowed for required settling accuracy.

Figure 4. Reset and Sample-and-Hold Timing

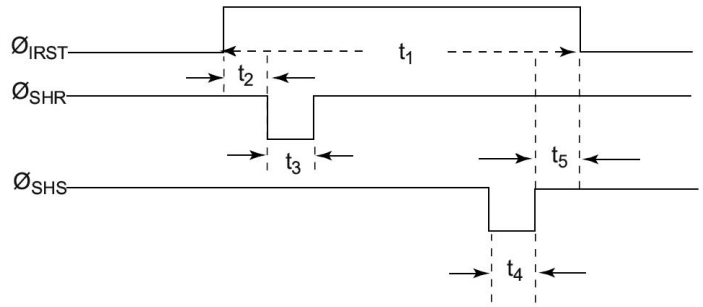


Table 1b. Data Sample Timing Limits

Time	Description	Minimums
t1	Total integration time	-
t2	Reset clock offset	1/2 Clock cycle
t3	Reset clock time	1 Clock
t4	Sample clock time	1 Clock
t5	Sample clock offset	1/2 Clock cycle

Output Data Readout

Figure 5 shows the clock timing for the data readout. A rising edge of the master clock ($Ø_{CLK}$) samples the $Ø_{ST}$ signal and begins the readout process. At each rising edge the decoder will send the next sequential channel to the output. $Ø_{CLK}$ increments the counter inside the control logic and allows it to send the next channel value to the output video buffer.

Complete Cycle

Figure 6 displays one complete process.

Readout Direction Control

$Ø_{DIR}$ controls the direction of the device readout. If $Ø_{DIR}$ is clocked high, then the multiplexer will clock out data from channel 0 to channel N+1 sequentially, and the start pulse should be sent into the pad marked $Ø_{ST}$/EOS. Conversely, if $Ø_{DIR}$ is low, it clocks from channel N+1 to channel 0, and the start pulse must be sent to EOS/$Ø_{ST}$. $Ø_{DIR}$ must not be used as a dynamic switch to reverse directions in the middle of a readout cycle.

Electrical Description

The XL-1 series multiplexers operate with standard power supplies for V_{DD} = 10 VDC, V_{SS} = 0 V, and V_{CC} = 10 VDC. To minimize the noise, the analog and digital grounds are separated. The equivalent input noise is 8 mV rms. It can be calculated by using the following equation:

Input referred Noise =

$$2\,(4/3 \times KT \times C_f/C_iC_L)^{+1/2}$$

System Noise = $2(8/3 \times KT/q_{e2}) + 1/2$

Where KT is constant at room temperature, and C_f/C_iC_L are feedback, input and load capacitance, q_e is an electron charge.

The bias pin is used to bias all analog components in the multiplexer. A 400 K ohm resistor is connected between the R_{BIAS} pad and V_{SS} for reduction of noise current. *Figure 7* shows the electrical connections of the device.

Figure 5. Data Readout Timing

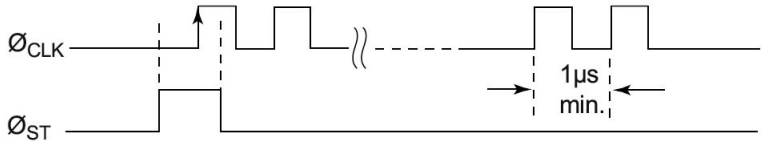


Figure 6. One Full Cycle

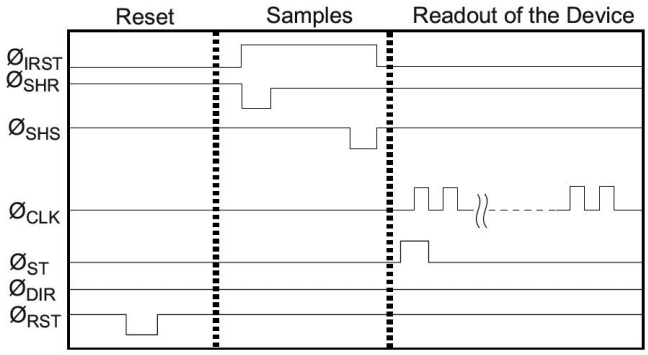
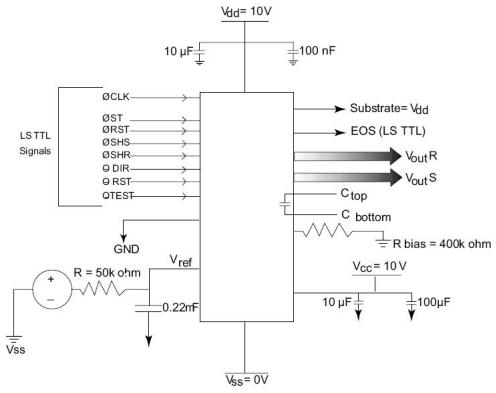


Figure 7. Electrical Connections



Physical Description

XL-1 series multiplexers are provided as sawed, tested die, and are packaged for protection from electrostatic discharge and handling damage. These die should be mounted on ceramic substrates and ball-bonded to the detector and the readout pins. Drawings showing the locations and sizes of bond pads are available in .dxf and .dwg formats from Excelitas.

Recommended bonding procedures are also available from Excelitas. Although these procedures are recommended, due to the high risk of damage attributed to improper handling, the devices are sold without warranty, regardless of bonding procedures.

The bond pad material is aluminum with 1% silicon flush with the top surface of the die suitable for aluminum or gold compression bonding. All die is 0.675 ± 0.020 mm thick.

Table 2. Specifications

Description	Min	Nom	Max	Units
Saturation charge	2.5[5]		40.5[6]	pC
Parasitic input capacitance (to V_{SS})		4.5		pF
Input leakage current (per channel)		±100	±250	fA
Charge conversion	10[6]		160[5]	nV/e-
Integration amplifier slew rate		1.0		V/µsec
Output clocked video level (V_{REF}= 5V)				
Q: 0 to QSAT	3.0	2.5	1.5	V
Q: 0 to -QSAT	6.5	7.5	8.5	V
Output quiescent video level		V_{REF}		V
Output video impedance		1.5		K ohm
Output video readout frequency			1.0	MHz
VoutS output variation[1]		15		mV
VoutR output variation[1]		15		mV
Video output differential offset[2]		40		mV
Digital outputs (EOL signal) high level	3.5		5.5	V
Digital outputs (EOL signal) low level	GND		GND+0.3	V
Quiescent V_{DD} current (I_{DD})		40	45	mA
Clocked V_{DD} current		50	55	mA
PSRR (@1kHz & 120 pF C_{IN}) To V_{SS}			-25	dB
PSRR (@1kHz & 120 pF C_{IN}) To V_{DD}			-25	dB
Operating potential (V_{DD} - V_{SS})	9.5	10	12.5	V
Reference potential		5	7	V
Digital input levels -high level	3.5	5	5	V
Digital Input levels - low level	GND	GND	0.4	V
Bias resistor current		16		µA
Operating temperature range	0		70	°C
Noise @25 pFC_{IN}[3]				
Input referred noise		5		µVms
		29		rms electrons
System noise		70		µVms
		450		rms electrons
Dynamic range[4]	90			dB

Notes:

[1] Output Variation is (max signal-min signal) at zero input charge.

[2] Peak-to-peak signal mismatch ($Vout_s$ - $Vout_r$)at zero input charge.

[3] Noise with 1pF integrating capacitor.

[4] Dynamic range defined as the Max Output/Noise Floor.

[5] Integrating capacitor is 1 pF.

[6] Integrating capacitor is 16 pF.

Figure 8. 64-Channel

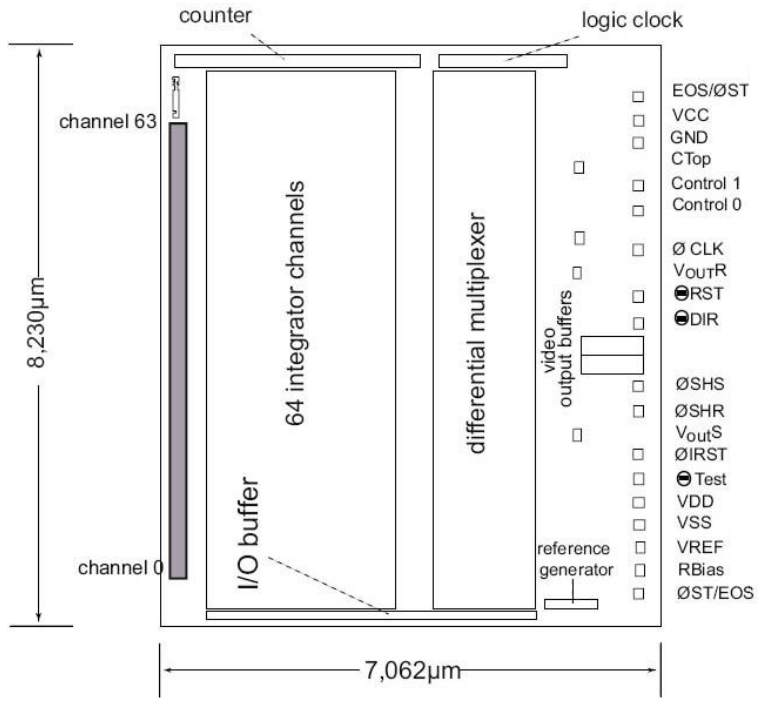


Figure 10. 256-Channel

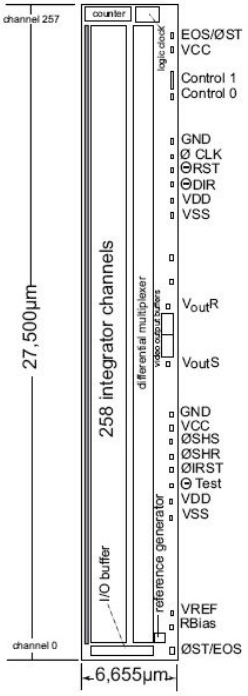


Figure 9. 128-Channel (same as old sheet)

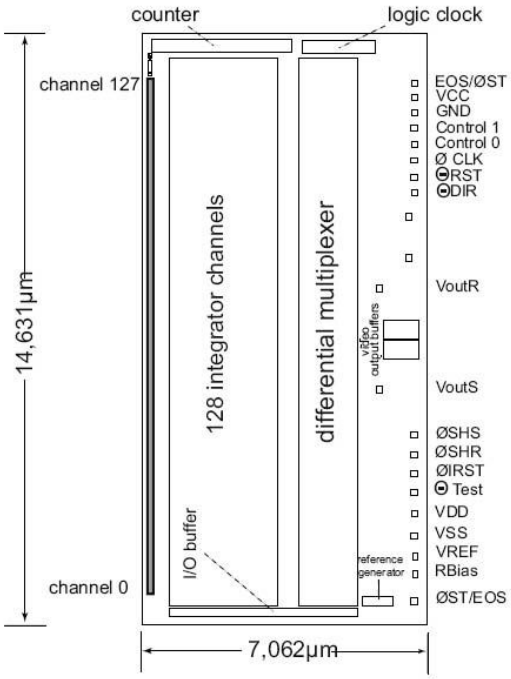


Table 3. Bond Pad Description

Name	Function	Nom. Voltages
$Ø_{TEST}$	Reserved	0V
$Ø_{RST}$	Integrator reset control	0 - 5 V
$Ø_{SHR}$	S&H reset control	0 - 5 V
$Ø_{SHS}$	S&H sample control	0 - 5 V
V_{CC}	Digital positive supply	10 V
GND	Digital ground	0 V
$V_{OUT}S$	Output video sample level	-
$V_{OUT}R$	Output video reset level	-
V_{SS}	Analog ground	0 V
V_{DD}	Analog positive supply, substrate	10 V
$Ø_{DIR}$	Bidirectionality control	0 - 5 V
$Ø_{RST}$	Counter reset control	0 - 5 V
$Ø_{CLK}$	Master clock signal	0 - 5 V
Control 0	Control 0 for the selectable gain	0 - 5 V
Control 1	Control 1 for the selectable gain	0 - 5 V
EOS/$Ø_{ST}$	EOS signal/start pulse	0 - 5 V
INPUTn	Input to mux channel n	-
$Ø_{ST}$/EOS	Start pulse/EOS signal	0 - 5 V
R_{bias}	Bias resistor to V_{SS}	Note 1
V_{REF}	Electrons (Q: 0 to -Qsat)	4 V
	Holes (Q: 0 to Qsat)	5 V

Note 1: Connect through 400 K ohm to GND.

Table 4. Product Numbers

Channels	64	128	256
Sawed and Tested Die	XL1064CAD-711	XL1128CAD-711	XL1256CAD-711

No Warranty

Due to the high risk of damage attributed to improper handling, all XL-1 devices are sold without warranty. Potential users should discuss proper handling procedures with Excelitas before using these devices.

For more information, email us at generalinquiries@excelitas.com or visit our website at www.excelitas.com.

Worldwide Headquarters
Excelitas Technologies
44370 Christy Street
Fremont, CA 94538 USA
Telephone: (+1) 510-979-6500
Toll Free (N. America): (800) 775-OPTO (6786)
Fax: (+1) 510-687-1140
generalinquiries@excelitas.com

European Headquarters
Excelitas Technologies
Wenzel-Jaksch-Str. 31
D-65199 Wiesbaden, Germany
Telephone: (+49) 611-492-430
Fax: (+49) 611-492-165

Asia Headquarters
Excelitas Technologies
47 Ayer Rajah Crescent #06-12
Singapore 139947
Telephone: (+65) 6775-2022
Fax: (+65) 6775-1008

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600035_01 DTS0805P Printed in U.S.A.