



## MICRF213

### 3.3V, QwikRadio® 315MHz Receiver

#### General Description

The MICRF213 is a general purpose, 3.3V QwikRadio Receiver that operates at 315MHz with typical sensitivity of -110dBm.

The MICRF213 functions as a super-heterodyne receiver for OOK and ASK modulation up to 7.2kbps. The down-conversion mixer also provides image rejection. All post-detection data filtering is provided on the MICRF213. Any one of four filter bandwidths may be selected externally by the user using binary steps (from 1.18kHz to 9.44kHz, Manchester Encoded). The user need only configure the device with a set of easily determined values, based upon data rate, code modulation format, and desired duty-cycle operation.

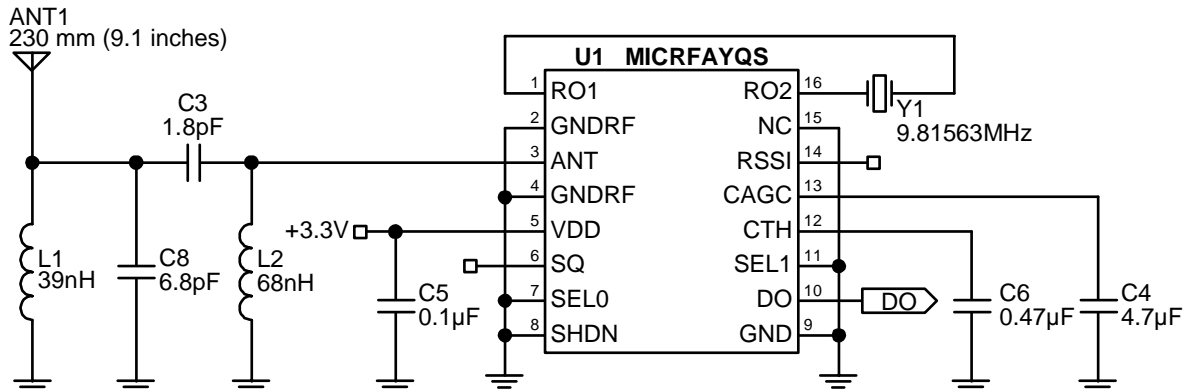
#### Features

- Up to -110dBm sensitivity, 1kbps and BER 10E-02
- Image Rejection Mixer
- Frequency from 300MHz to 350MHz
- Low current consumption: 3.9mA @ 315MHz, continuous on data rates to 7.2kbps (Manchester Encoded)
- Analog RSSI Output
- No IF filter required
- Excellent selectivity and noise rejection
- Low external part count

#### Ordering Information

| Part Number  | Temperature Range | Package     |
|--------------|-------------------|-------------|
| MICRF213AYQS | -40° to +105°C    | 16-Pin QSOP |

#### Typical Application



315MHz, 1kHz Baud Rate Example

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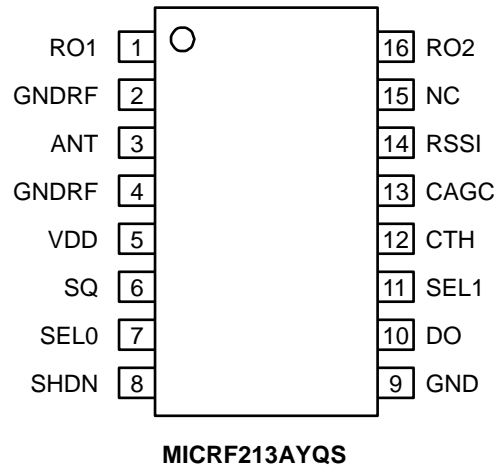
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## Pin Configuration



## Pin Description

| 16-Pin QSOP | Pin Name | Pin Function   |
|-------------|----------|--|
| 1           | RO1      | Reference resonator input connection to Colpitts oscillator stage. May also be driven by external reference signal of 1.5V p-p amplitude maximum.  |
| 2           | GNDRF    | Negative supply connection associated with ANT RF input.   |
| 3           | ANT      | RF signal input from antenna. Internally AC-coupled. It is recommended that a matching network with an inductor-to-RF ground is used to improve ESD protection.  |
| 4           | GNDRF    | Negative supply connection associated with ANT RF input.   |
| 5           | VDD      | Positive supply connection for all chip functions.   |
| 6           | SQ       | Squelch control logic input with an active internal pull-up when not shut down.  |
| 7           | SEL0     | Logic control input with active internal pull-up. Used in conjunction with SEL1 to control the demodulator low pass filter bandwidth. (See filter table for SEL0 and SEL1 in application section)  |
| 8           | SHDN     | Shutdown logic control input. Active internal pull-up.   |
| 9           | GND      | Negative supply connection for all chip functions except RF input.   |
| 10          | DO       | Demodulated data output.   |
| 11          | SEL1     | Logic control input with active internal pull-up. Used in conjunction with SEL0 to control the demodulator low pass filter bandwidth. (See filter table for SEL0 and SEL1 in application subsection)   |
| 12          | CTH      | Demodulation threshold voltage integration capacitor connection. Tie an external capacitor across CTH pin and GND to set the settling time for the demodulation data slicing level. Values above 1nF are recommended and should be optimized for data rate and data profile. |
| 13          | CAGC     | AGC filter capacitor connection. CAGC capacitor, normally greater than 0.47uF, is connected from this pin to GND   |
| 14          | RSSI     | Received signal strength indication output. Output is from a buffer with 200 ohms typical output impedance.  |
| 15          | NC       | Not Connected (Connect to Ground)  |
| 16          | RO2      | Reference resonator input connection to Colpitts oscillator stage, 7pF, in parallel with low resistance MOS switch-to-GND, during normal operation. Driven by startup excitation circuit during the internal startup control sequence.                                       |

### Absolute Maximum Ratings<sup>(1)</sup>

|                                      |                 |
|--------------------------------------|-----------------|
| Supply Voltage ( $V_{DD}$ )          | +5V             |
| Input Voltage                        | +5V             |
| Junction Temperature                 | +150°C          |
| Lead Temperature (soldering, 10sec.) | 260°C           |
| Storage Temperature ( $T_S$ )        | -65°C to +150°C |
| Maximum Receiver Input Power         | +10dBm          |
| EDS Rating <sup>(3)</sup>            | 3KV HBM         |

### Operating Ratings<sup>(2)</sup>

|                               |                 |
|-------------------------------|-----------------|
| Supply voltage ( $V_{DD}$ )   | +3.0V to +3.6V  |
| Ambient Temperature ( $T_A$ ) | -40°C to +105°C |
| Input Voltage ( $V_{IN}$ )    | 3.6V (Max)      |
| Maximum Input RF Power        | -20dBm          |

### Electrical Characteristics<sup>(4)</sup>

Specifications apply for  $3.0V < V_{DD} < 3.6V$ ,  $V_{SS} = 0V$ ,  $C_{AGC} = 4.7\mu F$ ,  $C_{TH} = 0.47\mu F$ ,  $f_{RX} = 315\text{ MHz}$  unless otherwise noted.  
**Bold** values indicate -40°C -  $T_A$  - 105°C. 900bps data rate (Manchester encoded), reference oscillator frequency = 9.81563 MHz.

| Symbol                      | Parameter                            | Condition   | Min | Typ                  | Max | Units      |
|-----------------------------|--------------------------------------|---|-----|----------------------|-----|------------|
| $I_{DD}$                    | Operating Supply Current             | Continuous Operation, $f_{RX} = 315\text{MHz}$                          |     | 3.9                  |     | mA         |
| $I_{SHUT}$                  | Shut down Current                    |   |     | 0.33                 |     | $\mu A$    |
| <b>RF/IF Section</b>        |                                      |   |     |                      |     |            |
|                             | Image Rejection                      |   |     | 20                   |     | dB         |
|                             | 1 <sup>st</sup> IF Center Frequency  | $f_{RX} = 315\text{MHz}$  |     | 0.86                 |     | MHz        |
|                             | Receiver Sensitivity @ 1kbps         | $f_{RX} = 315\text{MHz}$ (matched to 50 $\Omega$ ) BER=10 <sup>-2</sup> |     | -110                 |     | dBm        |
|                             | IF Bandwidth                         | $f_{RX} = 315\text{MHz}$  |     | 235                  |     | kHz        |
|                             | Antenna Input Impedance              | $f_{RX} = 315\text{MHz}$  |     | 32.5 - j235          |     | $\Omega$   |
|                             | Receive Modulation Duty Cycle        | <b>Note 5</b>   | 20  |                      | 80  | %          |
|                             | AGC Attack / Decay Ratio             | $t_{ATTACK} / t_{DECAY}$  |     | 0.1                  |     |            |
|                             | AGC pin leakage current              | $T_A = 25^\circ C$<br>$T_A = +105^\circ C$                              |     | $\pm 2$<br>$\pm 800$ |     | nA<br>nA   |
|                             | AGC Dynamic Range                    | RF <sub>IN</sub> @ -50dBm   |     | 1.13                 |     | V          |
|                             |                                      | RF <sub>IN</sub> @ -110dBm  |     | 1.70                 |     | V          |
| <b>Reference Oscillator</b> |                                      |   |     |                      |     |            |
|                             | Reference Oscillator Frequency       | $f_{RX} = 315\text{MHz}$<br>Crystal Load Cap = 10pF                     |     | 9.81563              |     | MHz        |
|                             | Reference Oscillator Input Impedance |   |     | 300                  |     | k $\Omega$ |
|                             | Reference Oscillator Input Range     |   | 0.2 |                      | 1.5 | Vp-p       |
|                             | Reference Oscillator Source Current  | V(REFOSC) = 0V  |     | 3.5                  |     | $\mu A$    |

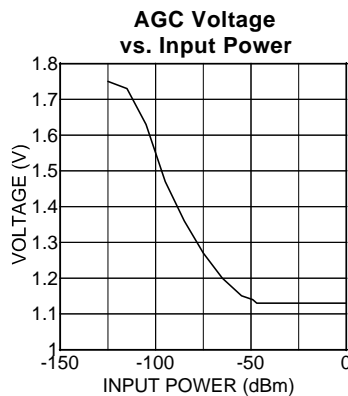
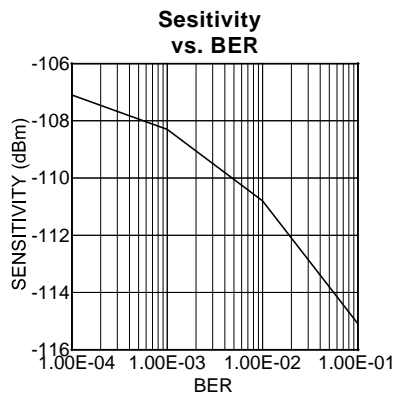
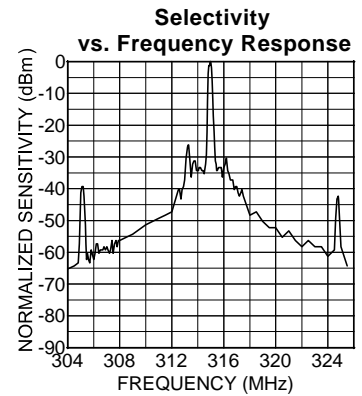
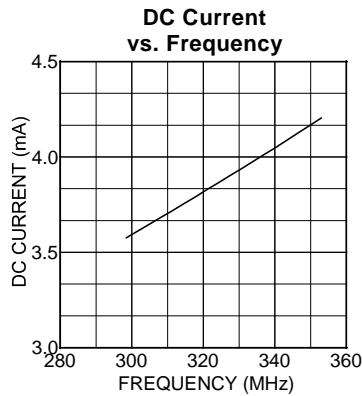
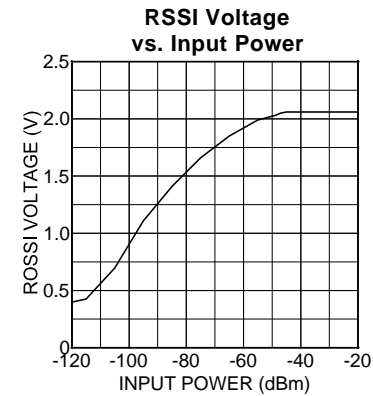
| Symbol                             | Parameter   | Condition  | Min | Typ                  | Max | Units           |
|------------------------------------|---|--|-----|----------------------|-----|-----------------|
| <b>Demodulator</b>                 |   |  |     |                      |     |                 |
|                                    | CTH Source Impedance  | $F_{REFOSC} = 9.81563\text{MHz}$                       |     | 165                  |     | k $\Omega$      |
|                                    | CTH Leakage Current   | $T_A = 25^\circ\text{C}$<br>$T_A = +105^\circ\text{C}$ |     | $\pm 2$<br>$\pm 800$ |     | nA<br>nA        |
|                                    | Demodulator Filter Bandwidth @ 315MHz (Programmable, see application section) | SEL0=0, SEL1=0   |     | 1180                 |     | Hz              |
|                                    |   | SEL0=1, SEL1=0   |     | 2360                 |     |                 |
|                                    |   | SEL0=0, SEL1=1   |     | 4720                 |     |                 |
|                                    |   | SEL0=1, SEL1=1   |     | 9400                 |     |                 |
| <b>Digital / Control Functions</b> |   |  |     |                      |     |                 |
|                                    | DO pin output current   | As output source @ 0.8Vdd<br>sink @ 0.2Vdd             |     | 260<br>600           |     | $\mu\text{A}$   |
|                                    | Output rise and fall times  | CI = 15pF, pin DO, 10-90%                              |     | 2                    |     | $\mu\text{sec}$ |
| <b>RSSI</b>                        |   |  |     |                      |     |                 |
|                                    | RSSI DC Output Voltage Range  | -110dBm to -50dBm                                      |     | 0.4 – 1.9            |     | V               |
|                                    | RSSI response slope   | -110dBm to -50dBm                                      |     | 25                   |     | mV/dB           |
|                                    | RSSI Output Current   |  |     | 400                  |     | $\mu\text{A}$   |
|                                    | RSSI Output Impedance   | $\pm 15$   |     | 200                  |     | $\Omega$        |
|                                    | RSSI Response Time  | 50% data duty cycle, input power to Antenna = -20 dBm  |     | 0.3                  |     | Sec             |

**Notes:**

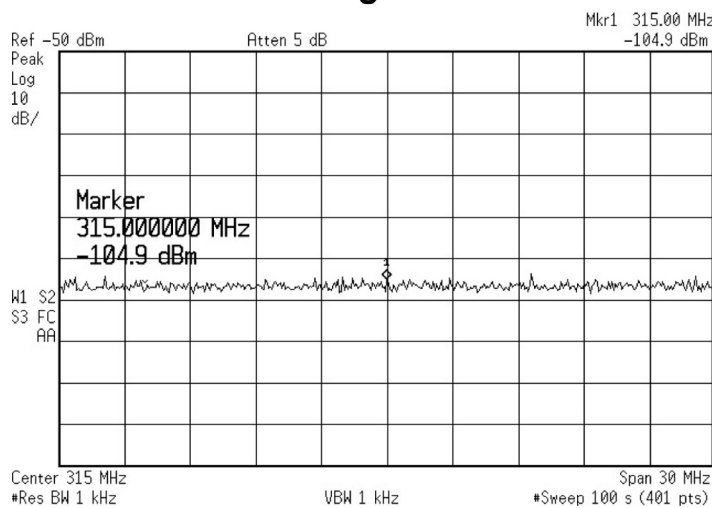
1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside of its operating rating.
3. Device is ESD sensitive. Use appropriate ESD precautions. Exceeding the absolute maximum rating may damage the device.
4. Sensitivity is defined as the average signal level measured at the input necessary to achieve  $10^{-2}$  BER (bit error rate). The input signal is defined as a return-to-zero (RZ) waveform with 50% average duty cycle (Manchester encoded) at a data rate of 1kbps.
5. When data burst does not contain preamble, duty cycle is defined as total duty cycle, including any "quiet" time between data bursts. When data bursts contain preamble sufficient to charge the slice level on capacitor  $C_{TH}$ , then duty cycle is the effective duty cycle of the burst alone. [For example, 100msec burst with 50% duty cycle, and 100msec "quiet" time between bursts. If burst includes preamble, duty cycle is  $Ton/(Ton+Toff) = 50\%$ ; without preamble, duty cycle is  $Ton/(Ton+ Toff + Tquiet) = 50\text{msec}/(200\text{msec})=25\%$ . Ton is the (Average number of 1's/burst) x bit time, and Toff = Tburst -Ton.)

## Typical Characteristics

### Sensitivity Graphs



### LO Leakage in RF Port



## Functional Diagram

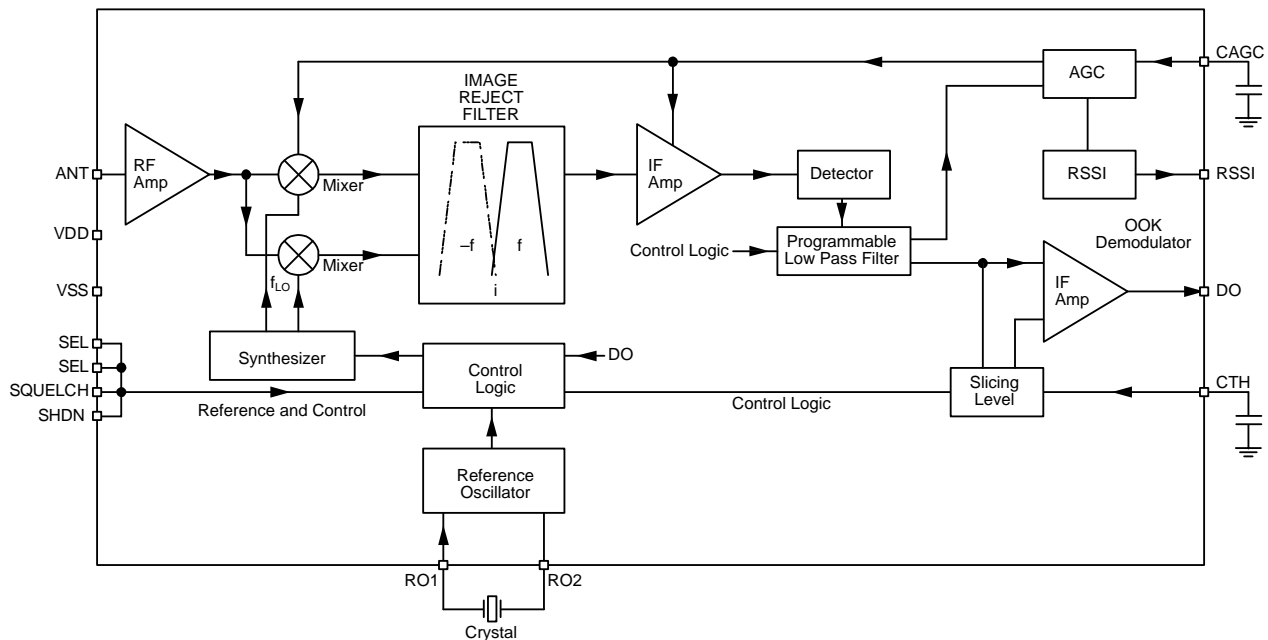


Figure 1. Simplified Block Diagram

## Functional Description

Figure 1. Simplified Block Diagram. It is the basic structure of the MICRF213. It is made of three sub-blocks; Image Rejection UHF Down-converter, the OOK Demodulator, and Reference and Control Logics. Outside the device, the MICRF213 requires only three components to operate; two capacitors (CTH, and CAGC) and the reference frequency device, usually a quartz crystal. An additional five components may be used to improve performance. These are: power supply decoupling capacitor, two components for the matching network and two components for the pre-selector band pass filter.

## Receiver Operation

### LNA

The RF input signal is AC-coupled into the gate circuit of the grounded source LNA input stage. The LNA is a Cascoded NMOS.

### Mixers and Synthesizer

The LO ports of the Mixers are driven by quadrature local oscillator outputs from the synthesizer block. The local oscillator signal from the synthesizer is placed on the low side of the desired RF signal. This allows suppression of the image frequency at twice the IF

frequency below the wanted signal. The local oscillator is set to 32 times the crystal reference frequency via a phase-locked loop synthesizer with a fully integrated loop filter.

### Image Reject Filter and Band-Pass Filter

The IF ports of the mixer produce quadrature down converted IF signals. These IF signals are low-pass filtered. This removes higher frequency products prior to the image reject filter where they are combined to reject the image frequencies. The IF signal then passes through a third order band pass filter. The IF center frequency is 0.86MHz. The IF BW is 235KHz @ 315MHz, this will vary with RF operating frequency. The IF BW can be calculated via direct scaling:

$$BW_{IF} = BW_{IF@315MHz} \times \left( \frac{\text{Operating Freq (MHz)}}{315} \right)$$

These filters are fully integrated inside the MICRF213.

After filtering, four active gain controlled amplifier stages enhance the IF signal to proper level for demodulation.

### OOK Demodulator

The demodulator section is comprised of detector, programmable low pass filter, slicer, and AGC comparator.

### Detector and Programmable Low-Pass Filter

The demodulation starts with the detector removing the carrier from the IF signal. Post detection, the signal becomes base band information. The programmable low-pass filter further enhances the base band information. There are four programmable low-pass filter BW settings: 1180Hz, 2360Hz, 4270Hz, 9400Hz for 315MHz operation. Low pass filter BW will vary with RF Operating Frequency. Filter BW values can be easily calculated by direct scaling. See the equation below for the filter BW calculation:

$$BW_{\text{Operating Freq}} = BW_{@315\text{MHz}} \times \left( \frac{\text{Operating Freq (MHz)}}{315} \right)$$

It is very important to choose filter setting that best fits the intended data rate as this will minimize data distortion.

Demod BW is set at 9700Hz @ 315MHz as default (assuming both SEL0 and SEL1 pins are floating). The low pass filter can be hardware set by external pins SEL0 and SEL1.

| SEL0 | SEL1 | Demod BW (@ 315MHz) |
|------|------|---------------------|
| 0    | 0    | 1180Hz              |
| 1    | 0    | 2360Hz              |
| 0    | 1    | 4270Hz              |
| 1    | 1    | 9400Hz - default    |

Table 1. Demodulation BW Selection

### Slicer, Slicing Level and Squelch

The signal, prior to slicer, is still linear demodulated AM. Data slicer converts this signal into digital "1"s and "0"s by comparing with the threshold voltage built up on the CTH capacitor. This threshold is determined by detecting the positive and negative peaks of the data signal and storing the mean value. Slicing threshold default is 50%. After the slicer, the signal becomes digital OOK data.

During long periods of "0"s or no data period at all, threshold voltage on the CTH capacitor may be very low. Large random noise spikes during this time may cause erroneous "1"s at DO pin. Squelch pin when pull down low will suppress these errors.

### AGC Comparator

The AGC comparator monitors the signal amplitude from the output of the programmable low-pass filter. When the output signal is less than 750mV threshold,

1.5µA current is then sourced into the external CAGC capacitor. When the output signal is greater than 750mV, a 15µA current sink discharges the CAGC capacitor. The voltage, developed on the CAGC capacitor, acts to adjust the gain of the mixer and the IF amplifier to compensate for RF input signal level variation.

### Reference Control

There are two components in Reference and Control sub-block: 1) Reference Oscillator and, 2) Control Logic through parallel Inputs: SEL0, SEL1, SHDN.

### Reference Oscillator

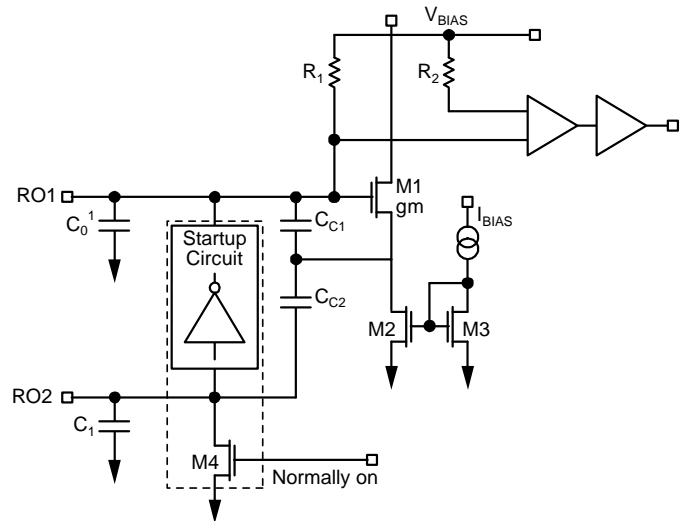


Figure 2. Reference Oscillator Circuit

The reference oscillator in the MICRF213 (reference Figure 2) uses a basic Colpitts crystal oscillator configuration with a MOS transistor to provide negative resistance. All capacitors shown in the figure are integrated inside MICRF213. R01 and R02 are external pins of MICRF213. The user only need connect the reference oscillation crystal.

Reference oscillator crystal frequency can be calculated thus as:

$$F_{\text{REFOSC}} = F_{\text{RF}} / (32 + 1.1/12)$$

For 315MHz,  $F_{\text{REFOSC}} = 9.81563 \text{ MHz}$ .

To operate the MICRF213 with minimum offset, crystal frequencies should be specified with 10pF loading capacitance.

## Application Information

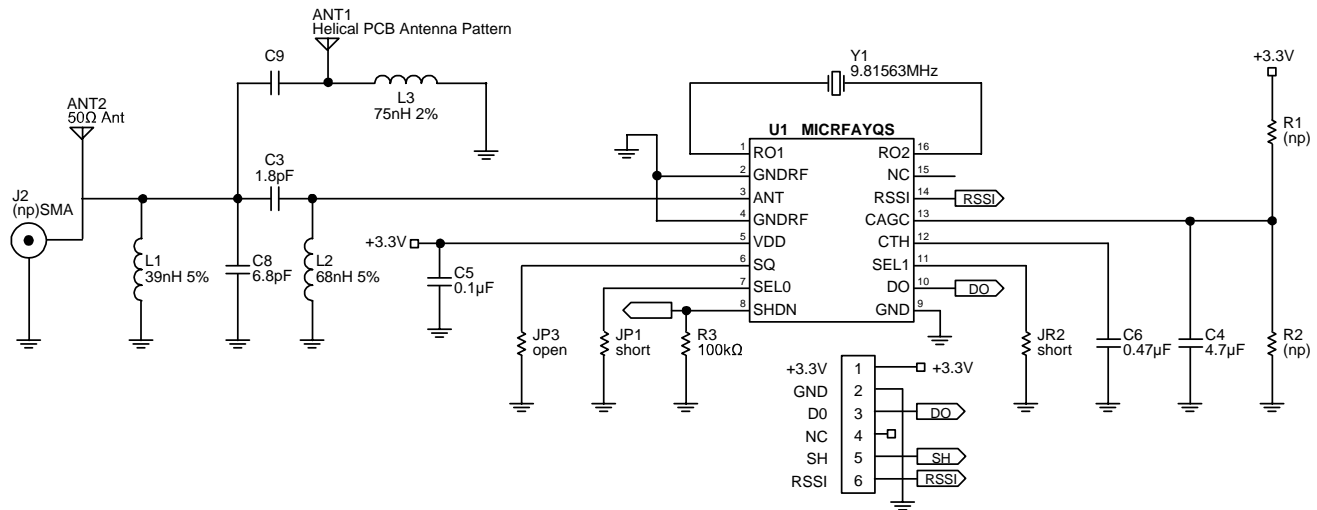


Figure 3. QR213HE1 Application Example, 315MHz

The MICRF213 can be fully tested by using one of the many evaluation boards designed by Micrel and intended for use with this device. As an entry level, the QR213HE1 (reference Figure 3) offers a good start for most applications. It has a helical PCB antenna with its matching network, a band-pass-filter front-end as a pre-selector filter, matching network and the minimum components required to make the device work. The minimum components are a crystal, Cagc, and Cth capacitors. By removing the matching network of the helical PCB antenna (C9 and L3), a whip antenna (ANT2) or a RF connector (J2) can be used instead. Figure 3 shows the entire schematic for 315MHz. Other frequencies can be used and the values needed are listed in the tables below.

Capacitor C9 and inductor L3 are the passive elements for the helical PCB matching network. It is recommended that a tight tolerance be used for these devices; such as 2% for the inductor and 0.1pF for the capacitor. PCB variations may require different values and optimization. Table 2 shows the matching elements for the device frequency range. For additional information, reference the: Small PCB Antennas for Micrel RF Products application note.

| Freq (MHz) | C9 (pF) | L3 (nH) |
|------------|---------|---------|
| 303.825    | 1.2     | 82      |
| 315        | 1.2     | 75      |
| 345        | 1.2     | 62      |

Table 2. Matching Values for the Helical PCB Antenna

To use another antenna, such as the whip kind, remove C9 and place the whip antenna in the hole provided in the PCB. Also, a RF signal can be injected there.

L1 and C8 form the pass-band-filter front-end. Its purpose is to attenuate undesired outside band noise which reduces the receiver performance. It is calculated by the parallel resonance equation  $f = 1/(2*PI*(SQRT(L1*C8)))$ . Table 3 shows the most used frequency values.

| Freq (MHz) | C8 (pF) | L1 (nH) |
|------------|---------|---------|
| 303.825    | 6.8     | 39      |
| 315        | 6.8     | 39      |
| 345        | 5.6     | 39      |

Table 3. Band-Pass-Filter Front-End Values

There is no need for the band-pass-filter front-end for applications where it is proven the outside band noise does not cause a problem. The MICRF213 has image reject mixers which improve significantly the selectivity and rejection of outside band noise.

Capacitor C3 and inductor L2 form the L-shape matching network. The capacitor provides additional attenuation for low frequency outside band noise and the inductor provides additional ESD protection for the antenna pin. Two ways can be used to find these values, which are matched close to 50Ω. One method is done by calculating the values using the equations below and another by using a Smith chart. The latter is made easier by using software that plots the values of the components C8 and L1, like WinSmith by Noble Publishing.

To calculate the matching values, one needs to know the input impedance of the device. Table 4 shows the input impedance of the MICRF213 and the suggested matching values used for the most frequencies.



Please keep in mind that these suggested values may be different if the layout is not exactly the same as the one depicted here.

| Freq (MHz) | C3 (pF) | L2 (nH) | Z device (Ω)  |
|------------|---------|---------|---------------|
| 303.825    | 1.8     | 72      | 34.6 – j245.1 |
| 315        | 1.8     | 68      | 32.5 – j235   |
| 345        | 1.8     | 56      | 25.3 – j214   |

**Table 4. Matching Values for the Most Used Frequencies**

For the frequency of 315MHz, the input impedance is  $Z = 32.5 - j235\Omega$ , then the matching components are calculated by:

Equivalent parallel =  $B = 1/Z = 0.577 + j4.175$  msiemens

$R_p = 1 / \text{Re} (B)$ ;  $X_p = 1 / \text{Im} (B)$

$R_p = 1.733 \text{ k}\Omega$ ;  $X_p = 239.5 \Omega$

$Q = \text{SQRT} (R_p/50 + 1)$

$Q = 5.972$

$X_m = R_p / Q$

$X_m = 290.21 \Omega$

Resonance Method For L-shape Matching Network

$L_c = X_p / (2.Pi.f)$ ;  $L_p = X_m / (2.Pi.f)$

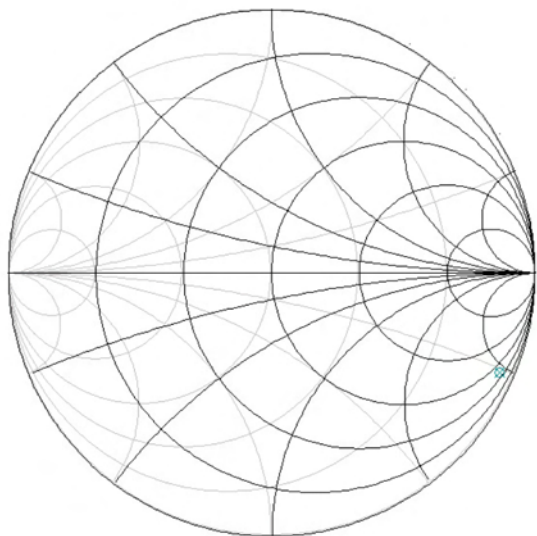
$L_2 = (L_c.L_p) / (L_c + L_p)$ ;  $C_3 = 1 / (2.Pi.f.X_m)$

$L_2 = 66.3\text{nH}$

$C_3 = 1.74\text{pF}$

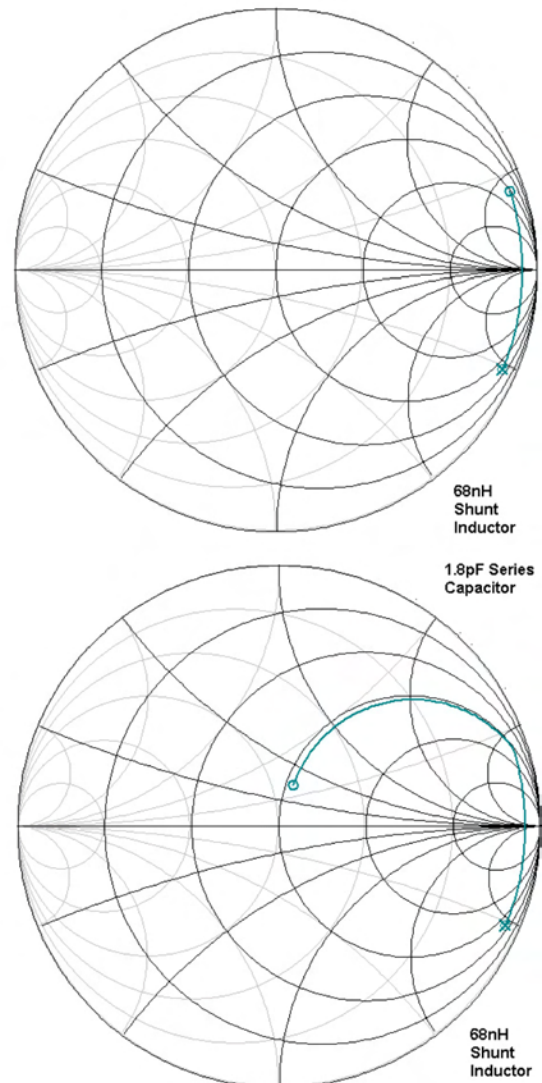
Doing the same calculation example with the Smith Chart, it would appear as follows,

First, we plot the input impedance of the device, ( $Z = 32.5 - j235\Omega$  @ 315MHz.(Figure 4).



**Figure 4. Device's Input Impedance,  $Z = 32.5 - j235 \Omega$**

Second, we plot the shunt inductor (68nH) and the series capacitor (1.8pF) for the desired input impedance (Figure 5). We can see the matching leading to the center of the Smith Chart or close to 50Ω.



**Figure 5. Plotting the Shunt Inductor and Series Capacitor**

Crystal Y1 or Y1A (SMT or leaded respectively) is the reference clock for all the device internal circuits. Desired crystal characteristics are: 10pF load capacitance, 30ppm, ESR < 50Ω and a -40°C to +105°C temperature range. Table 5 shows the crystal frequencies and one of Micrel's approved crystal manufactures ([www.hib.com.br](http://www.hib.com.br)).

The oscillator of the MICRF213 is a Colpitts type. It is very sensitive to stray capacitance loads. Thus, very good care must be taken when laying out the printed circuit board. Avoid long traces and ground plane on

the top layer close to the REFOSC pins RO1 and RO2. When care is not taken in the layout, and crystals from other vendors are used, the oscillator may take longer times to start as well as the time to good data in the DO pin to show up. In some cases, if the stray capacitance is too high (>20pF), the oscillator may not start at all.

The crystal frequency is calculated by  $REFOSC = RF \text{ Carrier} / (32 + (1.1/12))$ . The local oscillator is low side injection ( $32 \times 9.81563\text{MHz} = 314.1\text{MHz}$ ), that is, its frequency is below the RF carrier frequency and the image frequency is below the LO frequency. Refer to Figure 6. The product of the incoming RF signal and local oscillator signal will yield the IF frequency, which will then be demodulated by the detector of the device.

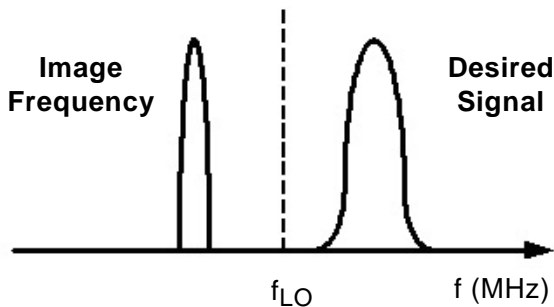


Figure 6. Low Side Injection Local Oscillator

| REFOSC (MHz) | Carrier (MHz) | HIB Part Number             |
|--------------|---------------|-----------------------------|
| 9.467411     | 303.825       | SA-9.467411-F-10-H-30-30-X  |
| 9.81563      | 315           | SA-9.815630-F-10-H-30-30-X  |
| 10.75045     | 345.0         | SA-10.750450-F-10-H-30-30-X |

Table 5. Crystal Frequency and Vendor Part Number

JP1 and JP2 are the bandwidth selection for the demodulator bandwidth. To set it correctly, it is necessary to know the shortest pulse width of the encoded data sent in the transmitter. Reference the example of the data profile, in the Figure 7, below:

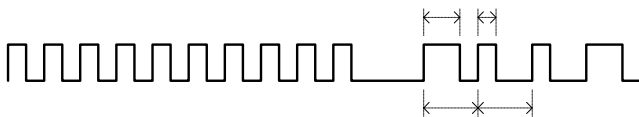


Figure 7. Example of a Data Profile

PW2 is shorter than PW1, so PW2 should be used for the demodulator bandwidth calculation. The calculation is found by  $0.65/\text{shortest pulse width}$ . After this value is found, the setting should be done

according to Table 6. For example, if the pulse period is  $140\mu\text{sec}$ , 50% duty cycle, then the pulse width will be  $70\mu\text{sec}$  ( $PW = (140 \mu\text{sec} * 50\%) / 100$ ). So, a bandwidth of  $9.286\text{kHz}$  would be necessary ( $0.65 / 70\mu\text{sec}$ ). However, if this data stream had a pulse period with a 20% duty cycle, then the bandwidth required would be  $23.2\text{kHz}$  ( $0.65 / 28\mu\text{sec}$ ), which exceeds the maximum bandwidth of the demodulator circuit. If one tries to exceed the maximum bandwidth, the pulse would appear stretched or wider.

| SEL0 JP1 | SEL1 JP2 | Demod. BW (hertz) | Shortest Pulse (usec) | Maximum baud rate for 50% Duty Cycle (hertz) |
|----------|----------|-------------------|-----------------------|--|
| Short    | Short    | 1180              | 551                   | 908  |
| Open     | Short    | 2360              | 275                   | 1815   |
| Short    | Open     | 4720              | 138                   | 3631   |
| Open     | Open     | 9400              | 69                    | 7230   |

Table 6. JP1 and JP2 Setting, 315MHz

Capacitors C6 and C4, Cth and Cagc capacitors respectively, provide the time base reference for the data pattern received. These capacitors are selected according to data profile, pulse duty cycle, dead time between two received data packets and if the data pattern has or not a preamble. See Figure 7 for an example of a data profile.

Other frequencies will have different demodulator bandwidth limits, which are derived from the reference oscillator frequency. Table 7 and Table 8, below, show the limits for the other two most used frequencies.

| SEL0 JP1 | SEL1 JP2 | Demod. BW (hertz) | Shortest Pulse (usec) | Maximum baud rate for 50% Duty Cycle (hertz) |
|----------|----------|-------------------|-----------------------|--|
| Short    | Short    | 1140              | 570                   | 8770   |
| Open     | Short    | 2280              | 285                   | 1754   |
| Short    | Open     | 4550              | 143                   | 3500   |
| Open     | Open     | 9100              | 71                    | 7000   |

Table 7. JP1 and JP2 Setting, 303.825MHz

| SEL0 JP1 | SEL1 JP2 | Demod. BW (hertz) | Shortest Pulse (usec) | Maximum baud rate for 50% Duty Cycle (Hertz) |
|----------|----------|-------------------|-----------------------|--|
| Short    | Short    | 1290              | 504                   | 992  |
| Open     | Short    | 2580              | 252                   | 1985   |
| Short    | Open     | 5170              | 126                   | 3977   |
| Open     | Open     | 10340             | 63                    | 7954   |

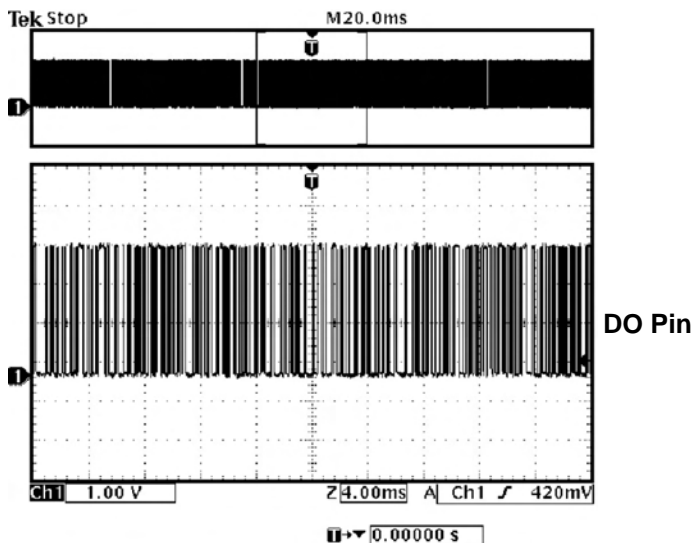
Table 8. JP1 and JP2 Setting, 345.0MHz

For best results, the values should always be optimized for the data pattern used. As the baud rate increases, the capacitor values decrease. Table 9 shows suggested values for Manchester Encoded data at 50% duty cycle.

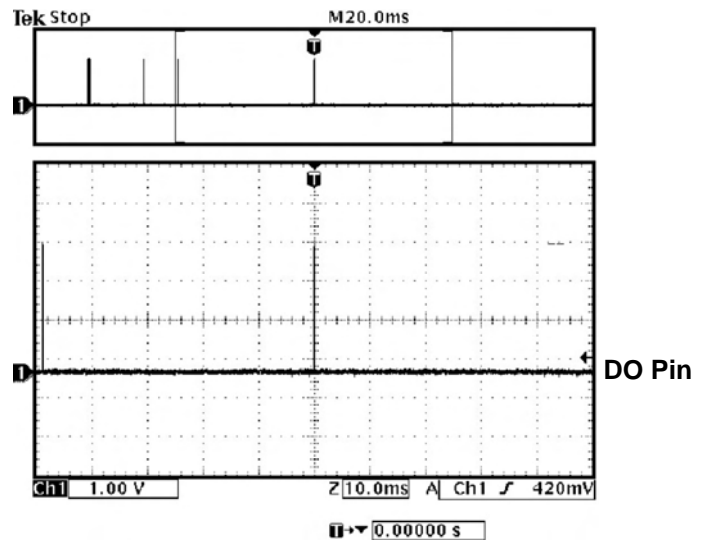
| SEL0 JP1 | SEL1 JP2 | Demod. BW (hertz) | Cth   | Cagc   |
|----------|----------|-------------------|-------|--------|
| Short    | Short    | 1400              | 100nF | 4.7uF  |
| Open     | Short    | 2800              | 47nF  | 2.2uF  |
| Short    | Open     | 5300              | 22nF  | 1uF    |
| Open     | Open     | 9700              | 10nF  | 0.47uF |

**Table 9. Suggested Cth and Cagc Values**

JP3 is a jumper used to configure the digital squelch function. When it is high, there is no squelch applied to the digital circuits and the DO (data out) pin yields a hash signal. When the pin is low, the DO pin activity is considerably reduced. It will have more or less than shown in the figure below depending upon the outside band noise. The penalty for using squelch is a delay in obtaining a good signal in the DO pin. That is, it takes longer for the data to show up. The delay is dependent upon many factors such as RF signal intensity, data profile, data rate, Cth and Cagc capacitor values, and outside band noise. See Figure 8 and 9.



**Figure 8. Data Out Pin with No Squelch (SQ = 1)**

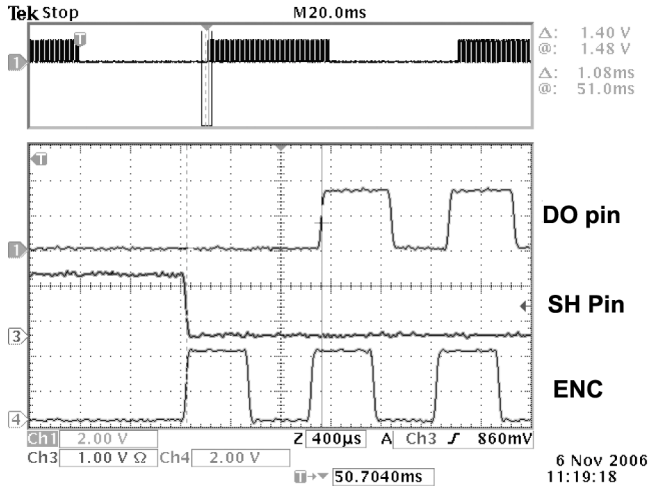


**Figure 9. Data Out Pin with Squelch (SQ = 0)**

Other components used include: C5, which is a decoupling capacitor for the Vdd line; R4 reserved for future use and not needed for the evaluation board; R3 for the shutdown pin (SHDN = 0, device is operation), which can be removed if that pin is connected to a microcontroller or an external switch; and R1 and R2 which form a voltage divider for the AGC pin. One can force a voltage in this AGC pin to purposely decrease the device sensitivity. Special care is needed when doing this operation, as an external control of the AGC voltage may vary from lot to lot and may not work the same in several devices.

Three other pins need to be discussed as well. They are the DO, RSSI, and shut down pins. The DO pin has a driving capability of 0.4mA. This is good enough for most of the logic families ICs in the market today. The RSSI pin provides a transfer function of the RF signal intensity vs. voltage. It is very useful to determine the signal to noise ratio of the RF link, crude range estimate from the transmitter source and AM demodulation, which requires a low Cagc capacitor value.

The shut down pin (SHDN) is useful to save energy. Making its level close to Vdd (SHDN = 1), the device is then not in operation. Its DC current consumption is less than 1µA (do not forget to remove R3). When toggling from high to low, there will be a time required for the device to come to steady state mode, and a time for data to show up in the DO pin. This time will be dependent upon many things such as temperature, crystal used, and if there is an external oscillator with faster startup time. Crystal vendors suggest that the data will show up in the DO pin around 1msec time, and 2msec over the temperature range of the device. See Figure 10.



**Figure 10. Time-to-Good Data After Shut Down Cycle, Room Temperature**

### PCB Considerations and Layout

Figure 11 through 16 show some of the printed circuit layers for the QR211HE1 board. The MICRF213 shares the exact same board with different component values. Use the Gerber files provided (downloadable from Micrel Website: [www.micrel.com](http://www.micrel.com)) which have the remaining layers needed to fabricate this board. When copying or making one's own boards, be sure and make the traces as short as possible. Long traces alter the matching network and the values suggested are no longer valid. Suggested Matching Values may vary due to PCB variations. A PCB trace 100 mills (2.5mm) long has about 1.1nH of inductance. Optimization should always be done with exhaustive range tests. Make individual ground connections to the ground plane with a via for each ground

connection. Do not share vias with ground connections. Each ground connection = 1 via or more vias. Ground plane must be solid and possibly without interruptions. Avoid ground plane on top next to the matching elements. It normally adds additional stray capacitance which changes the matching. Do not use phenolic material, only FR4 or better materials. Phenolic material is conductive above 200MHz. The RF path should be as straight as possible avoiding loops and unnecessary turns. Separate ground and VDD lines from other circuits (microcontroller, etc). Known sources of noise should be laid out as far as possible from the RF circuits. Avoid thick traces, the higher the frequency, the thinner the trace should be in order to minimize losses in the RF path.

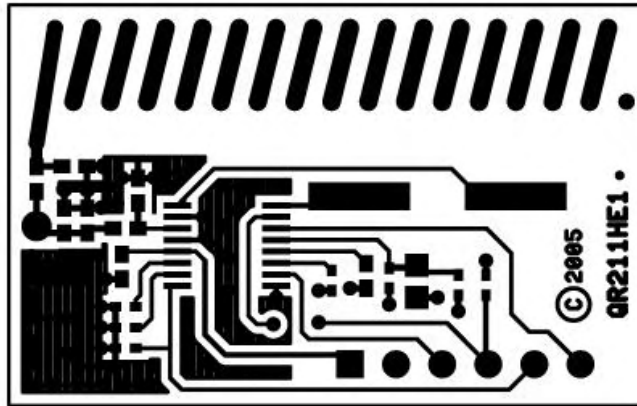


Figure 11. QR211/213HE1 Top Layer

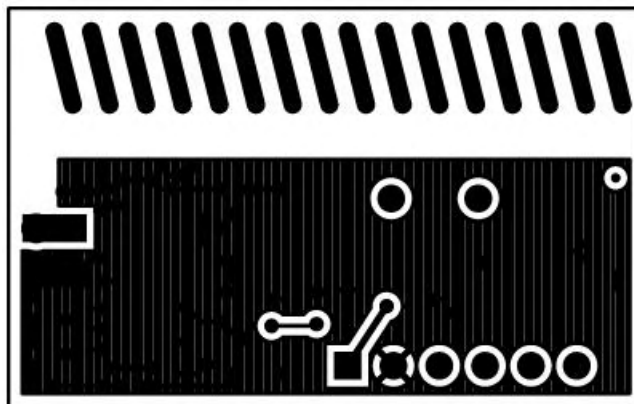


Figure 12. QR211/213HE1 Bottom Layer, Mirror Image

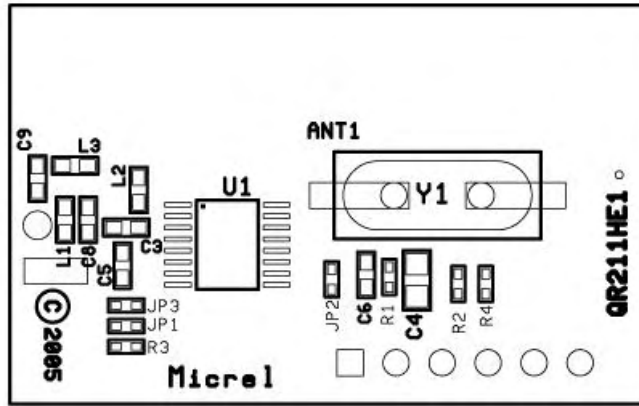


Figure 13. QR211/213HE1 Top Silkscreen Layer

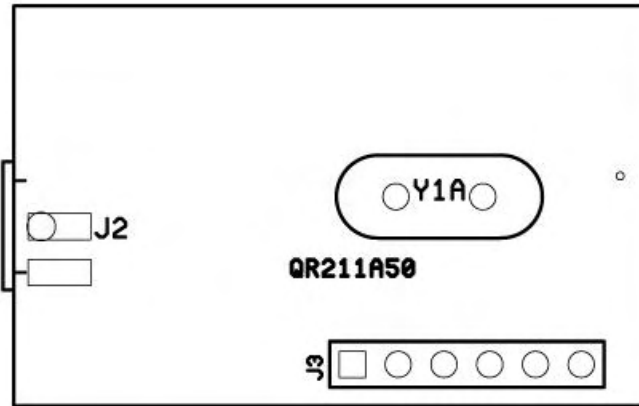


Figure 14. QR211/213HE1 Bottom Silkscreen Layer, Mirror Image

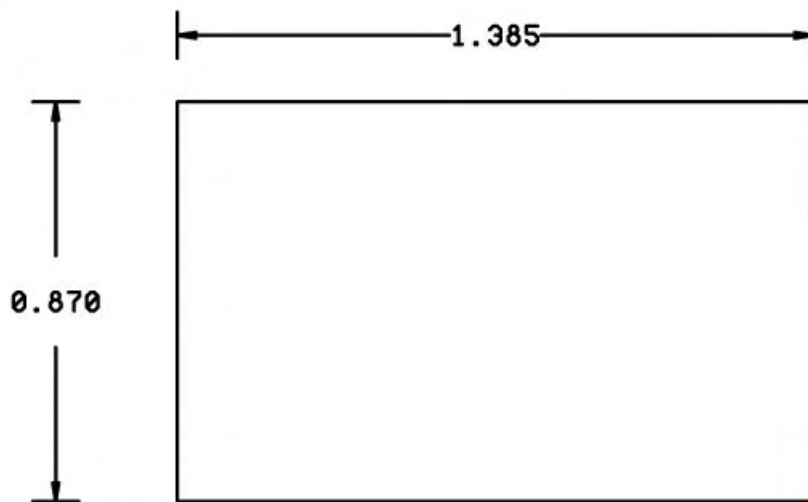


Figure 15. QR211/213HE1 Dimensions

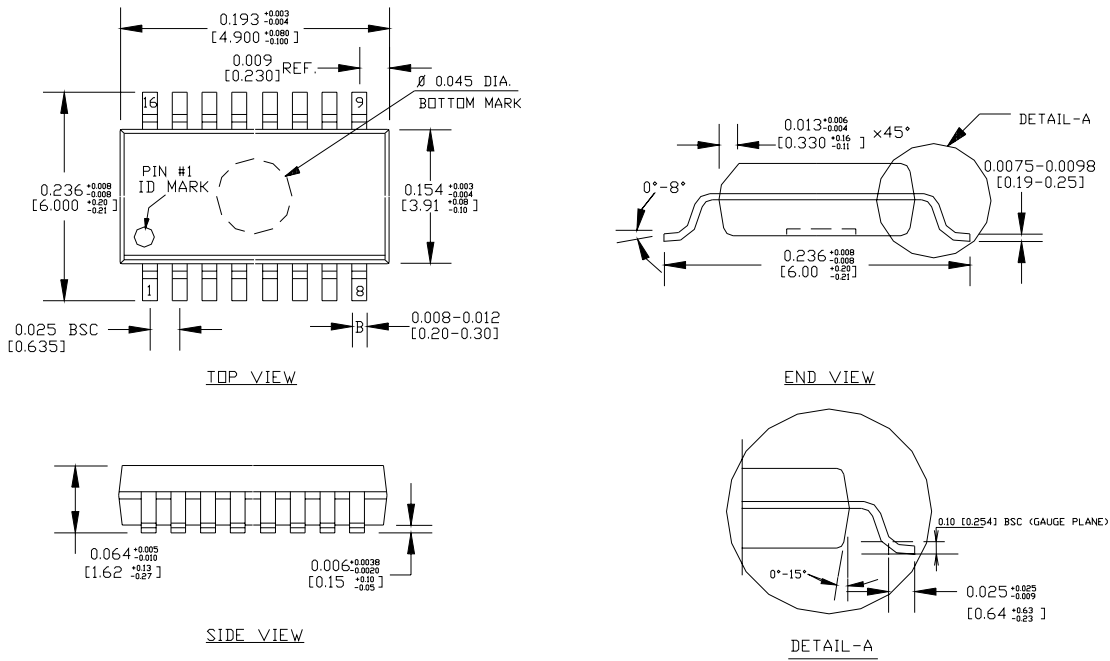
## QR213HE1 Bill of Materials, 315MHz

| Item        | Part Number         | Manufacturer   | Description  | Qty.     |
|-------------|---------------------|--|--|----------|
| ANT1        |                     |  | Helical PCB Antenna Pattern                        | 1        |
| ANT2        |                     |  | (np)50Ω Ant 230mm 20 AWG, rigid wire               | 1        |
| C3          |                     | MuRata <sup>(1)</sup>  | 1.8pF, 0402/0603                                   | 1        |
| C4          |                     | Murata <sup>(1)</sup> / Vishay <sup>(2)</sup>                          | 4.7μF, 0603/0805                                   | 1        |
| C5          |                     | Murata <sup>(1)</sup> / Vishay <sup>(2)</sup>                          | 0.1μF, 0402/0603                                   | 1        |
| C6          |                     | Murata <sup>(1)</sup> / Vishay <sup>(2)</sup>                          | 0.47μF, 0402/0603                                  | 1        |
| C8          |                     | Murata <sup>(1)</sup>  | 6.8pF, 0402/0603                                   | 1        |
| C9          |                     | Murata <sup>(1)</sup>  | 1.2pF, 0402/0603                                   | 1        |
| JP1,JP<br>2 |                     | Vishay <sup>(2)</sup>  | short, 0402, 0Ω resistor                           | 2        |
| JP3         |                     |  | open, 0402, not placed                             | 1        |
| J2          |                     |  | (np) not placed                                    | 1        |
| J3          |                     |  | CON6   | 1        |
| L1          |                     | Coilcraft <sup>(3)</sup> / Murata <sup>(1)</sup> / ACT1 <sup>(4)</sup> | 39nH 5%, 0402/0603                                 | 1        |
| L2          |                     | Coilcraft <sup>(3)</sup> / Murata <sup>(1)</sup> / ACT1 <sup>(4)</sup> | 68nH 5%, 0402/0603                                 | 1        |
| L3          |                     | Coilcraft <sup>(3)</sup> / Murata <sup>(1)</sup> / ACT1 <sup>(4)</sup> | 75nH 2%, 0402/0603                                 | 1        |
| R1,R2       |                     |  | (np) 0402, not placed                              | 2        |
| R3          |                     | Vishay <sup>(2)</sup>  | 100kΩ, 0402  | 1        |
| Y1          | HCM49               | HIB <sup>(5)</sup>   | (np)9.81563MHz Crystal                             | 1        |
| Y1A         | HC49                | HIB <sup>(5)</sup>   | 9.81563MHz Crystal                                 | 1        |
| <b>U1</b>   | <b>MICRF213AYQS</b> | <b>Micrel Inc.<sup>(6)</sup></b>                                       | <b>3.3V, QwikRadio<sup>®</sup> 315MHz Receiver</b> | <b>1</b> |

**Notes:**

1. Murata: [www.murata.com](http://www.murata.com)
2. Vishay: [www.vishay.com](http://www.vishay.com)
3. Coilcraft: [www.coilcraft.com](http://www.coilcraft.com)
4. ACT1: [www.act1.com](http://www.act1.com)
5. HIB: [www.hib.com.br](http://www.hib.com.br)
6. **Micrel, Inc.:** [www.micrel.com](http://www.micrel.com)

## Package Information



**NOTE:**

1. ALL DIMENSIONS ARE IN INCHES [MM].
2. LEAD COPLANARITY SHOULD BE  $0.004^b$  [0.10 mm] MAX.
3. MAX MISALIGNMENT BETWEEN TOP AND BOTTOM CENTER OF PACKAGE TO BE  $0.004^b$  [0.10 mm].
4. THE LEAD WIDTH, B TO BE DETERMINED AT .0075 [0.19 mm] FROM THE LEAD TIP.
5. BOTTOM MARK IS OPTIONAL, IT MAY NOT APPEAR ON THE ACTUAL UNITS.

### 16-Pin QSOP (QS)

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